Silicon Debug of Systems-on-Chips

Speakers
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Modern semiconductor process technologies, advanced design tools, and the reinvented reuse paradigm enable the design of very complex ICs. Some call these ICs 'system-on-chip', referring to the fact that their functionality could until recently only be implemented by one or several PCBs filled with ICs. While it was always difficult to locate design errors, guaranteeing that a deep sub-micron 'system-on-chip' is design error free is a real challenge. Floating specifications, growing geographically-spread design teams, time-to-market pressure, and the increasing distance of IC designers to actual silicon all make it likely that 'buggy' hardware will become as common as 'buggy' software.

Of course our industry does whatever is possible within given time and money budgets to prevent design errors before first silicon. Hereto techniques as simulation, emulation, and formal verification are used. However, all these techniques only deal with models of the IC, which do not take into account all effects that might occur on real silicon, and high computational costs often prevent exhaustive error coverage. In order to find design errors before the customer does, debug of actual silicon samples is inevitable.

This Hot Topic session provides an overview of the state-of-the-art in physical and electrical silicon debug. The speakers address techniques currently in use, their applications and their limitations, and the research challenges for the future. (EJM)

1 Physical Methods for Silicon Debug

Karel van Doorselaer - Alcatel Telecom (Antwerp, Belgium)

Silicon Debug can be needed at various stages in the lifecycle of a product (ASIC, system): during development, qualification, production ramp-up, or in *maintenance*-like activities in the field life of a product. The root cause of the problem-to-be-debugged can lie in the technology used, as well as in the design implementation (or the combination of these); the debugging process has to cover both aspects. Although it is clear that software tools and Design-for-Test are gaining in importance with the advent of systems-on-chip, physical debug methods have still an important role to play. One clear example is debugging of problems that are only visible by an increased supply current.

The presentation gives an overview of the different categories of physical debug methods, and illustrates their role in the total debug process.

- Physical methods for internal electrical analysis (e.g., probing, E-beam test), both on active circuitry and on isolated building blocks.
- Physical failure localisation techniques, based on thermal effects, photon emission, or the interaction of the circuitry with electron, ion, or photon beams.
- Physical device modification (e.g., using Focused Ion Beam) to verify and cure a supposed design bug.
- Physical analysis (deprocessing or cross-sectioning) to determine the root cause for problems in mask making or silicon processing.

Finally, the main challenges in this field w.r.t. the advent of new technologies (deep sub-micron, multiple metal layers, flip-chip, etc.) are clarified. (KvD)

Biography
Karel van Doorselaer received a M.Sc. degree in Physics from the University of Antwerp, Belgium in 1985 and a Ph.D. degree in Engineering Sciences from the University of Twente, The Netherlands in 1994. He has worked at the University of Antwerp and Philips Research Laboratories in Eindhoven. Currently, Van Doorselaer is group leader of Product Engineering, Technology & Reliability at Alcatel Telecom in Antwerp, Belgium.

2 Design-for-Debug of System-on-Chip Designs

Sridhar Narayanan - Sun Microsystems (Mountain View, California)

The complexity of system-on-chip designs in the future will provide numerous challenges for the test and debug community. With increasing levels of integration, use of high speed clocks, and aggressive time-to-volume goals, a systematic debug strategy must be set in place to deal with logic, circuit and timing errors.

In the chip industry, high-performance microprocessor design and test teams often get an early view of some of these upcoming challenges and problems. This observation is used to project the future demands in silicon debug of system-on-chip designs. As a first step, I provide an overview of some important Design-for-Debug techniques used in current microprocessor designs. These include the use of full and partial scan methodologies and their impact on debug and diagnosis; the use of clock control operations for checkpointing, single-stepping, and restart; initialization and memory dumps for RAM structures, and the use of internal controllability and observability hardware structures.

In addition, debug of timing errors through methods such as clock stretching and delay testing are briefly discussed. Based on this overview, an analysis is made on the use and modifications to these techniques to tackle the debug of future system-on-chip designs.

I conclude with some practical design examples, and some suggestions for new avenues in silicon debug of complex devices. (SN)

Biography
Sridhar Narayanan received the M.S. and Ph.D. degrees in Computer Engineering from the University of Southern California, Los Angeles in 1990 and 1994, respectively. Currently, Narayanan is a member of technical staff at Sun Microelectronics, a business unit of Sun Microsystems, Inc., California, USA. In his three years at Sun, he has worked on the Design-for-Test features, test verification, and debug aspects of three generations of UltraSPARC microprocessors, and other derivative devices. His main interests are in the areas of testing and design automation with emphasis on scan design, design for testability, built-in self test, and processor debug.

3 Tools for Silicon Debug of Systems-on-Chips

Gert Jan van Rootselaar - Philips Research (Eindhoven, The Netherlands)

First silicon contains design errors. This is a truth for today's complex system-on-chip designs. Only by following a well thought out strategy, and by using appropriate tools, we have a chance of finding errors within a reasonable amount of time. Analogous to test, a structured debug approach is a necessity. Such an approach encompasses Design-for-Debug (DfD) structures and debugger software. Together they provide an infrastructure for accessing the internals of the ICs at a suitable level of abstraction. In this talk we give a brief overview of required DfD. We then go on to discuss silicon debugger tools and their application in more detail.

Silicon debug tools give the user access to signals on the actual silicon in the same way as simulators provide access to the data in models. The user can, for example, create traces and set complex breakpoints. The tools then generate bit sequences which activate the appropriate on-chip DfD. These sequences are applied to the IC via tester hardware. Conversely, data read from the IC is abstracted to something that has meaning to the designer. (GJvR)

Biography
Gert Jan van Rootselaar received a M.Sc. degree in Electrical Engineering from Eindhoven University of Technology, The Netherlands in 1995. Van Rootselaar's current position is research scientist at the department of VLSI Design Automation & Test at Philips Research Laboratories in Eindhoven, The Netherlands. He is responsible for the development of methods and tools for debugging first silicon of system-on-chip ICs.