Design-Manufacturing Interface: Part I - Vision

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Abstract

This paper proposes a vision for a new research domain emerging on the interface between design and manufacturing of VLSI circuits. The key objective of this domain is the minimization of the mismatch between design and manufacturing which is rapidly growing with the increase in complexity of VLSI designs and IC technologies. This broad objective is partitioned into a number of specific tasks. Often, one of the most important task is the extraction of VLSI design attributes that may be relevant from a manufacturing efficiency standpoint. The second task is yield analysis performed to detect process and design attributes responsible for inadequate yield. This paper postulates both, an overall change in the design-manufacturing interface, as well as a methodology to address the growing design-manufacturing mismatch. Attributes of a number of tools needed for this purpose are discussed as well.

1.0 Introduction

The design-manufacturing interface can be seen as having evolved through three distinct phases. In Phase I, design and process development were conducted by the same small group of experts who could tune the process-design interface using all available “knobs” on both sides of the design-manufacturing border. This phase ended in the early 1970s, due to the large increase in the volume of ICs manufactured, and in the diversity of products fabricated on a single fab-line. Such increases prevent a simple centralized control of design/manufacturing operations. Another very important factor was the widespread adoption of simple design rules, enabling very efficient design automation but, at the same time, preventing fine tuning of designs.

In the second phase (still continuing in some places at present) design and manufacturing have been separated as much as possible to allow for “process independent” and, consequently, efficient design. The best measure of success of this trend is the emergence of fabless design houses which can perform efficient design with limited access to proprietary manufacturing data.

The third phase has just begun. To characterize this phase, it is useful to consider a timing factor which relates the key events of design with those of manufacturing. In Phase 2 this timing was simple - manufacturing process evolution was relatively well-synchronized with the ability of the design domain to absorb opportunities/restrictions provided by the newer versions of manufacturing processes. A simplified scenario of this “symbiotic” relationship is summarized in Fig. 1. In this scenario, the design of product “i” is guided by a set of design rules known to be effective from the previous version of the technology (process “r”). The design then is fabricated and its manufacturing efficiency (measured typically by manufacturing yield) is assessed. If the efficiency is not satisfactory, product “i” is redesigned with corrections ranging from optical mask shrink up to sophisticated changes in circuit timing. The redesigned circuit is then fabricated again. If yield is still inadequate, process modifications and another redesign cycle might be performed again. Of course, such a sequence of process-design tuning is possible if, and only if, the market permits such lengthy timetables of design and process corrections.

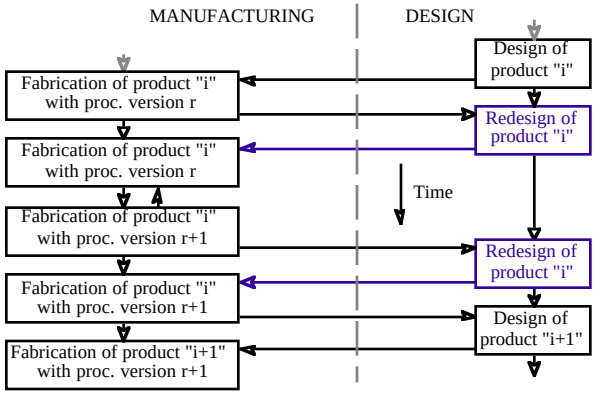

Fig 1. Manufacturing-design interface during a time period when simple design-manufacturing synchronizations are permitted (“phase 2”).

In Phase 3, relatively simple design-manufacturing synchronization is becoming a luxury available only to a few very high volume producers, who can afford time consuming and costly design-process tuning. For the majority of producers, the situation is different. They must deliver products to the market as quickly as possible and in a volume specified before hand. Also they must adapt to process and equipment changes that evolve according to product-independent (and often uncontrollable) agendas such as the one set by the SIA Roadmap. The rate of technology change enforced by these agendas, or by the high-volume-and-resource-rich IC producers, may not necessarily be optimal for IC fabricators who serve smaller but equally important segments of the IC market.

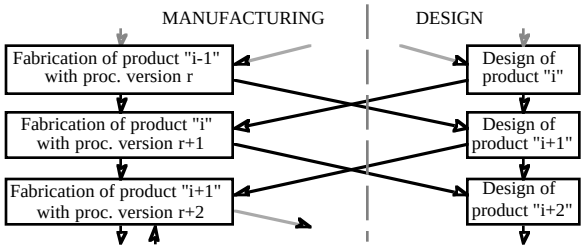

Fig 2. Manufacturing-design interface during a time period of rapid change (“phase 3”).

Consequently, the time domain relationship of the design-manufacturing interface in Phase 3 very often resembles the scenario depicted in Fig. 2. The characteristic feature of this scenario is that the design is performed when the process is not fully specified. Yet, the design must achieve a high and predictable level of manufacturability. As an example, in the likely scenario of Phase 3, product “i” must be designed when manufacturing experience is available only for a product of the previous generation (product “i-2”), fabricated with an “obsolete” version of the process (“r-1”). In addition, the rate of technology change is such that product “i” must be designed for technology “r+1”, which may be incompletely characterized or not even completely developed.

These conditions are usually very difficult to deal with and may lead to very inefficient designs. Therefore, for a growing segment of the IC industry, which is just entering Phase 3, it is essential to re-examine the paradigm of information exchange between design and manufacturing. Even from a simple discussion presented above, it is evident that this paradigm must be substantially modified. Such a modification should allow for accurate forecasting of future process capabilities/ restrictions and early assessment of manufacturability of the design. This should facilitate design correction without lengthy manufacturing experiments. The objective of this paper is to discuss a strategy for such modifications.

2.0 Illustration

The discussion presented in this paper is intended to influence and mobilize the forces capable of modifying both sides of the design-manufacturing interface. Therefore, it is essential that the ideas presented here be explained in the clearest possible manner, but without unacceptable simplifications. To that effect, an attempt has been made in this section to present a specific example of the design-manufacturing interface problem. This example is used to illustrate key points of the discussion which follows.

Let us assume that a CMOS product is to be designed in a technology which is in the process of being transferred from 6-inch to an 8-inch manufacturing facility. Let us also assume that the new technology uses a CMP (chemical mechanical polishing) process for planarization before all metal deposition steps. Of course such planarization is not perfect and even in a well controlled process, the surface of the wafer may not be flat after planarization. (See Fig. 3)

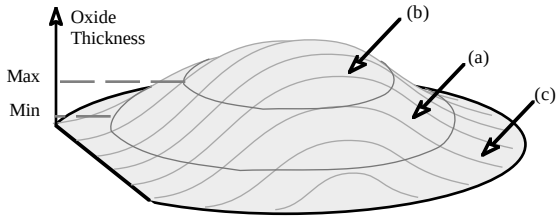

Fig 3. Surface of the manufacturing wafer after planarization.

Note that, even a difference of a fraction of a micrometer in the thickness of the polished layer (assuming that in our example this is the SiO_2 layer) may cause the drastic manufacturing problems illustrated in Fig. 4.

This figure shows cross-sections of three contact holes at the end of the etching process at three different locations (locations a, b and c in Fig. 3) on the wafer. Observe that contacts to active regions (source and drain of the p-MOS transistor) must be much deeper than the contacts to poly. This means that the etching process must be tuned such that deep contact holes are completely open while the shallow poly contact is still not over-etched. Such tuning is possible but variations in oxide thickness may cause situations shown in Fig. 4(b) and (c) - too thick an oxide layer may result in insufficient etching of diffusion contact holes (b) or too thin an oxide layer may cause over-etching of the poly contact (c). In both cases yield loss occurs due to non-uniform polishing. Such yield loss would manifest itself as the cumulative wafer map shown in Fig. 5 which is a possible outcome of the described CMP problem. (The cumulative yield wafer map is a representation of the wafer yield loss reported for each die site.)

The problem illustrated by the above example leads to the following question: How can one handle relationships between imperfections of new 8-inch wafer polishing process/equipment, design attributes, and yield loss data such that manufacturing efficiency (measured as a volume of fabricated and functional IC dies) is maximized? The new paradigm for the design-manufacturing interface described below should help to address this question.

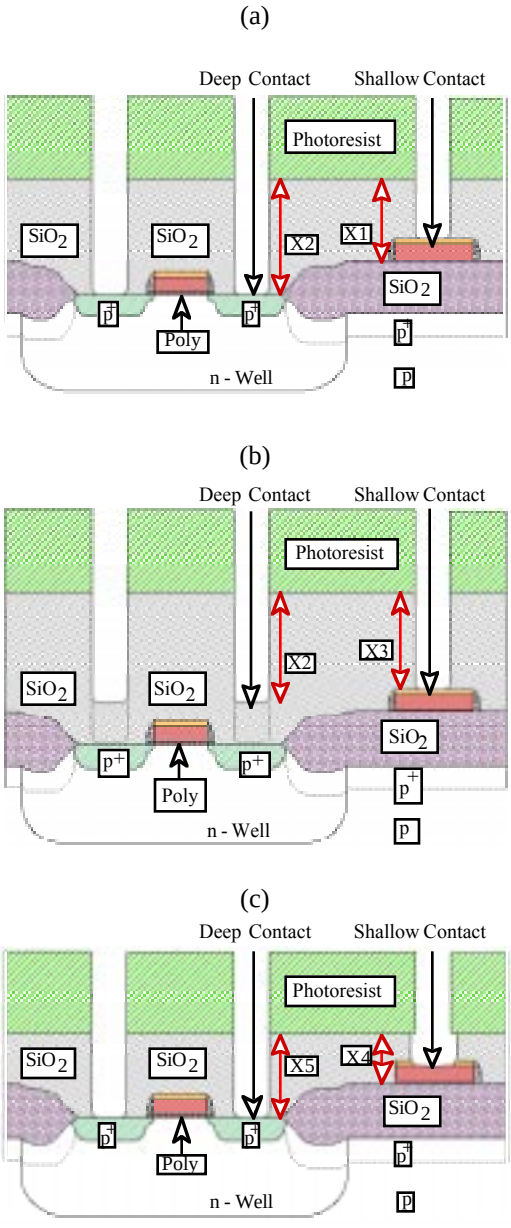

Fig 4. The cross-section of the same segment of a CMOS product in three different locations of a wafer.

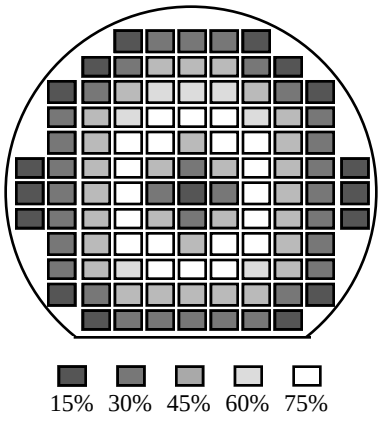

Fig 5. Cumulative yield wafer map.

3.0 New Design-Manufacturing Interface Paradigm [1]

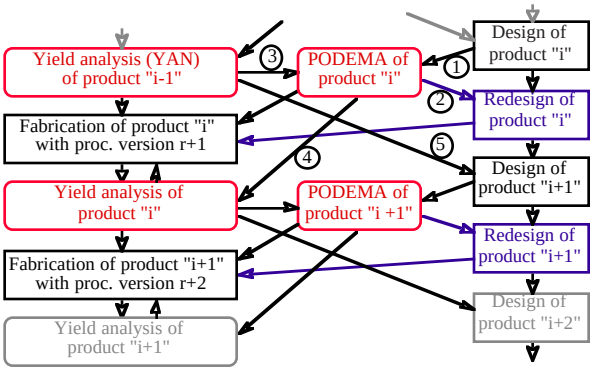

Fig 6. Design-manufacturing interface in the proposed paradigm.

The flow diagram in Fig. 6 captures the essence of the enhancement proposed for the design-manufacturing interface discussed in this paper. This diagram is derived from the one in Fig. 2 by adding two kinds of information processing capabilities: (a) yield analysis (YAN) and (b) post-design manufacturability assessment (PODEMA). The tasks to be handled by YAN and PODEMA are described below.

3.1 Yield Analysis

YAN is intended to produce:

a. A ranked list of causes of yield loss of the analyzed product;

b. Product-independent process characteristics related to yield;

c. A set of new design rules (or a set of design rule modifications) to minimize the impact of newly identified yield loss mechanisms.

d. A set of process guidelines or modifications necessary to achieve the desired yield.

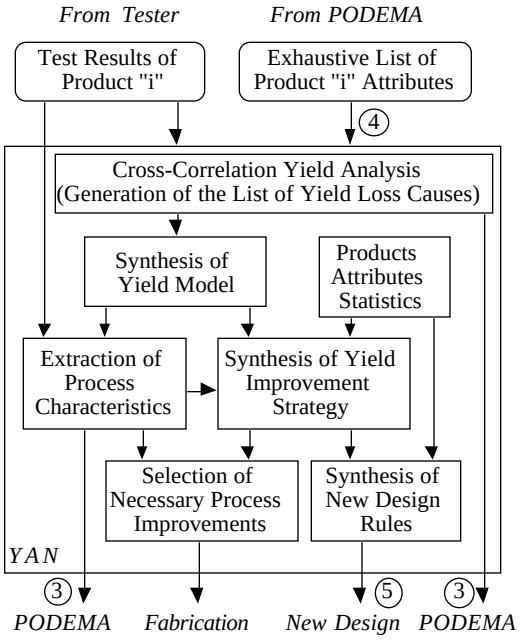

Fig 7. Organization of yield analysis.

A variety of ways exist in which YAN can be organized. One such organization is depicted in Fig. 7. Some of the procedures shown have been practiced in the industry in one form or another. Some of them are currently under development and some are yet to be developed. The key procedures of YAN are:

a. Cross-correlation yield analysis the objective of which is to produce a ranked list of phenomena that cause yield loss, and the associated list of design attributes that may have an impact on yield. The rationale is that by observing failures rates of distinct portions of the analyzed products, one will be able to correlate design attributes with observed yield loss. For the example in Sec. 2., cross-correlation yield analysis would involve two or more different portions of a product with different numbers of deep and shallow contacts. Analysis could determine, for instance, that the portion with more shallow contacts fails more often. This would be an indication that the shallow contacts are over-etched and that products with a large number of shallow contacts are likely to fail more often. Of course, the cross-correlation yield analysis process would have to start with a large number of design attributes. The reason is that at the beginning of analysis, there is very little indication of what phenomena could have caused the yield loss patterns observed on the cumulative yield maps (such as the one shown in Fig. 5).

b. Synthesis of the yield model which is intended to express yield as:

$$Y = \prod_{i=1}^{n} Y_i \qquad (1)$$

where Y_i is the yield loss of a particular failure mechanism from the yield loss list produced by the cross-correlation yield analysis. For instance, Yi could represent yield loss due to spot defects in each layer of the analyzed ICs. The yield model synthesis process should decide which of the potential yield loss mechanisms should be included in the model and how each partial yield (Y_i) should be expressed in terms of design attributes (e.g., critical area) and process characteristics (e.g., defect density). For the illustration in Sec. 2., the synthesis of the yield model involves deciding which of the yield loss phenomena should be included in the model and how to express each of them in terms of contact design rules, number of contacts and a measure of the randomness in the nonuniformity of oxide thickness.

c. Extraction of process characteristics which should generate all parameters of the postulated yield model. For the illustration of Sec. 2. the extraction would produce statistical characterization of the wafer polishing non-uniformities. Such a characterization should be product independent and applicable towards yield prediction of future products.

d. Synthesis of yield improvement strategy which should provide the answer to the question: which process characteristics and/or which design attributes should be changed to ensure acceptable yield for the analyzed product? For the illustration in Sec. 2. an yield improvement strategy could be either to increase the diffusion contact minimum size rule (in order to increase effective rate of etching of deep contacts), or change the polishing equipment, or change the contact etching settings.

e. Synthesis of new (modified) design rules for a given class of products which should translate specific yield improvement guidelines into a set of universal design rules. Such synthesis should be done with the current information about the process status (taken from process characterization) and the synthesized yield model. For the illustration in Sec. 2. this step would be to find the optimum value of the diffusion

contact cut. One could also envision design guidelines in the form of “soft design rules” encouraging minimum usage of contact banks (because etching rate can be affected in the regions with high density of deep contacts).

3.2 Post Design Manufacturability Assessment

The second proposed design-manufacturing interface capability, PODEMA, is intended for late assessment of a design’s manufacturability. Such an assessment should have the following consequences: either the analyzed design is classified as “good enough to be manufactured,” or as one which should be redesigned to meet an acceptable level of manufacturability. The proposed structure of PODEMA and its relation to YAN is shown in Fig. 8.

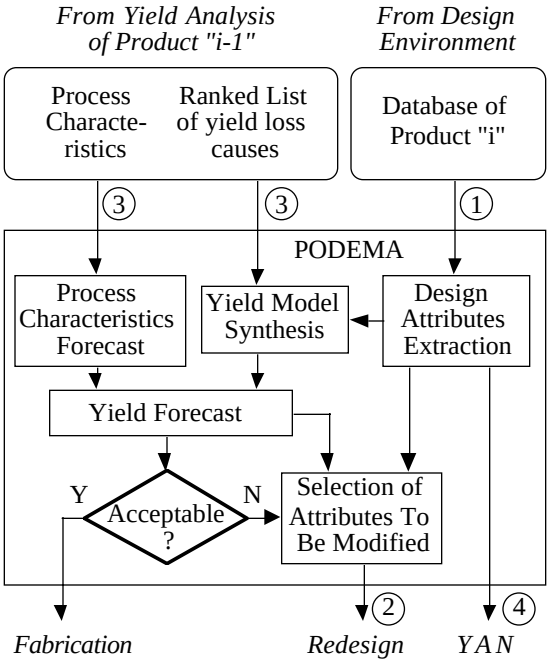

Fig 8. Organization of PODEMA.

Key functional blocks of PODEMA are:

a. Design attributes extractor which extracts an exhaustive list of the characteristics (also used by YAN) relevant to product yield. Such characteristics may include: critical areas for each layer and defect type, contact/via densities per functional block, sizes of antennas of various kinds, total area of gate oxide, total length of “bird’s beak”, clock imbalance index, and many others. (For more details see [3].)

b. Yield model compiler which produces a yield model template for an analyzed design. It takes as an input a ranked list of yield loss causes produced by YAN, and combines them with the product attributes.

c. Process characteristics forecaster which extrapolates current process characteristics into future versions of the process. For example, this block should predict the densities of defects for the process with a scaled down minimum feature size. For the example in Sec. 2 such a forecast should predict the distribution of oxide thickness for an 8-inch wafer based on 6-inch wafer distribution characterization data

d. Yield forecaster which should use the product yield model and predicted process characteristics to generate a yield forecast.

3.3 Interaction

Observe that the addition of YAN and PODEMA to the design-manufacturing interface has important implications. First of all PODEMA, when used as a “last minute” design check (arrows labeled 1 and 2 in Fig. 6), has the potential to filter out all design mistakes or “imperfections” introduced into the design, either due to the application of inadequate (or obsolete) design rules, or as an uncontrolled “by-product” of the employed design automation tools. Such filtration, if done with the most current information about the process (arrows labeled 3 in Fig. 6), can save time and cost in the early stages of the product development cycle. It can also help with the subsequent process modifications (arrow 4 in Fig. 6). Secondly, YAN can speed-up yield ramping, and at the same time produce guidelines for development of the next generation process (arrow 5 in Fig. 6). Finally, YAN and PODEMA can collectively deliver a much more complete, timely and accurate process characterization, thus facilitating more efficient Design for Manufacturability (DFM). It can be concluded, therefore, that the changes proposed here to the design-manufacturing paradigm, if implemented fully, do address one of the most pressing submicron domain problems - minimization of time to volume and consequently, minimization of time to money.

4.0 Status of PODEMA/YAN Vision

The vision described above has evolved over the years starting with the introduction of the critical area concept [4] and simple formalization of the yield analysis process [5] through intensive research conducted in CMU-SEMATECH Center of Excellence for Rapid Yield Learning founded in 1989, up to current interactions with many industrial partners. Some of the elements of yield analysis and DFM have been practiced since the beginning of the microelectronics era without being formalized or published. Given below is a brief evaluation of the status of YAN and PODEMA-related areas.

Yield analysis is performed on a daily basis in every IC manufacturing operation, although in an informal manner. The objective is to produce a ranked list (pareto

chart) of key yield detractors [6,7]. Yield analysis such as that proposed for YAN has not been reported yet. Some of its elements, however, have been proposed and/or developed in the past. Some form of cross-correlation yield analysis was applied at one of the Fairchild bipolar plants [8]. Yield model synthesis is also practiced in industry. But experiment-based yield models relating yield estimates to design attributes are usually not described in the literature. The only models of this kind published recently are models developed in collaboration between CMU, KLA and AMD [9]. Extraction of process characteristics needed for yield prediction is a large field. Currently, it is conducted using test structures (e.g. [10,11,12]), test results (e.g. [13]) or in-line measurements. However, the extracted characteristics are often in a form not directly translatable into yield figures. For instance, routinely collected CD measurements, which must be correlated to yield, cannot be utilized by simple yield models. The only exception is defect density data which has been used successfully with yield models. Synthesis of yield improvement strategy is again a domain which is informally practiced in industry. Such a synthesis is performed in an ad hoc manner with very little, if any, formal support. Synthesis of new (or improved) design rules is routinely done in industry as well. But again, the process of rule generation is rather informal and only a few papers dealing with this subject have been published (see e.g., [14,15]).

To summarize, the big-picture situation of yield analysis is as follows: Yield analysis is practiced in an informal way as a mean of yield improvement and control. Experimental yield models are built sometimes but these are rarely intended for, and capable of, yield prediction of new designs that are substantially different from those used in the model building process. The only exceptions are the critical area based yield models [4,9, 16,17,18,19,20] which can produce adequate predictive accuracy under the condition that proper defect data is available.

Post-design manufacturability assessment - PODEMA - in the form proposed in this paper is new, but it can be seen as a natural expansion of the Manufacturability Extraction Environment - MAPEX [3] (which has been inspired, in turn, by Fairchild's approach to yield analysis [8]). Status of key PODEMA components is as follows:

Design Attribute Extraction has been developed very intensely by CMU in collaboration with some of their Research Affiliates including: AMD, CADENCE, IBM, National Semiconductor, Philips and Siemens. The main vehicle used in the extraction was MAPEX [3] with a number of upgrades [21,22,23]. The upgraded version is referred to as MAPEX 2 [3]. Yield Model Synthesis is a domain discussed in numerous publications. The bottom-line assessment of this field can be summarized in the following way. There are two kinds of models which can approximate yield loss in a reasonable manner: experimental, fudge-factor based models and spot defect-based models. Fudge-factor based models are not very useful for PODEMA purposes. The spot defect models do not cover a number of yield loss mechanisms which are important in the early stages of process-design tuning. The conclusion is, therefore, that yield model synthesis has not yet been developed to an adequate level. Process Characteristics Forecasting must be a key element of any process development activity. It seems, however, that such forecasting is performed in a rather informal manner (and is often based on a given need - for instance a need to achieve the SIA Roadmap milestone - rather than on the modeling of the involved physics). Yield Forecasting is as good as the yield models applied and predictions of process quality. Currently, PODEMA-relevant yield forecasting is in its infancy and the only published yield forecasting technique is implemented in CMU's Y4 simulator [24,25].

Hence, one must conclude that despite reported effort, the design-manufacturing interface forms an important bottle-neck for further growth of microelectronics. This interface also seems to require a substantial investment, especially as far as computer applications are concerned. The reported results may, however, form a basis for future developments. The most advanced component of the design-manufacturing interface, as of now, seems to be post-design attribute extraction [3] - the key element of PODEMA.

5.0 Conclusions

The short characterization of the basis for change of the design - manufacturing paradigm discussed in this paper indicates that:

a. Despite overwhelming evidence that such a change is needed there is not enough intellectual or organizational momentum which could lead to the materialization of the vision proposed.

b. The key missing components are:

   b.1 Formal basis for efficient cross-correlation yield loss analysis;

   b.2 Yield models covering yield loss mechanisms other than spot defects;

   b.3 Modeling techniques allowing forecasting of yield loss mechanisms for newly developed processes.

   b.4 A methodology to translate newly detected manufacturability limitations into a set of design rules and design guidelines in a form acceptable by modern DA tools.

c. A few components which have recently been developed include:

   c.1 Design attributes extraction methodology, algorithms and software [3].

   c.2 Experimental evidence that key elements of the vision described in this paper may have an impact on the efficiency of design-manufacturing interface [26].

It is our contention that much needed change in the design-manufacturing interface can be accomplished if adequate investment in talent, time and money is committed in order to develop all components of YAN and PODEMA.

Acknowledgments

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