Microsystems Testing: an Approach and Open Problems

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Abstract

In this work a Computer-Aided Testing (CAT) tool is proposed that brings a systematic way of dealing with testing problems in emerging microsystems. Experiments with case-studies illustrate the techniques and tools embedded in the CAT environment. Some of the open problems that shall be addressed in the near future as an extension to this work are also discussed.

1. Introduction

The natural steps following the design and fabrication of microsystems aim at validating them at different phases of their lifetime. These steps include prototype debugging, post-fabrication and field testing. Similarly to the design, CAD and manufacture of microsystems with respect to microelectronics [10, 4, 5], some existing test techniques (specially those applicable to analog circuits) can be reused, and others need to be developed to cope with non-electrical parts of microsystems. Although many problems related to testing electronics can be supposed to be solved by existing techniques, with the advent of microsystems a number of unknowns have emerged:

- what are the failure mechanisms of non-electrical parts? what are their consequences at a higher level?
- how are (are not) these faults represented on the existing behavioural models?
- which input stimuli are needed to detect these faults? how to generate them automatically?
- how an appropriate layout design could easen detection or even avoid the occurrence of hard-to-detect faults?
- which faults may be detected by specific detectors/sensors like current and thermal detectors?

In this context, the goal of this work is to search for solutions for microsystems fault modeling, fault simulation, test signal generation and design for test problems, starting from the background on similar analog testing issues, and on microsystems design.

Few previous works have already addressed some of the questions above. [14] has pointed out many problems related to modeling faults in non-electrical elements and, it has discussed what would be the requirements to achieve fault simulation and test generation in microsystems. [9] addressed the design for test of micro-electro-mechanical systems, highlighting related fault simulation issues. Both works have made an important contribution to the field of microsystems testing, but none has clearly systematized its results, making it difficult to reuse the proposed testing techniques in a straightforward way.

In this work, this systematization is achieved by means of a Computer-Aided Testing (CAT) environment that goes further than simply integrating the contributions of the previous works. It also provides a library of fault models, a fault injection tool that instantiates these fault models into microsystem fault simulations, a tool that guides the process of searching input test stimuli and, a set of design for test strategies, that ranges from accessibility improvement to the on-chip test response analysis and the integration of testing sensors.

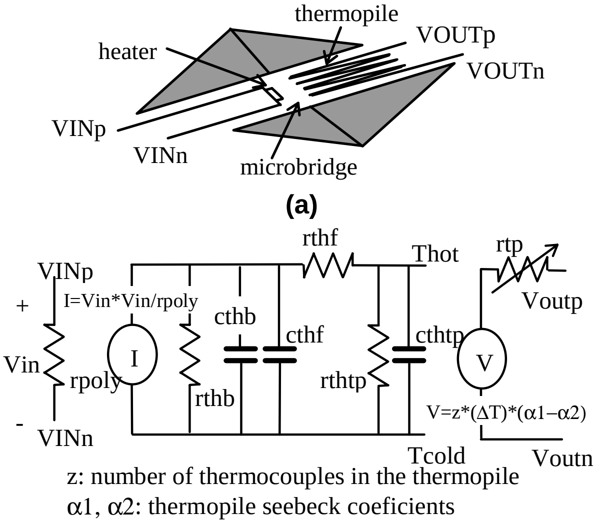
2. Fault Modeling

The modeling of non-electrical elements is usually based on a set of equations of the same nature as those modeling electrical elements. But faults that do exist in the non-electrical elements are not obviously represented in the model, and faults that might eventually be derived from the model do not necessarily represent faults of the actual non-electrical elements.

Sometimes, fault modeling of the non-electrical elements might come up as a matter of simply reusing analog fault models, but this is certainly not true in cases where the equivalent electrical circuit does not properly model distributed effects [14]. To cover both cases, two complementary approaches are merged is this work:

The first one is based on modeling single non-electrical defects as analog faults (multiple and parametric, in general). Defects are then injected into the microstructure fault-free description by changing the nominal values of components of the modeling circuit, in which case the modified description is referred to as a mutant [3].

To illustrate this way of modeling, let us consider the Electro-Thermal Converter (ETC) shown in figure 1(a). The behaviour of this ETC can be modeled by the circuit in figure 1(b) [15]. A defect, such as a break of the microbridge without breaking the heater and the thermopile, can be modeled by changing the values of rthf and cthf (the thermal resistance and capacitance of the path from the heater to the thermopile hot junction) of the circuit in figure 1(b) [6]. This single defect is thus mapped onto a multiple parametric (analog) fault. Single catastrophic (analog) faults, although less usual than multiple parametric faults, can also result from such a mapping. This is the case of a a heater open circuit that is modeled by simply reassigning to rpoly an infinity value.



z: number of thermocouples in the thermopile

α1, α2: thermopile seebeck coeficients

(b)

Figure 1 - Electro-thermal converter (ETC):
(a) microstructure; (b) behavioural model.

The second fault modeling approach is based on the addition of new elements to a microstructure behavioral model, such that they can properly represent the distributed effects of some failures associated to the micromachining fabrication steps. Those additional elements, used for modeling bridging faults in digital circuits [2], are referred to as saboteurs [3].

To illustrate the use of saboteurs for microsystems fault modeling, let us consider the resonant silicon beam force sensor shown in figure 2(a). Figure 2(b) shows the equivalent electrical circuit used for modeling the behaviour of the stimulation/readout parts of the sensor. Local defects, such as missing or exceeding material on these parts, can only be properly considered if saboteurs are inserted at the location indicated in figure 2(b). In this specific case, every saboteur will be structurally identical to the original behavioural model. Then, depending on the granularity required for modeling actual defects, the appropriate number of saboteurs will be chosen. Figure 2(c) illustrates the use of a saboteur to divide the stimulation/readout parts into two identical regions subject to separate fault injection. Note also that the new modeling subcircuits must be mutants of the circuit in figure 2(b), in order to ensure that, in the absence of faults, the circuit in figure 2(c) behaves identically to the original behavioural model of the force sensor. In [14], experimental results demonstrate the need of splitting up the sensor behavioural model before going into a fault simulation procedure.

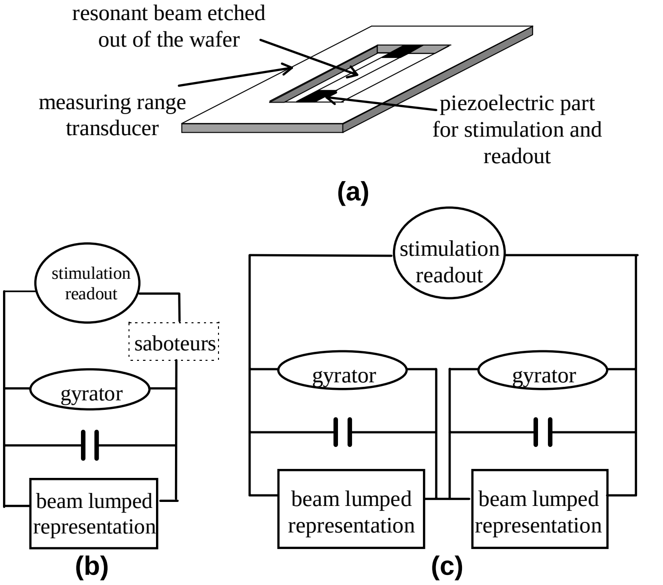


Figure 2 - Resonant beam force sensor [14]:
(a) microstructure; (b) stimulation/readout equivalent circuit;
(c) using saboteurs for fault modeling.

Silicon experiments are still needed to certify that the behaviour of some physical failures are properly modeled either as a mutant, or as a saboteur, in the electronic representation of the micro-mechanical elements.

3. Fault Simulation

In order to minimise efforts, instead of developping a completely new fault simulator, the injection of faults into the input description of the mixed-mode simulator ELDO (from Mentor Graphics) brings a pragmatic solution for the fault simulation of microsystems in our CAT environment. Fault injection is then achieved by simply modifying the fault-free microsystem description by instantiating mutant and saboteur descriptions of an HDL-A fault model library. In addition to conventional digital and analog single faults occuring in intrinsic (thermal, current, etc) microsensors, this library must model multiple parametric, bridging and open circuit faults, missing and exceeding material defects, for a variety of micro-electro-mechanical structures.

Figure 3 summarizes the main features of the fault simulation tool used in this work. To illustrate the use of this tool, let us consider an unetched microbridge defect in the ETC of figure 1(a).

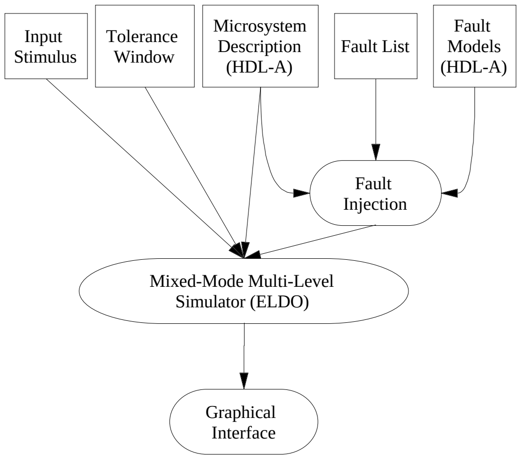


Figure 3 - The fault simulation environment

This defect is modeled as a mutant of the circuit in figure 1(b): rthf and cthf (thermal resistance and capacitance of the path from the heater to the thermopile), rthb and cthb (thermal resistance and capacitance of the path from the bulk to the air) have their nominal values either multiplied, or divided by a factor of 1000. This fault, was injected into the converter and simulated using a pulse with a duration of 150ms and an amplitude of 2.5V as input stimulus. The fault-free and faulty behaviour of the circuit under test are shown in figure 4. The fault-free and faulty output voltages are denoted in figure 4 as V and V2 respectively.

4. Test Generation

The process of searching input stimuli that activate and propagate faults to microstructures measuring points is assisted in this work by the ELDO-based fault simulation tool described in the previous section. The test generation procedure is based on the sensitivity-guided search process given in [8]. The sensitivity of a measuring parameter to a given component is defined as the ratio of the fractional change in the former to the fractional change in the latter. Experimental sensitivity figures are obtained by simulating the good and the faulty microstructure modeling circuit. The input stimuli range is provided by the user to the test generation tool. The initial test stimulus computed by this tool corresponds to the middle of the input range of interest. The test generation procedure checks by means of fault simulation whether or not every fault in the fault list is detected by measuring the test parameter under consideration. Those faults for which detection is ensured are dropped from the fault list. Those undetected faults are then checked by applying to the circuit two new input stimuli, one higher and another lower than the initial value (both in the middle of the corresponding ranges of interest). Yet undetected faults are partitioned into two new lists, one containing those faults for which the sensitivity of the measuring parameter is higher for higher input stimuli and, another containing those faults for which the sensitivity is higher for lower input stimuli. The procedure is recursively applied to the new lists, until all faults are detected or a maximum number of trials is reached.

Figure 5 summarizes the main features of the test generation approach used in this work.

To illustrate the use of this tool, let us consider the test generation for the ETC of figure 1. Basically, the following ETC defects are modeled in our fault library:

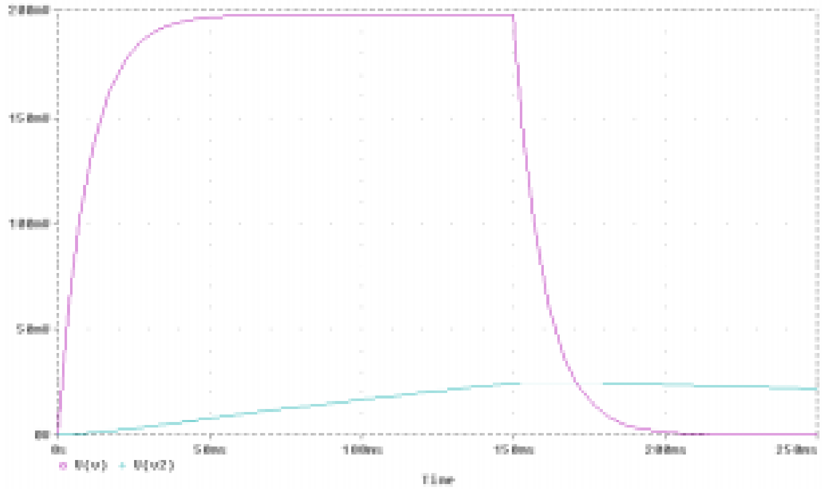


Figure 4 - ETC fault simulation for an unetched microbridge defect

heater and thermocouple open circuits, heater-thermocouple and thermocouple-thermocouple short circuits, unetched microbridge and, different possibilities of microbridge breaks and microbridge deformations.

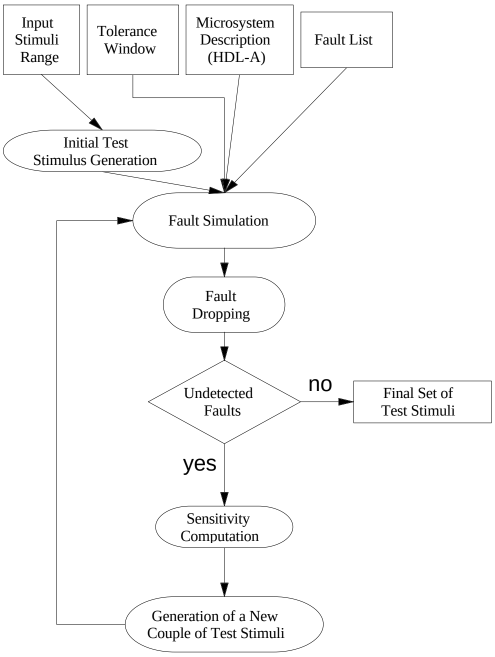

Input Stimuli Range
Tolerance Window
Microsystem Description (HDL-A)
Fault List
Initial Test Stimulus Generation
Fault Simulation
Fault Dropping
Undetected Faults
no
Final Set of Test Stimuli
yes
Sensitivity Computation
Generation of a New Couple of Test Stimuli

Figure 5 - The test generation environment

Considering a fault list consisting of all these faults, a range of stimuli amplitudes from 0 to 5V for the pulse Vin and, a tolerance window of ±5% for Vout, the test generation tool gives as result the following:

- Vin=2.5V detects all faults except the break of the microbridge without breaking the heater and the thermopile;
- the fault undetected at 2.5V remains undetected all over the input range.

On one hand, this test generation procedure cannot guarantee that it will find the best set of input test stimuli, be the criterion the error maximization or the minimal number of test stimuli. On the other hand, it can manage mutants and saboteurs exactly in the same way as it manages conventional single faults. If, similarly to [11], sensitivity figures were analytically computed for the whole input range, we might approach the best solution, but certainly could not avoid the exploding complexity of dealing with multiple analog faults (in the case of mutants) and increasingly complicate transfer functions (in the case of saboteurs).

5.Design for Testability and Built-in Self-Test

Even though a test generation tool is made available for microsystems testing, hard-to-detect faults can prevent that a good tradeoff between fault coverage and testing time is achieved. In these cases, the redesign of parts of the circuit can represent a possible solution to improve the acessibility to hard-to-test elements or to reduce the probability that faults occur at the layout level. The basic idea is then to choose an embedded layout line as test point in order to make it fully controllable and observable, thus enhancing the testability of the whole system. This choice is made based on defect-oriented experiments assisted by our ELDO-based fault simulator and test generator.

To illustrate this first design for test approach, we have considered the same bridge-type accelerometer sensor and fault model as in [9]. Realistic faults derived from actual defects occurring in the accelometer manufacturing line were modeled as mutants (parametric deviations) and as saboteurs (opens and resistive shorts). Our fault simulations confirmed the results obtained in [9].

In terms of design for test, another idea could be to build into microsystems self-test capabilities. One possibility is to achieve on-chip test response analysis in microsensors, for example.

The oscillation testing technique [1], for instance, has been reused in our test environment, to ensure the compliance with a capability already existing for checking microsystem analog blocks. Basically, this test method consists in converting every building block of the circuit under test into an oscillator, in measuring the oscillation frequency and, in comparing this frequency to a reference. Faults occurring in the components and/or parameters of the circuit under test should manifest themselves as a deviation of the oscillation frequency. In our specific case, a thermal sensor [13], originally providing an analog current-output, was redesigned in such a way that the current-output was converted into a frequency-output proportional to the measured temperature (figure 6).

Another built-in self-test possibility is to embed into microsystems specific detectors like current [7], thermal [13] and other sensors, whenever fault detection can be easen or enhanced by measuring current, temperature, etc.

To exemplify the use of current sensors, let us consider the undetected fault in the ETC discussed in sections 3 and 4 (a break of the microbridge without breaking the heater and the thermopile).

Typically, this fault could become detectable if a metal wire was laid down along the microbridge and, a constant current flowing through this wire was provided by an embedded current source. Assuming that the wire would also break if the microbridge broke, a built-in current sensor could check (even on-line) the existence of a quiescent current in this wire not smaller than a reference value. The main disadvantage of this approach is the additional power consumption. The interference of the extra wire in the heater and the thermopile behaviour is yet to determine.

In the case of thermal sensors, the early detection of excessive power consumption can avoid that the associated chip deterioration leads to fatal failures in the field. Accelometers, for example, usually have associated to them some kind of temperature measurement. A built-in thermal sensor in this case, could be useful for on-line testing the microsystem sensing element, at the same time that it would not interfere in the behaviour of the circuit under test.

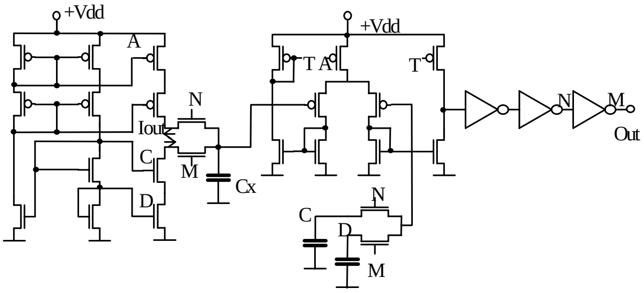


Figure 6 - Current-based temperature sensor with frequency-output

6. Conclusions

In this paper, a Computer-Aided Testing (CAT) environment was presented that deals with fault modeling, fault simulation, test generation and design for test of microsystems. Contrarily to previous works, the CAT tools provide a systematic way of preparing microsystems testing. Other novelties brought in by this work are:

- the development of a library of HDL-A fault models based on the mutant and saboteur concepts. This library is used for fault injection and ELDO-based fault simulation;
- a test generation tool capable of guiding the process of stimuli search by means of fault simulation and sensitivity computation; and,
- a set of design for test strategies, ranging from ad-hoc solutions derived from defect-oriented experiments, to the convertion of sensors into oscillators and the use of built-in current and thermal sensors.

Some case studies were presented in this paper in order to illustrate the many techniques and tools embedded in the proposed CAT environment.

The contributions mentionned above have been serving to answer many questions related to testing stand-alone (electrical and non-electrical) microsensors. But a lot is still to do regarding fault experiments, fault avoidance, optimal test generation, etc, to definitely put in phase microelectronics and micromechanics testing. In the near future, some of the many open problems that shall be addressed as an extension of this work are:

- the definition of a common computer-aided platform allowing to jointly simulate realistic faults and generate tests for both electronic (digital and analog) and micro-mechanical devices;
- the proposal of new structures for the design for testability and built-in self-test of electrical and non-electrical microsystem components, based on the testing requirements derived from the defect-oriented experiments.

7. References

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