Estimation of the Defective I_{DDQ} Caused by Shorts in Deep-Submicron CMOS ICs

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Abstract

The defective I_{DDQ} in deep-submicron full complementary MOS circuits with shorts is estimated. High performance and also low power scenarios are considered. The technology scaling, including geometry reductions of the transistor dimensions, power supply voltage reduction, carrier mobility degradation and velocity saturation, is modeled. By means of the characterization of the saturation current of a simple MOSFET, a lower bound of I_{DDQ} defective consumption versus L_{eff} is found. Quiescent current consumption lower bound for shorts intragate, and shorts intergate affecting at least one logic node is evaluated. The methodology is used to estimate the I_{DDQ} distribution, for a given input vector, of defective circuits. This I_{DDQ} estimation allows the determination of the threshold value to be used for the faulty/fault-free circuit classification.

1 Introduction

A bridging failure is one of the most frequent defect mechanisms appearing in mature CMOS processes. I_{DDQ} testing techniques have been established as an efficient support for testing bridges in long channel CMOS, high threshold voltage (V_{TH}) circuits [1]. The low quiescent current consumption (I_{off}) of defect-free CMOS circuits in conjunction with the high quiescent current consumption (I_B) of a large class of defective C.U.T.s is the fundamental requirement of this technique. Provided that I_B differs (exceeds) sufficiently from I_{off} in long channel, high V_{TH} technologies, the defect is easily detectable. However, the expected technology scaling trends predicts remarkable I_{off} increase as well as I_B decrease [2], [3], [4].

During the last years, several researchers have addressed the problem of the DC characterization of deep-submicron MOSFETs [5], [6], [7]. In relation to their quiescent consumption, two different behaviours are observed depending on the level of carrier inversion considered; for the strong inversion biasing case, the physical mechanisms governing deep-submicron MOSFETs transistors cause their (saturation) currents, I_{Dsat}, to decrease for a given W/L ratio in comparison with long channel, high V_{TH} devices. However, the opposite trend is observed in the subthreshold biasing of the MOSFETs. In fact, the quiescent current consumption in this region for the particular $|V_{GS}|$=0 value, the off-state current (I_{off}), increases drastically in short channel, low V_{TH} transistors.

Since I_B, the current flowing through a defective circuit, is directly related to I_{Dsat} and decreases for short channel, low V_{TH} transistors, I_B seems to decrease for future technologies. On the other hand, the off-state current has been found to increase for deep-submicron circuits. Due to the mentioned variations, the discrimination of good circuits from defective ones will require accurate estimation of the currents.

In this work, a lower bound of the quiescent current consumption for defective full complementary circuits (FCMOS) with bridging defects is presented. The assumed bridges include intragate shorts (shorting logical or internal nodes in the same gate), and intergate shorts (shorts between logical nodes, and shorts of an internal (electrical) node with a logical node, belonging to different gates). The class of shorts between two internal nodes of different gates is not included due to its low likelihood. The I_{DDQ} lower bound distribution for a given defective circuit and a particular input vector, together with the I_{off} leakage distribution, is needed for the determination of the I_{DDQ} threshold values to perform the test of the circuit, adapting the threshold value to the test vector applied.

The organization of this paper is as follows. In the next section, the quiescent current consumption of the defective domain for a FCMOS circuit with a bridge is evaluated. In the third section, the saturation cur-

rent versus the transistor effective length for individual MOSFETs are presented assuming high performance circuit scaling as well as low power scaling up to 0.2 μm. In the fourth section, the I_{DDQ} lower bounds for a general FCMOS circuit, considering intragate as well as intergate bridges affecting FCMOS gates are evaluated. Finally, conclusions are presented.

2 I_{DDQ} consumption of the defective CMOS circuit with a short

In a CMOS combinational circuit affected by a bridging defect, two contributions to the abnormally high I_{DDQ} consumption are identifiable. The first one is the current flowing from V_{DD} to GND and passing through the bridging defect. The transistors involved in the generation of this current are said to compose the defect subdomain. The second contribution to the defective quiescent current consumption comes from the stages fed by the signals coming from the defect subdomain. Although this part of the circuit is defect-free, the intermediate voltages of some of its inputs may generate an abnormally high current consumption. This second subcircuit is named the penetration subdomain. In the next subsections, the lower bounds of both contributions are characterized.

2.1 I_{DDQ} consumption of the defect subdomain

The current consumed by the defect subdomain in a CMOS circuit with a bridge is calculated in this subsection. To characterize the quiescent current supplied from V_{DD} to ground through the bridging defect, I_B, we are considering the electrical circuit composed by V_{DD}, pull-up network, short, pull-down network and ground. To illustrate the methodology, let us consider the bridging defect of a logical output node with an internal node of two different gates (Figure 1 a)). Two possible excitations of the defect are possible: 1) I_B flowing from V_{DD1} to ground in Gate2 and 2) I_B flowing from V_{DD2} through Gate1 to ground. If the pulling-up network crossed by I_B is replaced in the analysis by an equivalent pMOS transistor and, similarly, the pulling-down network is replaced by its equivalent nMOS transistor as proposed in [8], Figure 1 b) illustrates the resulting circuits. The resistance assumed for the bridging connection is zero. In spite of the resistances measured in [9] on the order of KΩ, the higher percentage of bridges presented resistances near zero Ω.

The quiescent current consumption of the defective circuit should be calculated as the intersection point of the $I_{DS}-V_{DS}$ characteristic curves of both transistors, nMOS$_{eq}$ and pMOS$_{eq}$, as shown on Figure 2 a). In order to manage easily the expressions leading to the I_B

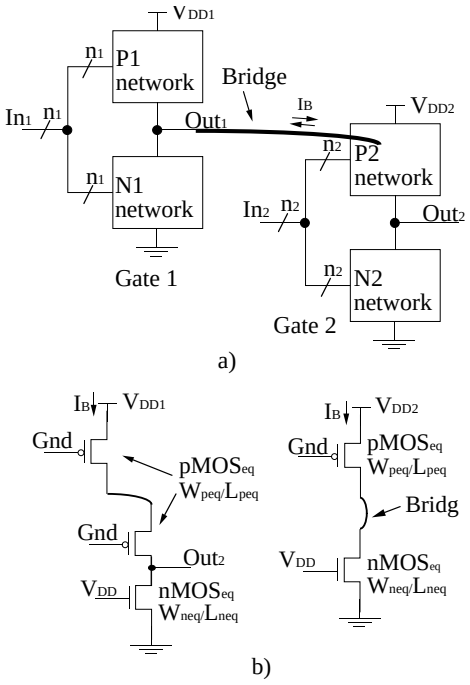

Figure 1: *a) A bridge connecting the output of two CMOS gates and, b) the equivalent circuit*

resolution, an upper and lower limit value will be calculated. Let us assume the curves to be intersected as shown in Figure 2 b). The quiescent point to be determined is named B on the figure. Obviously, point C is an upper bound for B and I_C=min$\{I_{Dsatn}, I_{Dsatp}\}$. The lower bound of current B can be found as the A point (see Figure b)). To obtain point A, three lines have been used to approximate each one of the two $I_{DS}-V_{DS}$ characteristic curves. For the nMOS transistor, the first line underestimates I_{DSn} and goes, in the (V_{DS}, I_{DS}) axes, from (0,0) to ($V_{DD}/2$, I_{Mn}), where the I_{Mn} is the current of the nMOS transistor for $V_{DS}=V_{DD}/2$; the second one, underestimating I_{DSn} too, goes from ($V_{DD}/2$, I_{Mn}) to (V_{DD}-V_{Tn}, I_{Dsatn}); and the third one, characterizes the saturation region, going from (V_{DD}-V_{Tn}, I_{Dsatn}) to (V_{DD}, I_{Dsatn}). A set of three equivalent lines have been used to approximate the I_{DSp} current. The I_B values can be bounded with the knowledge of $I_A \leq I_B \leq I_C$.

A trade-off between accuracy and time has been considered. The calculated bounds are quite an accurate way to find I_B avoiding the resolution of more complex equations analizing the estimation of I_{DDQ} in large circuits without the need of electrical (SPICE like) simulators.

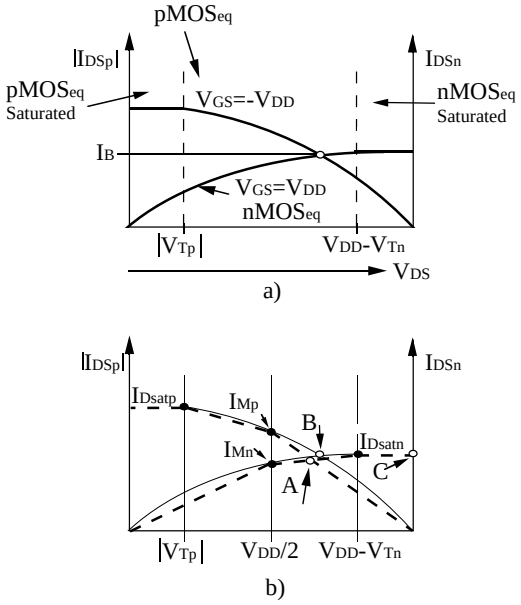

Figure 2: *Current consumption of the defective circuit*

2.2 I_{DDQ} consumption of the penetration subdomain

The number of defect free stages with elevated I_{DDQ} consumption due to intermediate voltage values, has been shown to be small [10], typically on the order of 1 to 3 stages, but with a significant likelihood of being 1. In this work, only one level of penetration is considered.

Each one of the gates belonging to the penetration subdomain can be modeled as one (n or p) network of series transistors connected to another (p or n) network of parallel transistors. For the considered technology, one network is composed by 1 to 4 transistors. Due to the erroneous intermediate voltage, at least one of the inputs of these gates has the analog value. The worst (lower) case for the I_{DDQ} consumption is the intermediate input entering the transistor of the series network placed the nearest to the output node. As an example, in Figure 3 a) one nand gate of 3 inputs is illustrated. The transistors of the series network with logic gate voltages, are modeled as a resistance derived from their correct V_{GS} value. For the particular case where all the transistors in the series network have intermediate voltages at their inputs, an equivalent channel width/length is calculated. The I_{DDQ} consumed is found by means of the saturation characteristics of both n and p networks. In Figure 3 b), the proposed methodology is compared with HSPICE results for MIETEC0.5 technology for a typical case (NAND with 3 inputs).

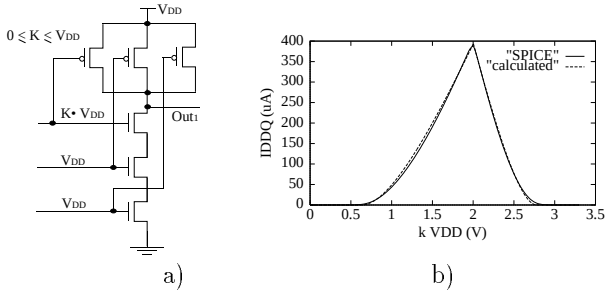

Figure 3: *Current consumption of the defective circuit*

3 Saturation drain current (I_{Dsat}) vs. transistor effective length (L_{eff}) for a deep submicron MOSFET

In this section, the saturation current I_{Dsat} versus L_{eff} is evaluated according to the expected scaling trends. The quadratic model for I_{Dsat} has been shown to be inadequate for today's MOSFET's due to the effects of mobility degradation caused by the vertical channel field, velocity saturation, short-channel effect or V_t "roll-off" and source and series resistance of LDD structures. A model for the saturation current of a MOS transistor with zero source/drain series resistance I_{Dsato}, in terms of the transistor dimensions and its gate-source voltage V_{GS}, and the threshold voltage V_{TH} [11] gives:

$$I_{Dsato} = W \cdot v_{sat} \cdot C_{ox} \frac{(V_{GS} - V_{TH})^2}{V_{GS} - V_{TH} + E_{sat} \cdot L_{eff}} \qquad (1)$$

where W is the MOSFET channel width, C_{ox} is the gate oxide capacitance per unit area and $E_{sat} = \frac{2v_{sat}}{\mu_{eff}}$ is the electric field corresponding to velocity saturation v_{sat}. Also, the electron mobility (μ_{eff})degradation with the strong efective field, E_{eff} or small oxide thickness, T_{ox}, is considered.

For LDD structures, the effect of the source/drain series resistances have to be considered . The approximation for the accounting of the series resistance at the source end, R_s, leads to the approximate expression for I_{Dsat} [11]:

$$I_{Dsat}(R_s) =$$

$$I_{Dsato} \cdot (1 - \frac{2 \cdot I_{Dsato} \cdot R_s}{V_{GS} - V_{TH}} + \frac{I_{Dsato} \cdot R_s}{V_{GS} - V_{TH} + E_{sat} \cdot L_{eff}}) \quad (2)$$

where $I_{Dsato} = I_{Dsat}(R_s = 0)$ is found by the expression (1). These expressions have been validated experimentally up to $L_{eff} = 0.2$ μm as reported by Chen et al. in [11].

It can be easily demonstrated that expression (1) is the upper limit of the I_{Dsat} of the circuit, for LDD structures, since zero series resistance at the source/drain ends is assumed. The lower I_{Dsat} limit is given by the equation(2) provided that no reduction of V_{TH} is assumed and R_s is taken into account. Both expressions, the upper and the lower limits, will be considered later in this work.

To characterize the relative evolution of the saturation current of MOSFETs transistors with the scaling trends, the I_{Dsat} value vs. L_{eff} is calculated. In Figure 4, the approximation used to model the V_{DD} vs. L_{eff} and the T_{ox} vs. L_{eff} dependences for both high performance and low power approaches according to [12] are modeled. The T_{ox} vs. L_{eff} dependence is considered equal for both scenarios. With these scaling considerations, the upper and lower saturation current boundaries of an nMOS transistor ($W = 10L_{eff}$) dependence on L_{eff} are shown in Figure 5. The presentation of the resulting current in the Figure is normalized to the I_{Dsat} for L_{eff}=0.7 μm. L_{eff} is considered within a range going from 0.7 μm to 0.2 μm. For each L_{eff} value, the scaled V_{DD}, T_{ox} and μ_{eff} are calculated according to the trends in CMOS scaling considered.

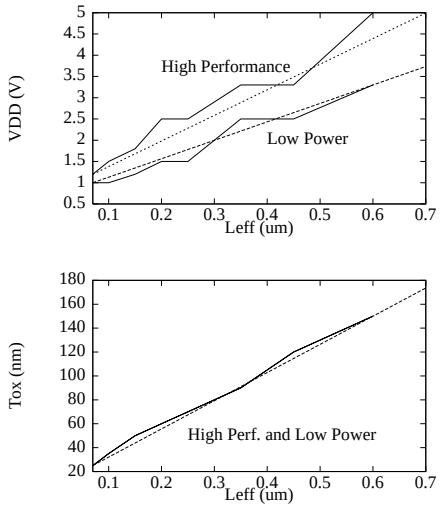

Figure 4: *V_{DD} vs. L_{eff} and T_{ox} vs. L_{eff} dependences for high performance and low power scenarios. With solid lines the scaling trends presented in [DAV95] are illustrated; with dashed lines, the approximate straight lines used in this work*

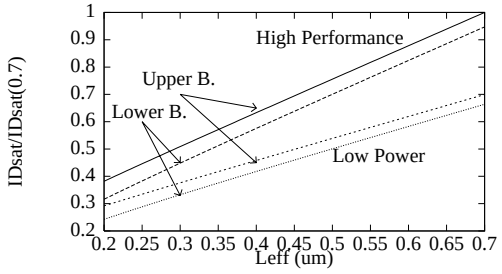

Figure 5: *I_{Dsat}vs.L_{eff} dependence for high performance and low power scenarios*

Observing the upper bound of $I_{DsatNORM}$ for high performance circuits, a decrease in L_{eff} from 0.7 to 0.2 μm (a factor of 3.5) causes a decrement of a factor 2.6 in the saturation current. For low power scaling scenario, it decreases less and, for the case considered, it gives an approximate reduction of 2.4. The effect of the drain/source series resistance makes the lower bound decrease in a larger factor, approximately between 3.0 and 2.7, respectively.

4 I_{DDQ} estimation of the defect domain in deep-submicron CMOS circuits

Once known the I_{Dsat} limits for MOS transistors, let us consider a general FCMOS circuit with a short connecting any pair of nodes, at least one of them being a logic node (the internal-internal class of bridges are excluded because their low likelihood). A standard cell library, MIETEC 0.5 μm MTC35000 library, with a maximum of 4 input gates, has been considered. The n and p networks present in the library gates are series and parallel networks of 1 to 4, n or p MOSFETs. The unitary nMOS transistor has W_{nu} width and, similarly, the unitary pMOSFET has W_{pu}=$K_u W_{nu}$ to equilibrate their strengths. For the parallel networks, the transistors have the unitary size. Two transistors in series have doubled unitary width, three transistors in series have 2.5 multiplied unitary widths and four transistors in series have tripled unitary widths. These size ratios have been taken from the considered library. For other libraries a similar approach would be followed.

For any of the inter and intragate considered, an equivalent circuit like shown in Figure 1 b) is obtained. To start with, let us consider shorts affecting only logic nodes as it is shown in Figure 6. Without a loss of generality, we assume the excitation of the short with (out1, out2) = (V_{DD}, 0), and the p network therefore equals three pMOSFETs in series and the n network equals two nMOSFETs in parallel, for this illustrative example (W_{peq}=(2.5/3)$K_u W_{nu}$ and $W_{neq} = 2\ W_{nu}$). Now, bounds on I_B can be obtained since the strength ratio between p and n networks are known. All the possibilities for the considered library are summerized in a table.

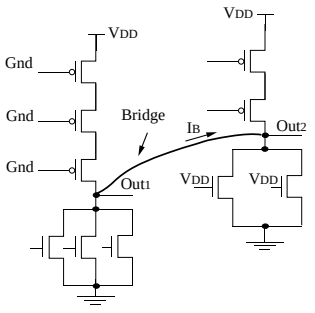

Figure 6: *Illustrative example of intergate short*

Once the table of strengths is obtained, the methodology indicated above (in Figure 2) to estimate the quiescent current of the defect subdomain is applied. I_{DDQ}

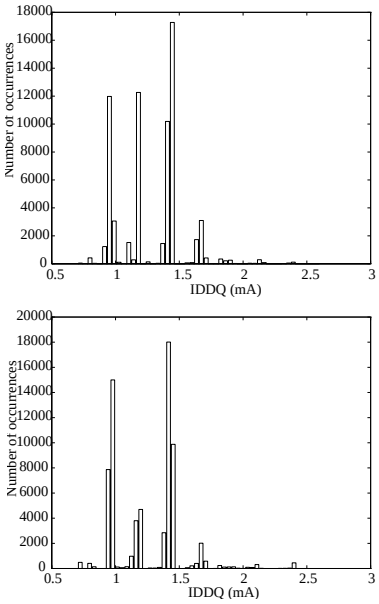

Figure 7: *Histogram of the intergate shorts I_{DDQ} (C880 ISCAS)*

values are easily obtained leading to the lower I_B bounds as shown in expression (1).

The I_{DDQ} contribution of the stages driven by the defective nodes is also included in the estimation. For the gates of the penetration subdomain, the n as well as the p networks are known and the saturation currents are directly calculated as previously indicated to obtain the lower bounds of the penetration current.

As an illustration of the methodology, in Figure 7 the I_{DDQ} distribution of the lower bound is shown, for all possible shorts, of the C880 ISCAS85 circuit for two different I_{DDQ} test vectors. In the defect subdomain, an average deviation of 1% has been found for current values and 5% for voltage values (comparing with SPICE results). The I_{DDQ} errors in the penetration subdomain have been lower than 8 %.

Once this distribution is found, depending on the I_{off} expected distribution [13], the I_{DDQ} threshold value can be settled. This value is a tradeoff between the escape rate and the yield loss accepted for the process.

5 Conclusions

The quiescent current of a FCMOS circuit caused by a short in submicron technologies has been estimated. The technology scaling including geometry reduction of L_{eff}, W, T_{ox} as well as V_{DD} lowering, carrier mobility degradation and velocity saturation is included in the model. Scaling trends in "High Performance" (low V_{TH}) circuits and in Low Power (high V_{TH}) circuits have been studied. A methodology to evaluate the lower bound of defective I_{DDQ} currents in the C.U.T. has been presented. The lower bound of the defective I_{DDQ} due to frequent shorts in a FCMOS library has been obtained and its reduction with scaling, evaluated. Comparing with 0.7 μm technologies, reductions of defective I_{DDQ} currents on the range of 2.4-3.0 have been found for L_{eff} reductions on the order of 3.5. As an application example for a commercial 0.5 micron technology, the distribution of the I_{DDQ} lower bound has been obtained for an ISCAS circuit and two particular I_{DDQ} test vectors. The defective I_{DDQ} lower bound distribution, together with the non-defective I_{DDQ} distribution, leads to the determination of vector dependent threshold I_{DDQ} values to enhance the test efficiency.

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