Next Generation System Level Design Tools

Wolfgang Rosenstiel

University of Tübingen, Sand 13, D-72076 Tübingen, Germany

Panel 6A

Next Generation System Level Design Tools

February 25, 1998
14.30-16.00 (Room A)

Organisers:
Wolfgang Rosenstiel, University of Tübingen, Germany and
Joachim Kunkel, Synopsys, USA

Moderator:
Joachim Kunkel, Synopsys, USA

Panelists:
Misha Burich, Cadence/Alta, USA
Raul Camposano, Synopsys, USA
Mark Genoe, Alcatel, Belgium
Lev Markov, Mentor Graphics, USA
Steve Schulz, Texas Instruments, USA

This panel discusses the requirements for the next generation system design tools and presents the latest developments from the industrial leaders. Attendees are representatives from system houses as well as from the electronic system design automation companies.

The panel is chaired by Joachim Kunkel, Director Engineering for System Level Design Tools at Synopsys.

The electronic system design companies are represented by Misha Burich, VP Engineering from the Alta Group of Cadence, Raul Camposano, Senior VP and General Manager for the Design Tools Group of Synopsys and Lev Markov, Chief Scientist for system level co-design of Mentor Graphics.

Marc Genoe, Chairman of the System Level Design and Verification Working Group of the Virtual Socket Interface Alliance will discuss the standardization process with respect of system level design.

Steve Schulz, Texas Instruments, the initiator of the System Level Design Language initiative, will present the status of this recent development. In addition, system house representatives will discuss future requirements for system level design tools.