

Formal Verification: A New Standard CAD Tool for the Industrial Design Flow

Wolfgang Rosenstiel

University of Tübingen, Sand 13, D-72076 Tübingen, Germany

Panel Session 5A

Formal Verification: A New Standard CAD Tool for the Industrial Design Flow

25 February 1998

11.00 - 12.30 (Room A)

Organisers:

*Wolfgang Rosenstiel, University of Tübingen, Germany and
Gerry Musgrave, Brunel University, GB*

Moderator:

Gerry Musgrave, Brunel University, GB

Panelists:

Dominique Borrione, TIMA-UJF, France

Antun Domic, Synopsys, USA

Ramayya Kumar, Verysys, Germany

Alan Page, Abstract Design Automation, GB

Michael Payer, Siemens, Germany

Formal verification has been the province of academic research for many years. More recently tools have become available from vendors to tackle some aspects of the design verification problems. There have been considerable learning scenarios in order to understand how this technique can fit in the real industrial design flow. The Panel, consisting of academics, vendors and users, will endeavour to clarify what these tools can do, what their potential will be and the experiences to date in helping validate today's complex designs.