Sigma-Delta Testability for Pipeline A/D Converters

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***Abstract*—Pipeline Analog to Digital Converters (ADCs) are widely used in applications that require medium to high resolution at high acquisition speed. Despite of their quite simple working principles, they usually form rather complex mixed-signal blocks, particularly if digital correction and calibration are considered. As a result, pipeline converters are difficult to test and diagnose. In this paper, we propose to reconfigure the internal Multiplying DACs (MDACs) that perform residue amplifications as integrators, each one with an analog and a digital input. In this way, we can reuse consecutive pipeline stages to form $\Sigma\Delta$ modulators, with very reduced area overhead. We thus get an on-chip DC (low-frequency) probe with a digital 1-bit output that does not require any extra pin. In addition, digital test techniques developed for $\Sigma\Delta$ modulators may be used to enhance the diagnosing capabilities. An industrial 1.8V 15-bit 100Msps pipeline ADC that had previously been fully validated in a $0.18\mu m$ CMOS process is used as a case of study for the introduction of the DfT modifications.**

I. Introduction

Analog-to-Digital Converter (ADC) can be considered as one of the main blocks in a lot of systems, since they are mandatory to make the link between the analog outside world and the evermore ubiquitous digital computer world. Among the many available architectures, pipeline ADC is one of the best candidates for high-speed, medium-resolution applications: typically higher than 10 bits at a few hundred MHz. However, for resolutions above 11 effective bits, digital calibration is usually required and the complexity of pipeline converter design can reach high levels, giving rise to mixed-signal blocks in the range of a few mm^2 (depending on the technology node).

This hardware complexity is obviously a limiting factor to the test and diagnosis of these converters. For instance, if poor performance is observed, it may be difficult to determine if the digital calibration process is failing or if the building blocks are out of calibration range. Identifying different sources of performance limitations in the analog building blocks (static, dynamic, random noise, etc.) is a challenging task in these high-accuracy applications, where the resolution is typically bounded by thermal noise.

Relatively few pipeline-specific Design-for-Testability (DfT) schemes have been proposed in the past. For instance, the pipeline converter in [1] is reconfigured as a chain of A/D - D/A converters and simple DC stimuli are used to detect the faults. The same authors also propose an online testing scheme [2]. In [3], the digital correction is partially disabled to check for design guard-bands.

What we propose in this paper is to introduce DfT modifications in the pipeline structure so that consecutive stages can be reconfigured as $\Sigma\Delta$ modulators. The main interest is that the modulator structure is relatively simple and robust. It definitely does not have the same performance sensitivity as the pipeline in terms of branch coefficient accuracy and linearity. It also provides a significant improvement in thermal noise, since the contributors located farther than the first integrator in the loop are shaped to high frequencies. The approach can be double: on one hand we can obtain a robust DC probe with a single bit digital output directly available for off-chip processing, and on the other hand we can also see it as a divide and conquer approach to the pipeline building blocks if digital test techniques are used to evaluate the performance of the re-configured $\Sigma\Delta$ modulators [4]–[7].

The observation that pipeline stages can be re-used with little overhead to build a $\Sigma\Delta$ modulator is not new [8]. In that paper, the authors presented a reconfigurable converter that can be either a pipeline or a $\Sigma\Delta$ converter depending on the specification requirements. Consequently, the reconfigurability was contemplated as part of the design, and did not aim at testability. In this work we take a different approach and propose to introduce the necessary DfT modifications to an existing architecture from an industrial project with minimum modification on the switching sheme/schedule, without affecting the critical analog blocks and with negligible performance impact. We believe that this should be more attractive for the industry, since enhanced testability features are hardly considered by designers at early stages of the architectural design.

The paper is organized as follows. Section II discusses the pipeline and $\Sigma\Delta$ architecture and presents the required DfT modifications. In Section III we introduce the practical implementation of the scheme on a pipeline prototype, showing how can the $\Sigma\Delta$ modulator improve testability and diagnosis, validating the concept by transistor-level simulations. Finally, Section IV summarizes the conclusions of the paper.

II. Architectural description

A. Generic Pipeline

Pipeline ADCs actually perform a recursive algorithmic division of the input sample by the Least Significant Bit (LSB) value. The first stage in the pipeline (following the Sample

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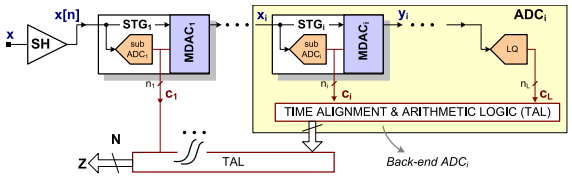

Fig. 1. Simplified block diagram of a L-stage pipeline ADC with details on the stage topology and the time alignment and correction logic (TAL).

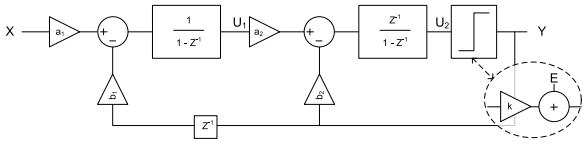

Fig. 2. Generic Cascade of Integrators with distributed Feedback 2^{nd} order single-bit $\Sigma\Delta$ modulator

and Hold), performs a coarse A/D conversion of the input sample ($x\,[n]$), computes the residue and amplifies it such that the next stage can process it. This second stage performs the same operation on the residue and sends the amplified error signal to the next stage, and so on. In the end, an appropriated combination of the digital sub-codes from all the stages forms the output word (Z) of the pipeline ADC.

Fig.1 shows a simplified diagram of a pipeline ADC. A stage (STG) is composed by a sub-ADC (usually a FLASH ADC) that performs the coarse conversion (c), a sub-DAC that will generate the coarsely approximated signal and an error amplifier that will subtract the approximation from the input and amplify the error to generate the amplified residue (y). In practice, the DAC and the error amplifier are implemented in a single block then called Multiplying-DAC (MDAC).

If all operations were ideal, the gain of the residue amplifier could be set such that the coarse quantizer error is amplified to the full-scale defined by the converter reference (R).

In practice, the unavoidable non-idealities of the sub-ADC – due to the offsets of their comparators – make this approach unfeasible, since it would possibly bring some stage in over-range. In order to avoid this limitation, unitary redundancy is introduced [9]: the gain of the residue amplifier is halved with respect to its theoretical ideal value. The LSB of stage i is redundant with the MSB of stage $i+1$ and the final word is accordingly obtained by a weighted addition of the sub-codes with 1-bit overlap. The practical depth of the pipeline is only limited by the amount of noise in the signal (the input noise plus the noise added by each stage).

In order to reach the highest resolutions, other non-idealities that are not handled by the redundancy have to be corrected. This is achieved by means of digital calibration [10]–[13]. Entering into the details of this process is out of the scope of this paper, but roughly speaking the idea consists in measuring the errors in the MDACs (including gain errors), using the own back-end ADC (constituted by the least significant stages to the specific one under calibration) as measurement instrument, and updating accordingly the associated stage sub-code in a Look-Up Table (LUT).

B. Building a $\Sigma\Delta$ modulator

We have seen in the previous subsection that a pipeline stage is made of a FLASH sub-ADC and a multiplying DAC, which is nothing else than a subtracting amplifier with an analog input and a digital input. Let us consider closely the block diagram of a Cascade of Integrators with distributed FeedBack modulator (CIFB), as defined in [14] and depicted in Fig.2.

Each integrator is preceded by a summing node with an analog input and a digital input fed by the modulator output bitstream. This structure resembles strikingly that of the pipeline converter MDAC. We just have to convert the amplifier into an integrator and modify some weights of the different branches. So in order to build a $\Sigma\Delta$ modulator, we could use the MDAC of consecutive stages plus the sub-ADC of the next stage which would perform as the quantizer of the modulator.

The design of a particular $\Sigma\Delta$ modulator is a cumbersome task and so might be the reconfiguration of the pipeline, especially if all the possibilities are contemplated. However, we decided to restrict our research – at least in a first approach– to a simple structure.

Multibit modulators can achieve higher Signal-to-Noise Ratio (SNR) for the same oversampling ratio (OSR) as their single-bit counterparts and are less susceptible to spurious tones and limit cycles. Multibit sub-ADCs are present in the pipeline, as well as the corresponding DACs of the MDACs, so it seems to be a feasible choice at first hand. However, these multibit modulators also require dynamic element matching to get the proper linearity in the feedback DAC, which would introduce significant complexity in the design. We thus decided to limit our design to single-bit modulators whose architecture is inherently linear in most of the input range. This is easily done by using only the MSB of the sub-ADC as the modulator output.

Similarly, the higher the modulator order, the higher the resolution for a given OSR. However, single-loop modulators of order higher than two are only conditionally stable, which is clearly not desirable for our testability purpose. Indeed, we want our test instrument to be more robust (or at least as robust) as the pipeline ADC.

So let us consider the design of 2^{nd} order single bit. As shown in Fig.2, the 1-bit quantizer can be linearized as a gain element (k) and an additive white noise E whose standard deviation is known to be equal to,

$$\sigma_E^2 = \Delta^2/12 \tag{1}$$

In a first approximation the gain settles to the value that minimizes the noise power, which can be shown to be [15],

$$k = E\left(|U_2|\right)/E\left(U_2^2\right) \tag{2}$$

where U_2 is the second integrator output. This value can easily be computed thanks to high-level simulations.

TABLE I
PERFORMANCE OF 2^{nd} ORDER CIFB $\Sigma\Delta$ MODULATOR

a_1	$1/2$	$1/4$	$1/4$
b_1	$1/2$	$1/4$	$1/4$
a_2	$1/2$	$1/2$	$1/4$
b_2	$1/2$	$1/4$	$1/4$
SNDR @ OSR=100	80dB	80dB	76dB
k	2.3	4.7	5.1
$max\left(\left\|U_1\right\|\right)$	1.5	0.74	0.9
$max\left(\left\|U_2\right\|\right)$	1.3	0.63	0.37

The linearized transfer function can be written as follows,

$$\begin{aligned} Y &= STF\left(z\right)X + NTF\left(z\right)E \\ &= \frac{ka_1a_2z^{-1}X + \left(1-z^{-1}\right)^2 E}{D\left(z\right)} \\ D\left(z\right) &= 1 + z^{-1}\left(-2 + kb_2\right) + z^{-2}\left(1 + ka_2b_1 - kb_2\right) \end{aligned} \tag{3}$$

The limit of the denominator in DC is

$$\lim_{z\to 1} D\left(z\right) = ka_2b_1 \tag{4}$$

So the behavior of the modulator Signal Transfer Function (STF) in DC is independent of the exact value of the quantizer gain and we have,

$$E\left(Y\right) = \frac{a_1}{b_1}E\left(X\right) \tag{5}$$

If the input branch coefficient is equal to the feedback coefficient, the DC transfer function is always 1.

On the other hand, there is a double zero at DC for the Noise Transfer Function (NTF), but we can see that the noise density gain will be affected by the actual coefficient values through (4). An optimal set of coefficients should minimize noise density, but we shall also take into account the practical realization, which involves the feasibility of capacitor ratios and the excursion of the integrator output. Since we want to re-use the pipeline ADC blocks, it seems better to concentrate on binary fractions which imply less DfT modifications. Table I shows the results of three different configurations. The first column corresponds to the structure in [16], the second one corresponds to a scaled version and the third one is a sub-optimum structure for which all the coefficients are set to $1/4$.

It can be seen that the modulator with all the coefficients set at $1/4$ achieves less SNDR. Indeed, the increase of the quantization noise density expected from (4) corresponds to $3.9dB$ which is what is observed approximately. Because of this worse noise performance, we decided to opt for the scaled Boser architecture (i.e the second column in table I). For this architecture, the output of the two integrators is maintained at low level and will not be subject to output range issues.

C. Design-for-Testability modifications

Figure 3-a) shows the schematic of a switched-capacitor MDAC in the most used flip-around configuration with thermometer capacitor array based on [9]. During phase ϕ_1 the input signal is sampled on both capacitors C_1 and C_2. Meanwhile, the amplifier is reset to get rid of the charge stored

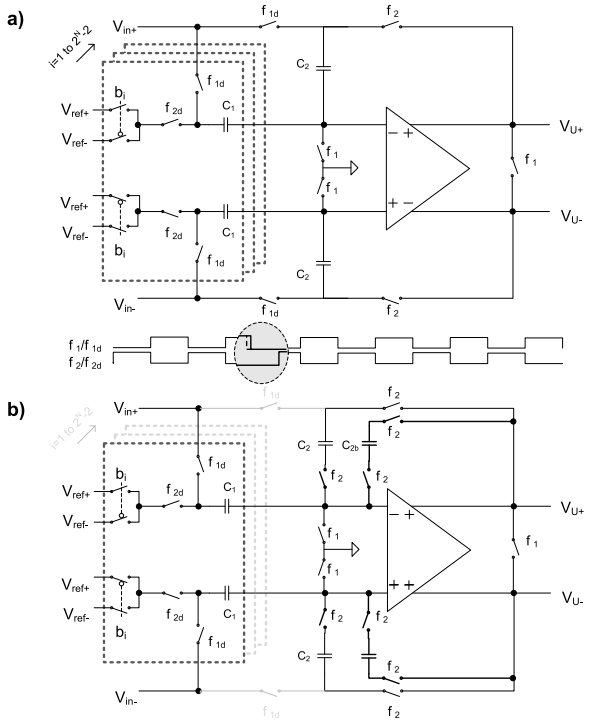

Fig. 3. a) Schematic of a multiplying DAC in a flip around configuration; b) Schematic of the integrator reconfiguration

on the parasitic input capacitor. During phase ϕ_2 capacitor C_2 is used as a feedback capacitor and capacitor C_1 is connected to the negative or positive reference voltage, depending on the DAC input word. Notice that the dotted rectangles stand for the multiplicity of capacitor C_1. The number of bits of pipeline stages is usually low, so both the sud-ADC and DAC can use thermometric coding.

If the pipeline implements a 1-bit interstage redundancy (which definitely is the most common situation) and a thermometric codification, we have that for this topology,

$$C_2 = 2 \times C_1 \tag{6}$$

whatever the number of bits of the stage.

The first DfT modification consists in converting the amplifier into an integrator. This implies that capacitor C_2 must not be reset. In $\Sigma\Delta$ mode, the switch that normally connects C_2 to the input voltage during ϕ_{1d} must be left open. Since the amplifier is reset during ϕ_1, an extra switch should be introduced between capacitor C_2 and the amplifier virtual ground. With these simple modifications, and by enabling only one of the thermometric input branches (the switches of the remaining branches are left open) we obtain an integrator of gain $1/2$. In order to obtain a gain of $1/4$, we can either divide and scale an input branch in two identical parts (that would be controlled by the same bit in pipeline mode) or implement an extra capacitor C_{2b} in parallel with C_2 that would be active only in $\Sigma\Delta$ mode. These modifications are sketched in fig.3-b).

For the second stage of the proposed $\Sigma\Delta$ modulator, we

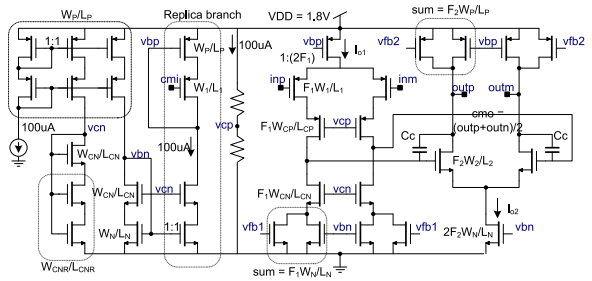

Fig. 4. Two-stage operational amplifier (op-amp) with Miller compensation and details on the biasing network.

need a different coefficient for the input path ($1/2$) than for the feedback path ($1/4$). This can be achieved by enabling another input branch that would sample the input voltage but connect to common mode during the integrating phase ϕ_2. This modification requires an extra switch to connect to common-mode.

So in summary, the proposed DfT modifications only involve simple local clock gating on some switches, the introduction of one switch per stage in the signal path and eventually an extra capacitor of the same value as C_2 and a switch to common-mode in parallel with the reference voltages. Notice that this reconfiguration can be carried out for all the stages of the pipeline. Whatever two consecutive stages can thus be considered to form a 2^{nd} order modulator. It would also be straightforward to build a 1^{st} order modulator with the last stage.

III. Experimental Validation

A. The pipeline prototype

In this section, the system level characteristics of the industrial pipeline ADC demonstrator without DFT (ADC_{noDFT}) and with DfT facilities (ADC_{DFT}) are briefly introduced.

The target specifications for the ADC_{noDFT} were 15-bit 74dB-SNDR 100Msps with a 2Vpp differential input in a 1.8V $0.18\mu m$ CMOS process. The architecture featured the following parameters:

- a front-end Sampled & Hold (SH), followed by six stages of 2.5 bits based on [9];
- a resolution of 2.5 bits for the last quantizer (LQ);
- a unique multi-stage comparator design formed by a front-end SC, a pre-amplifier and a dynamic latch for all stages and LQ;
- unitary redundancy with digital correction;
- op-amp finite gain and capacitor mismatching calibration [11] in STG_1 and STG_2 to improve linearity;
- op-amps based on the two-stage topology shown in Fig.4.

To optimize power consumption, current ratios F_1 and F_2 with respect to the bias reference (Ibias = $100\mu A$) were scaled down from the most to the least significant stages.

Once introduced the original characteristic of the demonstrator, we focus now on the DfT modifications, paying special attention to the considered design strategies to reduce the impact on the performance. With this goal in mind, we have explored several switching schemes and timing schedules concluding that optimum performance can be achieved by acting on the clock phases of the switches under reconfiguration using simple clock gating logic. This approach minimizes the capacitive load due to DfT, while has negligible impact on the available time for the sampling and amplifying operations in the SC circuits. The clock gating logic (CGL) basically consists of a single NAND or NOR gate (in some switches, a simple inverter is also required). The extra time introduced by CGL (in the order of 50-100ps) has been recovered in the critical paths by playing with the delayed phase already available in the ADC_{noDfT}, without any modification of the clock generator and clock tree. The typical delay between ADC_{noDfT} clock phases is in the order of 200ps.

Similarly to the CGL, the modifications of the reset in ADC_{noDfT} have shown negligible impact on the performance and require no significant design time (aside of the simulation time for verification, they were performed in less than 1 day). These include: a) to size the reset switch between capacitor C_2 and the amplifier virtual ground to reset the huge non-linear parasitic capacitance at the input of the op-amp; b) to adjust the Miller compensation capacitance by mean of a programmable bank of capacitors. The area overhead in STG_1 and STG_2 is estimated to be around 10% (less than 2% for the whole pipeline ADC).

B. Pipeline functional test

First of all we have to validate that the proposed DfT modifications do not impact the overall performance of the pipeline converter. As a matter of fact, performance degradation is usually considered very negatively by the industry in competitive markets struggling for the state-of-the-art. For this purpose, we perform two electrical simulations: one of the original converter prototype without any DfT modifications, and another of the modified converter with all the modifications. Obviously, these modifications are not active in normal operating mode and the two converters are identical form a high level viewpoint. However, all the extra delays related to clock gating and extra parasitics due to switches are considered in the simulation. Layout parasitics due to the extra routing are not considered but, since all the changes are local, we can assume that their impact should not dominate that of the schematic.

Fig.5 shows the power spectrum of the original modification-free converter, for an input sine-wave of almost full-scale close to Nyquist frequency. The obtained Effective Number of Bits (ENOB) is 13.2 for the simulation without transient noise and 11.5 for the worst-case simulation with transient noise and calibration averaging disabled.

Fig.6 shows the power spectrum of the pipeline converter with DfT, for the same input sine-wave. The obtained Effective Number of Bits (ENOB) is 13.7 without noise and 12 with transient noise.

Indeed, the performance of the modified converter appears slightly higher than that of the original converter. However this

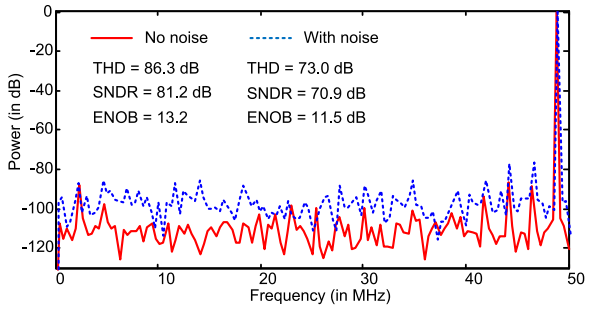

Fig. 5. Power spectrum of the original pipeline, with and without transient noise

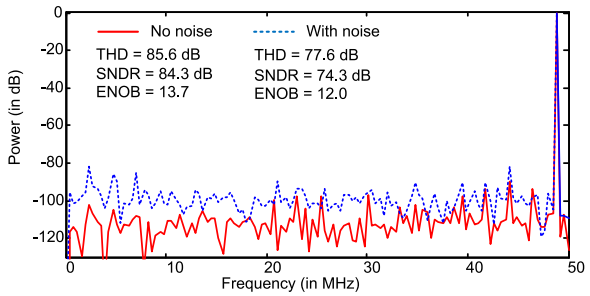

Fig. 6. Power spectrum of the DfT pipeline, with and without transient noise

is only a marginal improvement that may be due to computational approximations. To speed-up these simulations, only 256 samples have been considered in the FFT evaluation. In addition, the true calibration process is not simulated: the LUT calibration registers were evaluated with a single measurement, and therefore, they were highly affected by thermal noise. When averaging is activated, the effective resolution of the unmodified pipeline is expected to be above 12 effective bits in agreement with the targets. In any case we can safely state that the proposed modifications have no impact on performance.

The lack of performance penalty, together with the low overhead, makes the approach worth of a closer look since it can be achieved at practically no cost (excepting the non-recursive engineering cost linked to design).

C. Sigma-Delta functional tests

Once we have shown that the introduction of DfT modifications does not affect significantly the accuracy of the pipeline, we want to measure the performance of the $\Sigma\Delta$ converter. For this particular prototype, all the stages are architecturally identical (3-bit stages, with a flip-around implementation) and we thus simulate only one modulator: the one formed by the first and second stages. For this purpose, we build a test setup without the pipeline Sample and Hold, and connect the sampling capacitor of the first stage directly to the input signal. The sampling frequency is the same as for the pipeline: $f_s = 100MHz$. The input signal frequency is set to $46kHZ$ and its amplitude to 60% of full-scale. Fig.7 shows the power spectrum obtained for a simulation with transient noise. A high performance Rife-Vincent window is used to avoid any spectral leakage from the main lobe but also from the high

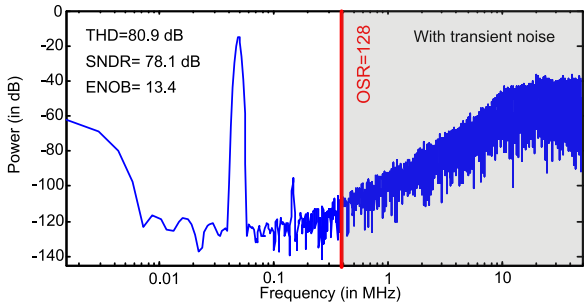

Fig. 7. Power spectrum of the $\Sigma\Delta$ modulator with transient noise

power quantization noise. In order to calculate the performance metrics, we selected an OSR of 128, but this is an arbitrary value since the bit-stream will be processed off-chip. Taking a closer look at the spectrum, we can evaluate the corner frequency at which the thermal noise begins to dominate the shaped quantization noise. This approximately occurs for an OSR of 300. Beyond this point (i.e. for higher OSR), additional filtering will only produce an improvement of half a bit per octave in the Signal to Noise Ratio (SNR).

It can be noticed that we obtain a linearity that is in line with the complete pipeline ADC with only the first two stages. Simulations for sine-waves at lower amplitudes show that the noise floor at an OSR of 128 is on a 15-bit level. Actually, with an amplitude at 40% of full-scale, a Total Harmonic Distortion of $90dB$ is reached.

We can thus conclude that the proposed DfT modifications lead to a good $\Sigma\Delta$ performance in test mode and do not degrade the pipeline performance in normal operating mode.

D. DC probe

In the previous subsection we have shown that a high linearity can be reached in the $\Sigma\Delta$ mode. Additionally, this linearity is achieved without the need of any calibration, which is not the case of the pipeline converter. Indeed, it is acknowledged that simple $\Sigma\Delta$ modulators are not sensitive to coefficient variations (i.e. capacitor mismatch) in first order. On the contrary, a Monte Carlo of the original pipeline showed that before calibration the ENOB could fall to 10.5, while it consistently remained above 12.5 after calibration. Hence, we can use this modulator as a robust DC probe to diagnose the previous stage.

E. Digital tests

In addition to the value of the $\Sigma\Delta$ modulators as a robust instrument, it is possible to re-use some techniques that have been proposed to test $\Sigma\Delta$ modulators in a fully digital manner. In [4], a digital sequence that encodes a sine-wave in a high-order $\Sigma\Delta$ bitstream is sent to the modulator through a 1-bit DAC. Actually the same DAC that is used during the feedback phase can be re-used during the sampling phase to input the test sequence. It has been demonstrated that this test is quite close to the equivalent functional test with an analog sine-wave, at least for amplitudes lower than the saturation point.

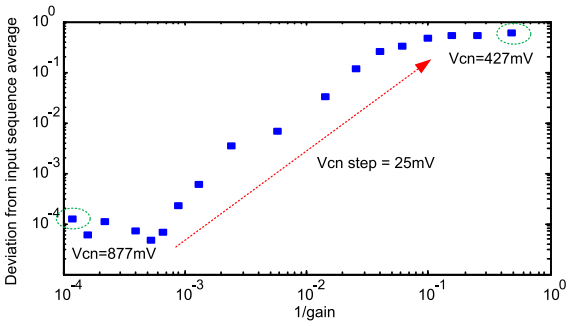

Fig. 8. Digital test results for integrator leakage.

In [5], the authors propose several digital tests using either short periodic sequences or pseudo-random sequences that can easily be programmed in a Linear Feedback Shift Register. These tests target mainly the integrator pole errors and the integrator settling errors.

The first approach is undoubtedly of interest: a poor performance of the $\Sigma\Delta$ modulator would be the sign of a defect in the pipeline block since the signal path is very similar in both configurations. The second approach shall, in turn, bring significant diagnosis information as it is possible to isolate the different amplifiers. In order to illustrate the potential of this approach, we performed the following experiment: i) Vary the bias voltage of a cascode transistor (V_{cn} in Fig.4) by $25mV$ steps. ii) Evaluate the amplifier DC gain at each step. iii) Simulate, for each step, the response of the modulator to a periodic digital sequence $[1\ 1\ 0]$ of equivalent mean value $1/3$. iv) Compute the mean value of the modulator output using a 3^{rd} order comb filter of length 100.

According to [5], [6], the deviation of the output bitstream DC component from the input sequence mean value should be inversely proportional to the gain of the amplifier in the first integrator (i.e. the amplifier in the first MDAC). Fig.8 shows a plot of this relationship with the inverse of the amplifier gain. Due to the soft errors in the cascode voltage, the amplifier DC gain changes from 6dB to 80dB approximately. On the right part of the graph, large errors begin to drive strong non-linearities (actually the amplifier almost does not amplify). On the left part of the graph, high amplifier gains are obtained and too few points have been acquired (roughly 300) to correctly discriminate the associated error. In the central part, however, the relationship is reasonably linear and in any case the correlation is patent. Therefore the proposed digital test allows diagnosing the amplifier DC gain in the MDAC. The other amplifiers may also be diagnosed by properly reconfiguring subsequent stages.

IV. Conclusions

In this paper we have conceptually shown that the stages of almost any pipeline ADC can be reconfigured to form a $\Sigma\Delta$ modulator. The practical DfT modifications have been discussed and implemented on an industrial prototype. The performance impact of these modifications is completely negligible and the associated overhead is very reduced. The obtained DfT $\Sigma\Delta$ modulator can be used as a DC probe to test the preceding stage, but smart digital test techniques can also be used to diagnose the building blocks. The preliminary test results presented in this paper are very promising, with many possible applications.

Further work will focus on the optimization of the $\Sigma\Delta$ modulator architecture to get even better performance and on the research of other potential use of the $\Sigma\Delta$ modulator, particularly for calibration. Additionally, the $\Sigma\Delta$ digital test outcomes may be used as signatures in an alternate test setup to predict the pipeline ADC performance with digital tests.

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References

[1] E. Peralias, G. Huertas, A. Rueda, and J. Huertas, "Self-testable pipelined ADC with low hardware overhead," in *IEEE VLSI Test Symposium,VTS*, 2001, pp. 272–277.

[2] E. Peralias, A. Rueda, J. Prieto, and J. Huertas, "DFT and on-line test of high-performance data converters: a practical case," in *Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, 1999, pp. 84–87.

[3] C. Mangelsdorf, S.-H. Lee, M. Martin, H. Malik, T. Fukuda, and H. Matsumoto, "Design for testability in digitally-corrected ADCs," in *IEEE International Solid-State Circuits Conference*, 1993, pp. 70–71.

[4] L. Rolindez, S. Mir, J.-L. Carbonero, D. Goguet, and N. Chouba, "A stereo audio $\sigma\delta$ ADC architecture with embedded SNDR self-test," in *IEEE International Test Conference*, 2007, pp. 1–10.

[5] G. Leger and A. Rueda, "Low-cost digital detection of parametric faults in cascaded $\sigma\delta$ modulators," *IEEE Transactions on Circuits and Systems I*, vol. 56, no. 7, pp. 1326–1338, 2009.

[6] ——, "Digital test for the extraction of integrator leakage in first- and second-order sigma-delta modulators," *IEE Proceedings - Circuits, Devices and Systems*, vol. 151, no. 4, p. 349358, 2004.

[7] C.-K. Ong, K.-T. Cheng, and L.-C. Wang, "A new sigma-delta modulator architecture for testing using digital stimulus," *IEEE Transactions on Circuits and Systems I*, vol. 51, no. 1, pp. 206–213, 2004.

[8] K. Gulati and H.-S. Lee, "A low-power reconfigurable analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1900–1911, 2001.

[9] S. Lewis, H. Fetterman, J. Gross, G.F., R. Ramachandran, and T. R. Viswanathan, "A 10-b 20-msample/s analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, 1992.

[10] S.-H. Lee and B.-S. Song, "Digital-domain calibration of multistep analog-to-digital converters," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1679–1688, 1992.

[11] A. Karanicolas, H.-S. Lee, and K. Barcrania, "A 15-b 1-msample/s digitally self-calibrated pipeline ADC," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, 1993.

[12] A. J. Gines, E. J. Peralias, and A. Rueda, "New swapping technique for background calibration of capacitor mismatch and amplifier finite DC-gain in pipeline ADCs," *Analog Integrated Circuits and Signal Processing*, vol. 57, no. 1-2, pp. 57–68, Nov. 2008.

[13] A. Gines, E. Peralias, and A. Rueda, "A survey on digital background calibration of ADCs," in *European Conference on Circuit Theory and Design, ECCTD*, 2009, pp. 101–104.

[14] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters*. IEEE press, 1997.

[15] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Wiley, Nov. 2004.

[16] B. Boser and B. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1298–1308, 1988.