Impact of Steep-Slope Transistors on Non-Von Neumann Architectures: CNN Case Study

Indranil Palit*, Behnam Sedighi*, András Horváth†, X. Sharon Hu*, Joseph Nahas*, and Michael Niemier*
*Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, IN 46556, USA
†Faculty of Information Technology, Pázmány Péter Catholic University, Budapest, Hungary
*{ipalit, bsedighi, shu, jnahas, mniemier}@nd.edu, †horvath.andras@itk.ppke.hu

***Abstract*—A Cellular Neural Network (CNN) is a highly-parallel, analog processor that can significantly outperform von Neumann architectures for certain classes of problems. Here, we show how emerging, beyond-CMOS devices could help to further enhance the capabilities of CNNs, particularly for solving problems with non-binary outputs. We show how CNNs based on devices such as graphene transistors – with multiple steep current growth regions separated by negative differential resistance (NDR) in their I-V characteristics – could be used to recognize multiple patterns simultaneously. (This would require multiple steps given a conventional, binary CNN.) Also, we demonstrate how tunneling field effect transistors (TFETs) can be used to form circuits capable of performing similar tasks. With this approach, more "exotic" device I-V characteristics are not required – which should be an asset when considering issues such as cell-to-cell mismatch, etc. As a case study, we present a CNN-cell design that employs TFET-based circuitry to realize ternary outputs. We then illustrate how this hardware could be employed to efficiently solve a tactile sensing problem. The total number of computation steps as well as the required hardware could be reduced significantly when compared to an approach based on a conventional CNN.**

I. Introduction

Historically, most information processing hardware essentially implements a von Neumann (i.e., stored program) architecture which is based on Boolean logic, and operates at discrete time on discrete, binary coded data. This paradigm has obviously and deservedly continued to enjoy exponential growth due to Moore's Law scaling. However, issues such as device-to-device variation, power density requirements, limited parallelism in many applications, etc. could all impact future scalability of this approach [1]. To continue performance scaling trends associated with Moore's Law, solutions are sought at both the device and architectural levels. In this paper we explore the possibilities of utilizing emerging devices to process information with non-binary/non-von Neumann Cellular Neural Networks (CNNs).

A CNN is a powerful analog array processor *architecture* [2], [3]. Previous efforts suggest that for computation-intensive information processing applications, such as image processing, pattern recognition, etc. (e.g., [4]–[8]), CNNs can significantly improve both power and performance. In a CNN, the interconnections between the processing units – called cells – are local, and space-invariant, which makes CNNs very suitable for VLSI implementation. The continuous-time processing of analog signals in a highly concurrent manner by the cells allows for massive real-time, fast signal processing with low energy dissipation. Previous research efforts have considered using non-linear devices, including Resonant Tunneling Diodes (RTD), Tunneling Field Effect Transistors (TFET), etc. to improve various aspects of the conventional CNN (e.g., [9], [10], [11]), and results suggest that positive impacts on power, performance, and area are indeed possible. However, the functionality of a CNN is demonstrated in the context of binary classifications only. More specifically, while RTD-based CNNs exhibit multiple equilibrium points [9], [12], device realizations have been challenging in practice [13].

In this work, we show how devices such as graphene transistors [14] – with multiple steep current growth regions separated by negative differential resistance (NDR) in their I-V characteristics – could be used successfully in CNN architectures to solve quaternary classification problems. Alternative solution through a binary CNN requires multiple iterations – costing longer time and higher energy. Also, while "single device solutions" (e.g., via graphene transistors) for multi-valued problems are obviously attractive, it should also be noted that the likelihood of device-to-device, etc. mismatch would likely increase, which would in turn result in varying cell-to-cell behavior. Given this, we have designed TFET-based circuits that exhibit useful properties (for multi-valued problems) in their output transfer characteristics.

To determine the utility of these approaches, as a case study, we consider a tactile sensing problem from [15] where the goal is to detect and identify slippage of an object from a robotic arm. Architectural level simulations for this problem demonstrate that TFET circuit-based CNNs are capable of efficiently solving ternary classification problems. When compared to the conventional CNN, a TFET-based ternary CNN requires fewer computational steps and obviates the necessity of a complete datapath – thus reducing hardware by half.

II. Background

The conventional single-layer, spatially invariant CNN architecture proposed in [2] is an $M \times N$ array of identical cells (Fig. 1a). Each cell, C_{ij}, $(i,j) \in \{1,...,M\} \times \{1,...,N\}$, has identical synaptic connections with all the adjacent cells in a predefined neighborhood, $N_r(i,j)$ of radius r. The size of the neighborhood, m, depends on the distance between the central cell, C_{ij}, and its adjacent cells, where $m = (2r+1)^2$, and r is a positive integer. The conventional design of C_{ij} consists of one resistor, one capacitor, $2m$ linear voltage controlled current sources (VCCSs), one fixed current source, and one non-linear voltage controlled voltage source (Fig. 1b). The node voltages $u_{i,j}$, $x_{i,j}$, and $y_{i,j}$ correspond to the input, state,

978-3-9815370-2-4/DATE14/©2014 EDAA

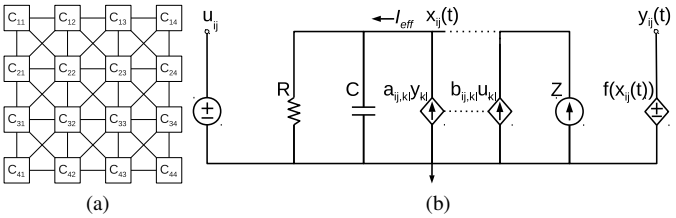


Fig. 1. (a) CNN topology; (b) Circuit layout for a conventional CNN cell.

and output of $C_{i,j}$, respectively. The input and output voltages of the m neighbors contribute m feedback and m control currents, respectively, to $C_{i,j}$ through the linear VCCSs.

The dynamics of the CNN can be expressed by a system of $M \times N$ ordinary differential equations (ODEs), each of which is simply the Kirchhoff's Current Law (KCL) at the state nodes of the corresponding cells as shown in Eq. 1. At any given time, each cell in the network would have a net current, I_{eff}, flowing into its state node x, from various VCCSs, as well as the fixed bias.

$$C\frac{dx_{ij}\left(t\right)}{dt} = -\frac{x_{ij}\left(t\right)}{R} + \sum_{C_{kl}\in N_r(i,j)} a_{ij,kl}y_{kl}\left(t\right) + \sum_{C_{kl}\in N_r(i,j)} b_{ij,kl}u_{kl} + Z \tag{1}$$

Here, $a_{ij,kl}$ and $b_{ij,kl}$ act as weighting parameters for the feedback and control currents from cell C_{kl} to cell C_{ij}. As the synaptic connections between cells are space invariant, these parameters are denoted by two 3×3 matrices (for $r = 1$), and are referred to as the feedback template A and the control template B. The parameter Z represents a fixed bias current, and provides a means to adjust the total current flowing into the cell. By carefully programming the values of the A and B templates as well as Z, it is possible to solve a wide range of binary classification problems.

A conventional CNN cell also employs a non-linear sigmoid-like output transfer function $f\left(x_{ij}\left(t\right)\right)$ specified by Eq. 2 to make the output state to saturate at either a high or low voltage (e.g., $+1\ V$ or $-1\ V$).

$$y_{ij}\left(t\right) = \frac{1}{2}\left(\mid x_{ij}\left(t\right)+1 \mid - \mid x_{ij}\left(t\right)-1 \mid\right) \tag{2}$$

To perform binary classification it is essential to have some form of non-linear relationship between I_{eff} and the output voltage, which is provided by the output transfer function defined above. It is also possible to introduce non-linearity to the state node's behavior by replacing the linear resistor with a non-linear resistive component or device. When employed in a CNN architecture, non-linear devices like Resonant Tunneling Diodes (RTD) [9], [10], Tunneling Field Effect Transistors (TFET) [11], etc. are shown to be capable of solving binary classification problems.

Among the potential non-linear devices, devices with steep slopes and that operates at low voltages are especially interesting. Devices with steep current growth regions in their I-V characteristics can accommodate a wide range of currents within a very narrow window of voltages. As such, a number of different values of I_{eff} corresponding to a specific output class would result in stable voltages within a very close range. The given output class can be represented by this narrow voltage window, and the steep-slope of the device itself ensures saturating state voltages. Therefore, the non-linear output transfer function is no longer required; i.e., the state voltage and output becomes equivalent to each other. Furthermore, to compensate for device mismatch issues associated with current CMOS scaling, implementations of the output transfer function could require a large amount of area [10]. Hence, by employing steep-slope devices in the CNN cell design, it should be possible to reduce the area of each cell. The low voltage operability of the devices improves power dissipation.

III. Multi-valued CNN with Emerging Devices

Multi-valued CNNs provide a powerful alternative to solve general classification problems [16]. Though it is possible to decompose a multi-valued problem with n classes into a series of $n-1$ binary classification steps, both operation time and energy dissipation would obviously increase with this approach. Also, reprogramming hardware between iterations (for different template operations) would introduce additional overheads. Therefore, a CNN cell capable of classifying multiple classes in a single step would be useful. Existing CNNs achieve multi-value functionality either by using output function that has several saturated levels [16] or by the discrete time version of CNN (DT-CNN) [17].

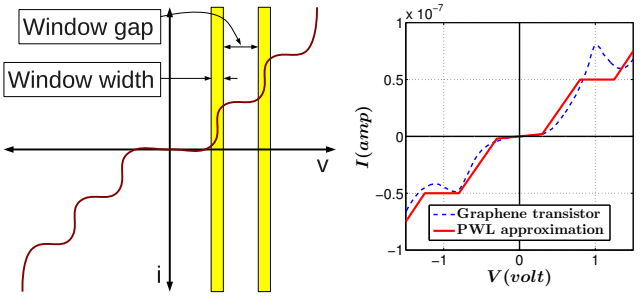
A. Desired Characteristics

We first discuss how a CNN architecture can be used to solve multi-valued problems in a single step by enforcing some characteristics in a non-linear device's I-V. An example of a desirable device I-V characteristic is shown in Fig. 2a. More specifically, a device (or equivalent circuit) should exhibit more than two current growth regions as each growth region can represent an output level. Furthermore, very steep current growth regions are desired as this ensures that stable state voltages would be bounded within very narrow windows, and this would further eliminate the need for analog to digital conversion at the output. Also, it is desirable that the growth regions of a device are reasonably well separated, as this should lead to more robust operation in the presence of noise. Ideally, the slopes of the I-V characteristics in the separation regions should not be positive, as this could effectively merge two neighboring output windows. Interestingly, recent work on double-layer graphene transistors [14] suggests that a single device (Fig. 2b) might be able to deliver desired I-V characteristics (like those illustrated in Fig. 2a).

B. Example Multi-valued CNN

Assuming a piece-wise linear approximation (Fig. 2b) of the graphene transistor (for simplicity), we now demonstrate how CNN cells based on such characteristics can perform quaternary classifications. First, we explain the operation principle of a quaternary CNN cell through the concept of driving point (DP) plots [18]. To this end, the cell equation is rewritten as:

$$C\frac{dx_{ij}\left(t\right)}{dt} = -h\left(x_{ij}\left(t\right)\right) + a_{ij,ij}x_{ij}\left(t\right) + \sum_{C_{kl}\in N_r(i,j)\wedge kl\neq ij} a_{ij,kl}x_{kl}\left(t\right) + \sum_{C_{kl}\in N_r(i,j)} b_{ij,kl}u_{kl} + Z \tag{3}$$



(a) (b)

Fig. 2. (a) Example characteristics of a CNN device for multi-valued problems; (b) I-V characteristics of the double-layer graphene device at room temperature [14], and its Piece-wise linear (PWL) approximation.

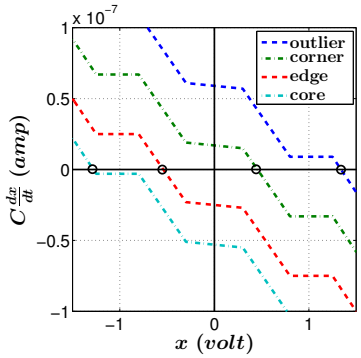


Fig. 3. DP plots for the representative cases of the four classes with $k = 7 \times 10^{-9}$ and $\varepsilon = 3 \times 10^{-9}$. The state equilibrium points are marked with open circles.

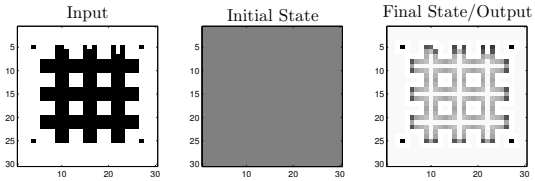
where $h(x_{ij})$ represents the graphene transistor's I-V characteristics. In a DP plot, Eq. 3 is plotted as a function of the state voltage, x_{ij}. The shape of the plot can be modulated by the first two right hand side terms (together called the DP component), whereas the last three terms' summation provides an offset to shift the plot vertically. As such, the equilibrium states of a cell can be identified at points where the plot intersects the x-axis with a negative slope. Physically it means that at equilibrium, the current through the capacitor is zero – i.e., the capacitor has completely charged or discharged to the equilibrium voltage.

Below, we use an example problem to further illustrate quaternary CNN functionality. Given an image of an object as input (see Fig. 4a), the problem is to identify four distinct features, e.g., outliers, corners, edges, and cores. Each cell processes a single pixel of the input image. The input nodes of the cells are provided with the corresponding input image pixel ($-1\ V$ or $+1\ V$ for a white or black pixel, respectively). The cell states can be initialized with any random values. While a detailed discussion of template design is beyond the scope of this paper, the template values are:

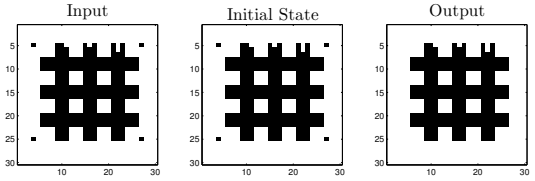
$$A = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, B = k \begin{bmatrix} -1 & -1 & -1 \\ -1 & 8 & -1 \\ -1 & -1 & -1 \end{bmatrix}, Z = -8k + \varepsilon$$

As the values in the feedback template are equal to zero, the DP component becomes the negated version of the device's I-V. From Fig. 3, we see that each steep-slope current growth region of the device is responsible for identifying one particular feature of the problem. For a given feature, the programmed templates offset the DP component by the proper amount of current such that the responsible steep-slope (negated in DP) intersects with the x-axis and results in an equilibrium state voltage. The ranges of stable voltages for the features are always finite, and mutually exclusive. Thus, with proper template design graphene transistor based cells can reach desired output states.

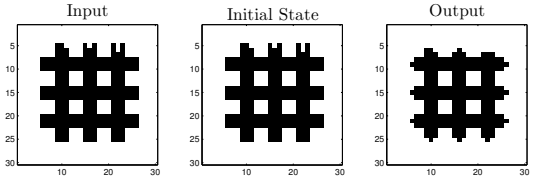
To verify the cell array dynamics, we augmented a MATLAB based simulator [19] that solves a system of ODEs numerically by using the Runge-Kutta method. For an $M \times N$ CNN array, the system of ODEs consists of MN equations each defined for a given cell. Each cell in the array requires an initial value for the state voltage which defines the initial condition for the cell's equation. Fig. 4 illustrates the simulation results of the quaternary problem solved by both the graphene transistor based CNN (in a single computational step, Fig. 4a), and the conventional CNN (requires three computational steps, Fig. 4b-d). The resistor value in the conventional CNN is set to 36 $M\Omega$ such that the settling time for a binary step is similar to that of graphene transistor based CNN. During each step, the conventional approach eliminates one particular feature, and passes the remaining features to the succeeding step. Moreover, step 1 requires pre-processing to initialize the state nodes with the input image. Altogether, simulation suggest that the conventional CNN takes 59 ns to complete the quaternary classification whereas the graphene transistor based CNN needs only 16 ns.



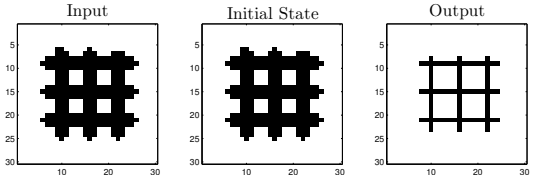
(a) Single step of graphene transistor based CNN



(b) Step 1 of conventional CNN



(c) Step 2 of conventional CNN



(d) Step 3 of conventional CNN

Fig. 4. Simulation results for quaternary classification.

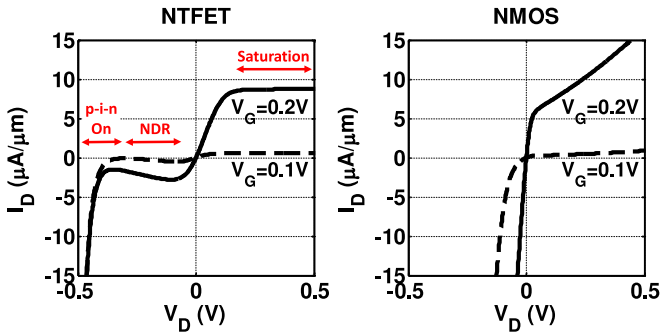


Fig. 5. I-V characteristic of a TFET and a MOSFET. The drain current is given per width of the transistor. The length of the NMOS is 24 nm, the minimum in the 22 nm technology.

IV. Circuits for Multi-valued Problems

While the previous section illustrates their utility, devices such as graphene transistors are still in the early stages of development and additional studies and experiments are required before these devices can be used in complex systems such as CNNs. In this section, we show that multi-valued characteristics can be realized via circuits based on a more mature beyond-CMOS technology. An InAs TFET technology [20] is considered in this work. The transistors have a channel length of 20 nm, channel thickness of 7 nm and oxide thickness of 2.5 nm. A verilog-A model is built from T-CAD device simulations using the method explained in [21]. The DC characteristic of an N-type TFET is shown in Fig. 5, where the source terminal of the transistor is grounded and the drain terminal is changed from -0.5 V to 0.5 V. Compared to a 22 nm MOSFET [22] [23], TFET shows a higher output resistance when operating in the saturation region (at a large positive V_{DS}), and negative differential resistance (NDR) at negative drain-source voltages [11].

The key component in building a ternary cell is a nonlinear resistance that can be used to replace the nonlinear term in Eq. 3. Such a resistance can be created using an NTFET and PTFET as shown in Fig. 6a. The I-V characteristic of the resulting element (shown in Fig. 6b) has three low resistance regions: one low-resistance region around 0 V, where the two TFETs are in ohmic (linear) region, and two other low-resistance regions where the p-i-n diode of one of the two TFETs is turned on. In between these regions, the resistance is high (and sometimes negative) because one TFET is in the saturation, and the other in the NDR region. The I-V curve in Fig. 6b is sufficient for a ternary CNN cell. However, the two non-linear regions at the beginning and the end of the curve are determined by the turn-on voltage of the p-i-n diodes (V_{ON}) and hence are not programmable. Furthermore, the large value of V_{ON} mandates a large peak-to-peak voltage swing of about 1 V over the nonlinear component. For TFETs based on a technology with a bandgap voltage higher than that of InAs (e.g. a Si-based TFET), V_{ON} will be even larger, resulting in a voltage swing and supply voltages well beyond the breakdown voltages of other transistors in the cell.

To add to the programmability of the cell and make it compatible with low supply voltages, the nonlinear element in Fig. 7a is proposed. It combines the idea of Fig. 6a with a clamp circuit consisting of transistors T3 and T4. For small values of $|V_{in}|$, both T3 and T4 are off and the I-V

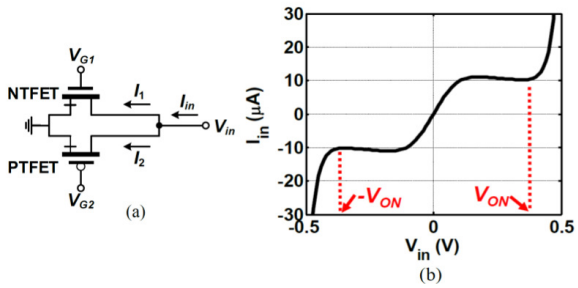


Fig. 6. (a) Nonlinear element. (b) Characteristic of the nonlinear element. The width of the TFETs is 1 μm.

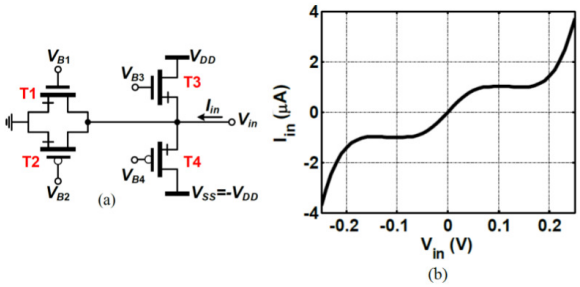


Fig. 7. (a) Proposed nonlinear element for a ternary cell. (b) Its DC characteristic when $V_{B1} = V_{B4} = 0.1V$, $V_{B2} = V_{B3} = -0.1V$, $V_{DD} = -V_{SS} = 0.25V$ and the width of all TFETs is 1 μm.

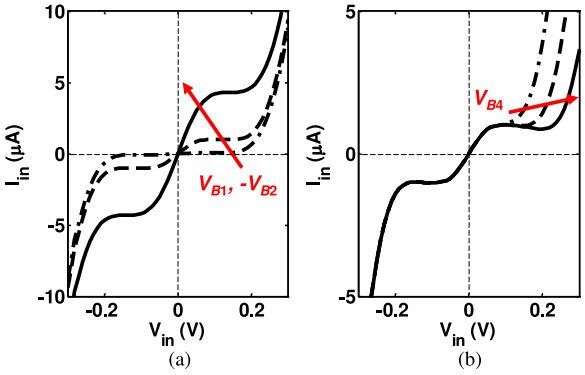
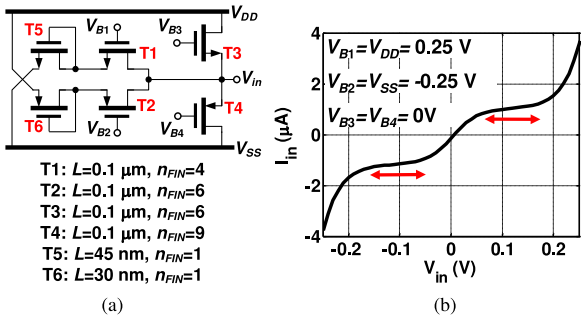


Fig. 8. (a) Sweeping V_{B1} and $-V_{B2}$ from 50 mV to 150 mV, whereas other parameters are similar to those of Fig. 7b. (b) Sweeping V_{B4} from 50 mV to 150 mV, while other parameters are similar to those of Fig. 7b.

characteristic of the cell (shown in Fig. 7b) is similar to that of Fig. 6b. When V_{in} is smaller than $V_{B3} - V_{TH}$ (where V_{TH} is the threshold voltage of the TFET) such that T3 is turned on, a large current will be conducted by the transistor. Similarly for large positive values of V_{in}, T4 will conduct a large current. Using the four bias voltages V_{B1-4}, it is possible to tune the characteristic of the element. Fig. 8 illustrates two examples of such tunings. This feature adds to the versatility of a CNN to handle different applications. Moreover, the small voltage swing of the nonlinear element allows the difference between the positive and negative supply rails to be as low as 0.5 V.

It is instructive to compare the TFET-based nonlinear element with a CMOS design shown in Fig. 9a. Here, the diode-connected transistors T5 and T6 are added to make the current passing through T1 and T2 asymmetric. A major difference between Fig. 7b and Fig. 9b is that in the two



(a) (b)

Fig. 9. (a) CMOS nonlinear element. Note to the increase of transistor length (L) which is done to improve the output resistance of the MOSFETs. (b) The I-V characteristic of the CMOS nonlinear element.

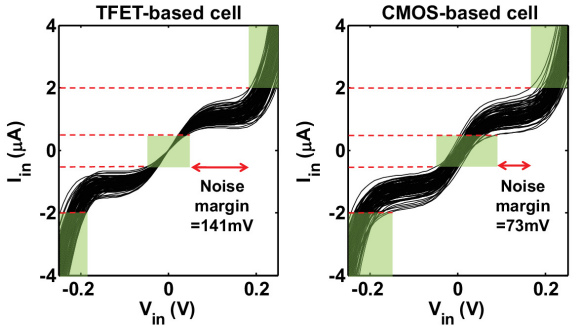
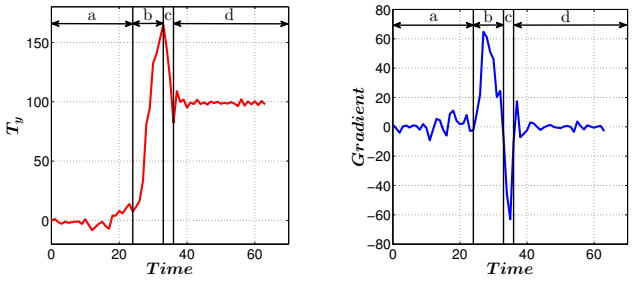


Fig. 10. Impact of threshold voltage variations on the characteristic of the nonlinear elements.

regions that a high resistance is expected, the resistance of the CMOS-based design is significantly lower than that of the TFET-based design. This is a consequence of the higher output resistance of TFETs shown in Fig. 5, and degrades the noise margin when the ternary cell is used in classification tasks. The robustness of the cells can be evaluated using Monte-Carlo simulation. Since the mismatch properties of the transistors are not yet available, the threshold voltage of the transistors was varied by adding random errors to the gate voltages. The errors have a Gaussian distribution with a zero mean and a standard deviation of 10 mV. Fig. 10 shows the result of 100 runs. The dashed areas show the target input/outputs of the cell assuming that a given classification task results in cell currents in three range of (-∞,2mA), (-0.5mA, 0.5mA), and (2mA,∞). Clearly, the TFET-based design demonstrates a higher noise margin.

V. Case Study

As a case study, we consider how CNNs that employ ternary classification circuitry can be used to solve a tactile sensing problem. Initially described in [15], CNNs can be used to process vertical sheer stress – which is an indicator of slippage of an object grasped by a two-fingered robotic hand. Fig. 11 (from [15]) describes the time-evolution of the vertical sheer stress (denoted as T_y) and its gradient when an object starts to slip out of the robotic grasp as a result of increased weight. Here, the task of the CNN system is to measure the duration of region 'b', and 'c' locally, which conveys information about how much weight is applied to the object and how fast it is slipping. Based on this data, the next level of computation (which may not be located with sensors) can make a decision about exactly how much grasping force should be applied to stop the slippage without causing any harm to the object.



(a) (b)

Fig. 11. (a) Profile of the vertical component of sheer stress, T_y from [15]. In region 'a', nothing is grasped. T_y increases proportionally with the weight, in region 'b'. During 'c' the object starts to slip out of the robot's grasp. In 'd', T_y becomes stable as it equal with the kinetic friction force; (b) The gradient profile of T_y.

Employing the TFET circuit-based ternary CNN, we can solve the slippage detection problem in 3 steps as shown in Fig. 12. The input to the system is a 64×64 gray scale image, where each column corresponds to a given sensor, and the image data reflect the normalized T_y profile over time (as in Fig. 11a). To account for the 64 sensors in the system, data for each time step (i.e., a row in the input image) is generated by a normal distribution with the value from Fig. 11a (for the given time step) as the mean, and 10% of the value as variance. The first step calculates the gradient of T_y with respect to time (similar to the data in Fig. 11b). The output of the gradient function shows the positive and negative bulges in the gradient profile (i.e., region 'b' and 'c') as black and white horizontal strips, respectively.

The next step, referred to as thresholding, classifies the output data of Step 1 into three distinct classes: positive (black) and negative (white) bulges, and no-change (gray) (see Fig. 12). The I-V characteristic of the TFET based-circuit (Fig. 7b) represents a black, white, and gray pixel by $(0.20, 0.25)$ V, $(-0.25, -0.20)$ V, and $(-0.05, 0.05)$ V, respectively. The functionality of this step is explained in Fig. 13a, where the three stable state voltages (marked with open circles) are separated by the two meta-stable points p and q. Any initial state voltage in the ranges of $(-\infty, p)$, (p, q), and (q, ∞) would eventually settle to one of the three stable voltages that reside in that range. Thus, the output of the threshold function contains pixels of only three distinct values.

The final step is the connected component detection (CCD) function that projects the presence of a black/white pixel in a horizontal line, to the leftmost column by the same colored pixel. As a result, by counting the number of black and white pixels in the first column, the lengths of region 'b' and 'c' are obtained. The information is processed by the next level for making further decisions. Note that, CCD requires its input pixels to be strictly stratified to one of the class levels for its correct functionality. This is why the threshold step is required.

As a comparison, a solution of the same problem based on a conventional binary CNN requires 5 steps and 2 sets of hardware (see [15] for more detail). This additional cost in both hardware and time is due to the fact that a binary classifier would only be able to retain information about one bulge in an image as one of the two stable output levels needs to be reserved for representing the empty space.

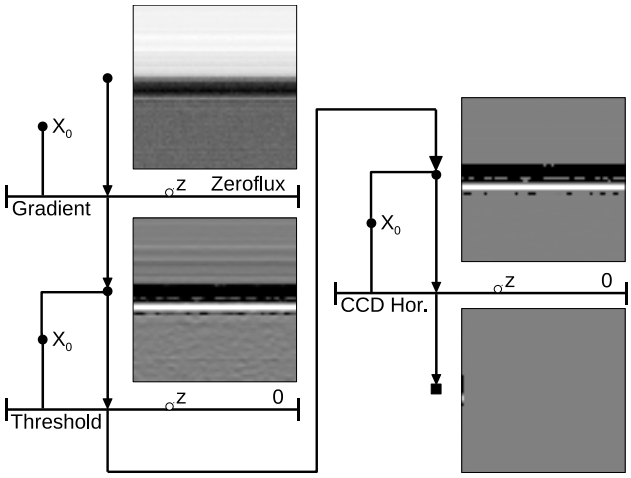
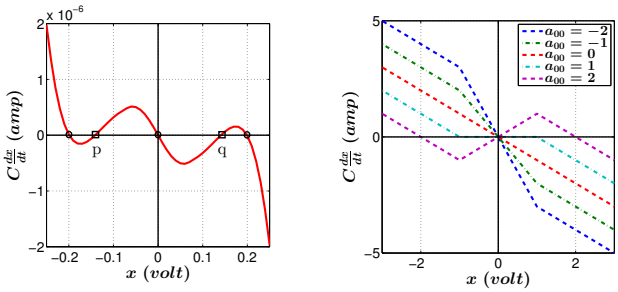


Fig. 12. The Universal Machines on Flows (UMF) [24] description of the TFET circuit-based CNN for detecting slippage.



(a) (b)

Fig. 13. DP components for (a) TFET circuit-based CNN with the center matrix element of the feedback template, $a_{00} = 7 \times 10^{-6}$; (b) Conventional CNN with 1 Ω resistance.

This fact becomes evident also from Fig. 13b, where we can find at most two stable output levels for any of the curves. Consequently, the solution of the problem through conventional CNN requires two different sets of hardware. Thus, TFET circuit-based CNN requires fewer computational steps (3 vs. 5), and reduces hardware by half.

VI. Conclusion

Apart from overcoming the challenges in digital computation, emerging devices have a great promise for enabling new and enhanced functions for non-von Neumann computing paradigms. Moreover, circuits built from emerging device technologies could also bring clear benefits over existing approaches. Initial study shows that at the cell level, multi-valued classifications improve the energy dissipation by an order of magnitude. Detail analysis of the energy, power, and performance – considering other system components (e.g., the current multipliers) – would be considered in future work.

Acknowledgment

This work was supported in part by the Center for Low Energy Systems Technology (LEAST), one of six centers of STARnet, a Semiconductor Research Corporation program sponsored by MARCO and DARPA. The authors also acknowledge Tamás Roska from Pázmány Péter Catholic University, Hungary for valuable discussion.

References

[1] H. Esmaeilzadeh *et al.*, "Dark silicon and the end of multicore scaling," *IEEE Micro*, vol. 32, no. 3, pp. 122–134, 2012.

[2] L. O. Chua *et al.*, "Cellular Neural Networks: Theory," *IEEE Transactions on Circuits and Systems*, vol. 35, no. 10, pp. 1257–1272, 1988.

[3] ——, "Cellular Neural Networks: Applications," *IEEE Transactions on Circuits and Systems*, vol. 35, no. 10, pp. 1273–1290, 1988.

[4] ——, "The CNN paradigm," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 40, no. 3, pp. 147–156, 1993.

[5] T. Roska *et al.*, "Toward visual microprocessors," *Proceedings of the IEEE*, vol. 90, no. 7, pp. 1244–1257, 2002.

[6] K. Karahaliloglu *et al.*, "Bio-inspired compact cell circuit for reaction-diffusion systems," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 9, pp. 558–562, 2005.

[7] J. Kowalski, "0.8 um CMOS implementation of weighted-order statistic image filter based on cellular neural network architecture," *IEEE Transactions on Neural Networks*, vol. 14, no. 5, pp. 1366–1374, 2003.

[8] P. Kinget *et al.*, "A programmable analog cellular neural network CMOS chip for high speed image processing," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 235–243, 1995.

[9] M. Hanggi *et al.*, "Cellular neural networks based on resonant tunnelling diodes," *International Journal of Circuit Theory and Applications*, vol. 29, no. 5, pp. 487–504, 2001.

[10] P. Mazumder *et al.*, "Tunneling-Based Cellular Nonlinear Network Architectures for Image Processing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 4, pp. 487–495, 2009.

[11] I. Palit *et al.*, "TFET-based cellular neural network architectures," in *ISLPED*, 2013, pp. 236–241.

[12] M. Itoh *et al.*, "RTD-based Cellular Neural Networks with Multiple Steady States," *International Journal of Bifurcation and Chaos*, vol. 11, no. 12, pp. 2913–2959, 2001.

[13] E. Buccafurri, "Analytical modeling of Silicon based Resonant Tunneling Diodes for RF oscillator Application," Ph.D. dissertation, National Institute of Applied Sciences, Lyon, France, 2010.

[14] L. Britnell *et al.*, "Resonant tunnelling and negative differential conductance in graphene transistors," *Nature Communications*, vol. 4, p. 1794, 2013.

[15] A. Kis *et al.*, "3D tactile sensor array processed by CNN-UM: a fast method for detecting and identifying slippage and twisting motion," *International Journal of Circuit Theory and Applications*, vol. 34, no. 4, pp. 517–531, 2006.

[16] A. Kanagawa *et al.*, "Cellular neural networks with multiple-valued output and its application," *IEICE Trans. on Fundamentals of Electronics*, vol. E79-A, no. 10, pp. 1658–1663, 1996.

[17] H. Harrer *et al.*, "Discrete-time cellular neural networks," *International Journal of Circuit Theory and Applications*, vol. 20, no. 5, pp. 453–467, 1992.

[18] L. O. Chua *et al.*, *Cellular Neural Networks: Foundations and Primer*. Cambridge University Press: Cambridge, 2001.

[19] R. Csaba, *MATCNN. Analogic CNN simulation toolbox for MATLAB. Version 1.0. (Research report of the Analogical and Neural Computing Laboratory, DNS-11-1997.).* MTA SZTAKI, 1997.

[20] U. Avci *et al.*, "Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic," in *Symposium on VLSI Technology*, 2011, pp. 124–125.

[21] V. Saripalli *et al.*, "An energy-efficient heterogeneous CMP based on hybrid TFET-CMOS cores," in *Design Automation Conference (DAC)*, 2011, pp. 729–734.

[22] S. Sinha *et al.*, "Exploring sub-20nm FinFET design with Predictive Technology Models," in *Design Automation Conference (DAC)*, 2012, pp. 283–288.

[23] "PTM-MG model," [online], June 2012, Available: http://ptm.asu.edu.

[24] T. Roska, "Computational and computer complexity of analogic cellular wave computers," in *IEEE International Workshop on Cellular Neural Networks and Their Applications*, 2002, pp. 323–338.