# Design of 3D Nanomagnetic Logic Circuits: a Full-Adder Case Study

Robert Perricone, X. Sharon Hu, Joseph Nahas, and Michael Niemier
Department of Computer Science and Engineering, University of Notre Dame
Notre Dame, IN 46556, USA, Email: {rperrico,shu,jnahas,mniemier}@nd.edu

***Abstract*—Nanomagnetic logic (NML) is a "beyond-CMOS" technology that combines logic and memory capabilities through field-coupled interactions between nanoscale magnets. NML is intrinsically non-volatile, low-power, and radiation-hard when compared to CMOS equivalents. Moreover, there have been numerous demonstrations of NML circuit functionality within the last decade. These fabricated structures typically employ devices with in-plane magnetization to move and process data. However, in-plane layouts imply circuits and interconnects in only two dimensions (2D), which makes signal routing – and hence circuits – more complex. In this paper, we introduce NML circuits that move and process data in three dimensions (3D). We employ devices with perpendicular magnetic anisotropy (PMA) (i.e., out-of-plane magnetization states) and discuss their behavior when utilized in 3D designs. Furthermore, we provide a systematic design approach for 3D NML circuits using a threshold full adder as a case study. We compare our 3D adder to 2D adders to highlight the benefits of 3D NML circuits, which include simpler signal routing and a smaller area footprint.**

## I. Introduction

Nanomagnet logic [1] (NML) employs bistable, single-domain nanomagnets to store binary data. Via fringing field interactions, NML devices can be used to both propagate and process information [1], [2]. In principle, NML ensembles can be integrated with CMOS logic as magnetization states can be set or read using current driven wires [3] or magnetic tunnel junctions (MTJs) [4].

Most NML circuits have been comprised of devices that have in-plane magnetization states. Still, when considering design issues such as signal routing, in-plane devices are restrictive as logic *and* interconnect are confined to a single functional layer [2]. As a result, circuits have larger footprints due to replicated inputs, long signal propagation paths, etc.

More recently, NML devices with perpendicular magnetic anisotropy (PMA) (i.e., out-of-plane magnetization states) have been proposed [5], and simple circuits have been experimentally demonstrated [6], [7], [8]. (In this paper, we refer to the out-of-plane device architecture as pNML.) Furthermore, experimental demonstrations suggest that circuits comprised of devices with PMA can employ additional functional layers as a means to route signals [9]. In this paper, we illustrate how logical operations/gates can also be distributed over multiple functional layers. Furthermore, by using multiple functional layers for logic, compact circuits that would typically require 10s of devices, multiple gates, and/or large devices can be reduced to just a few small devices.

More specifically, we will first discuss a set of observations that are essential for developing three dimensional (3D) pNML circuits. We then present a methodology that can be used to design 3D pNML circuits. The output of our methodology is a design that should function correctly (for all possible input combinations) when tested via micromagnetic simulation with a uniform clocking methodology. As it is generally well-accepted that there is good correlation between micromagnetic simulations and experimental results (e.g., [10]), outputs from our design methodology can serve as initial fabrication targets for experimental verification and testing.

As proof-of-concept, we illustrate the application of our methodology to design a 3D full adder. The adder is based on threshold logic [11], and by employing multiple functional layers, just 5 magnets are required to realize the entire structure. (This *includes* the 3 input magnets.) Finally, we compare our design to other (NML-based) adder designs. Notably, our design is almost an order of magnitude denser than other designs reported in the literature. Critical path lengths are also reduced. As longer device switching times (when compared to a transistor) are one of NML's less desirable features, minimizing critical path lengths is especially important.

## II. Background

Most NML research has focused on devices that couple in-plane (iNML) [1], [2]. Per Fig. 1a, the magnetization direction of an in-plane device can be used to represent binary information, and fringing field interactions between devices can be used to process information. However, it is also possible to create nanomagnets with perpendicular magnetic anisotropy (pNML) [12], [13] (Fig. 1b). Again, magnetization state can be used to represent binary information. (In Fig. 1b, a positive $Z$-magnetization ($+M_z$) represents a logic '1' whereas a $-M_z$ represents a logic '0'.) While devices with PMA can also process information via fringing field interactions, there are some important differences with respect to how pNML devices switch/are clocked when compared to iNML.

With pNML, focused ion beam (FIB) irradiation can be employed to further influence device switching. Experimental and simulation-based studies have shown that by partially irradiating a specific location of a pNML device (e.g., an edge), one can define the nucleation center for the switching of the magnet [14]. The coercivity of the magnet is determined by the coercivity of its highest-irradiated region. Localized FIB irradiation can also define dataflow directionality as a given magnet will couple more strongly with one neighbor than another.

This allows large arrays of pNML device ensembles can be re-evaluated (or "clocked") with a global out-of-plane

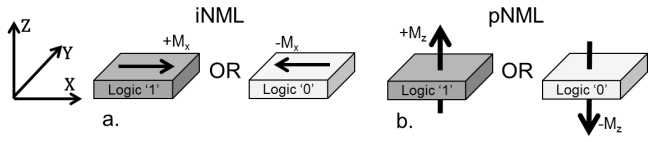


Fig. 1. (a) in-plane (iNML) vs. (b) perpendicular (pNML). iNML magnetization direction is parallel to the $XY$-plane while pNML is perpendicular to the $XY$-plane. The two possible stable states for each type are shown.

This work is supported in part by the NSF NEB program under grant CCF-1124850.
978-3-9815370-2-4/DATE14/©2014 EDAA

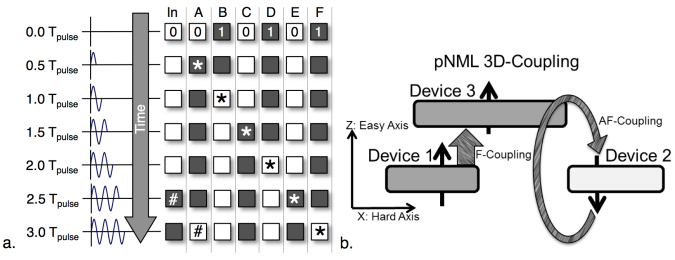


Fig. 2. How information would move in an AF-ordered line (assuming that the left edge of each magnet is FIB irradiated); * is used to show dataflow associated with the new input.

magnetic field [6], [7], [8], [13]. Data moves in a clocked ensemble as metastable (MS) states (parallel-aligned magnet pairs) can be deterministically driven out of the pNML circuit. During each field cycle, a switching event occurs if and only if a neighbor is in a parallel, MS state. After an appropriate number of field cycles – defined by the critical path through an ensemble of interest – metastabilities are eliminated, and a logically correct, computational ground state is reached. On-chip, fields could be generated via inductor structures that could be coupled with a capacitance in an LC oscillator[15].

This process is illustrated in Fig. 2a [15] for a line of anti-ferromagnetically (AF) coupled pNML devices that are clocked with a sinusoidal, out-of-plane field (with a period of $T_{pulse}$ and a peak amplitude of $H_{pulse}$). $H_{pulse}$ should be determined such that it can switch a particular magnet if and only if a given device is metastable with respect to its neighbor on the input side. To avoid errors, the switching field margin should be larger than the switching field variations caused by film inhomogeneities, thermal noise, etc. – see Sec. 6. We assume magnets are FIB irradiated on their left edges, so information will flow from left-to-right. At time 0.0, the input to the AF-line has been flipped. After the first application of $H_{pulse}$ (in the +z-direction), the magnet immediately adjacent to the flipped input will change state after $0.5T_{pulse}$. ($0.5T_{pulse}$ must be greater than the magnet switching time.) For switching, $H_{pulse}$ should be of sufficient magnitude to remove the metastability at the input, but not of sufficiently high magnitude to alter the state of other magnets in the line. As the clock waveform transitions such that $H_{pulse}$ is negative, the metastability between Magnets A and B is removed, and Magnet B switches to the new, logically correct state associated with the new input. Note that after two applications of $T_{pulse}$, the state of the input magnet is flipped (at $2.5T_{pulse}$). With successive applications of the time varying field, multiple bits of information can move through the AF-line simultaneously.

When comparing iNML to pNML, pNML does have several distinct advantages [16]. Notably, signal routing can be simplified as devices can be arbitrarily sized. As such it is easy to obtain a complemented/uncomplemented signal value as needed in a circuit layout. Similarly, irregularly shaped pNML devices (e.g., L-shaped devices) are still single domain (see images in [7], [8]). This also simplifies in-plane signal routing. Finally, as alluded to earlier, pNML devices can also interact with one another in a third dimension. For example, in Fig. 2b, two pNML devices can couple ferromagnetically when they overlap. This effect led to the experimental demonstration of true, 3D signal crossings with devices that communicate via fringing field interactions [9]. While this too can simplify signal routing, we can also leverage additional functional layers for 3D logic operations – the focus of this paper.

## III. Design Methodology

In this section, we first discuss observations related to how 3D pNML devices (i.e., nanomagnets) interact with one another. We then present the basic concept behind threshold logic based pNML. We close by describing a general design process for generating 3D pNML circuits.

### A. Observations on 3D pNML device interactions

We leverage micromagnetic simulations to investigate the interactions between pNML devices. In our work, we use the Object Oriented Micro-Magnetic Framework (OOMMF) developed by NIST [17]. Relevant simulation parameters are chosen based on experimental results [18]. Below, we present several key observations derived from 3D pNML structures, which form the basis of our systematic design process.

We first discuss simulations of two overlapping magnets in different layers, which are 24 nm apart. Each magnet was $100 \times 100 \times 6\text{nm}^3$. Magnet $B$ (bottom) was held constant at logic '1' while Magnet $A$ (top) was able to change state (per the approach in [9]). We then subjected this system to a global clocking field to facilitate the switching of Magnet $A$. We varied parameters of Magnet $B$ (i.e., overlap, size, and distance) and observed their effect on the coupling with Magnet $A$. We then plotted the magnetization of Magnet $A$ (normalized with respect to the saturation magnetization ($M_s$)) versus the applied field (in units of milliTesla (mT)). Ultimately, we observed the magnitude of the clocking field necessary to switch Magnet $A$ from a logic '1' to a logic '0' and back to a logic '1' (i.e., magnetic hysteresis curves). We denote the field magnitude needed to switch a magnet to a logic '1' (resp., '0') as $H^1$ (resp., $H^0$).

Our first observation relates to how the amount of overlap between two magnets in different layers influences the coupling (F or AF) between them (e.g., Fig. 2b). In Fig. 3a, we show the effect of overlap on the coupling between Magnets $A$ and $B$. We began with an overlap of 100%, and reduced the overlap for subsequent simulations (Magnet $B$ is shifted as illustrated by the inset in Fig. 3a). At 100% overlap, Magnet $A$ switches from logic '1' to logic '0' at an applied field of -153 mT (i.e., $H_A^0 = 153$ mT) and switches back to logic '1' at 94 mT ($H_A^1 = 94$ mT). Not surprisingly, a logic '1' state is preferred from the F-coupled devices. ($H_A^1 < H_A^0$)

At 50% overlap (dashed line) we observed that $H_A^0 = 72$ and $H_A^1 = 44$. The decrease in $H_A^0$ and $H_A^0$ is the result of Magnet $A$ experiencing both AF-coupling (Fig. 2b) and F-coupling fields. For 25% overlap (dotted line), we observed that $H_A^0 \approx H_A^1$, and at 0% overlap (dash-dot line), the two magnets now couple anti-ferromagnetically since $H_A^0 < H_A^1$.

Our second observation illustrates how the size of a magnet affects coupling. The simulation results presented reflect reduced lengths and widths of Magnet $B$. Fig. 3b shows hysteresis curves that represent four different sizes of Magnet $B$. Observe that $H_A^1$ increases as the size of Magnet $B$ decreases. Smaller magnets provide less fringing fields, which may not influence the switching dynamics of Magnet $A$.

The third observation is the impact of distance between

The pNML devices are constructed from Co/Pt (Cobalt/Platinum) multi-layers. The anisotropy constant is 310 kJ/m$^3$, the saturation magnetization is $7.0 \times 10^5$ A/m, the exchange stiffness constant is $1.5 \times 10^{-11}$ J/m, and the damping coefficient is 0.05. A simulation mesh of $5 \times 5 \times 1.5$ nm$^3$ was used.

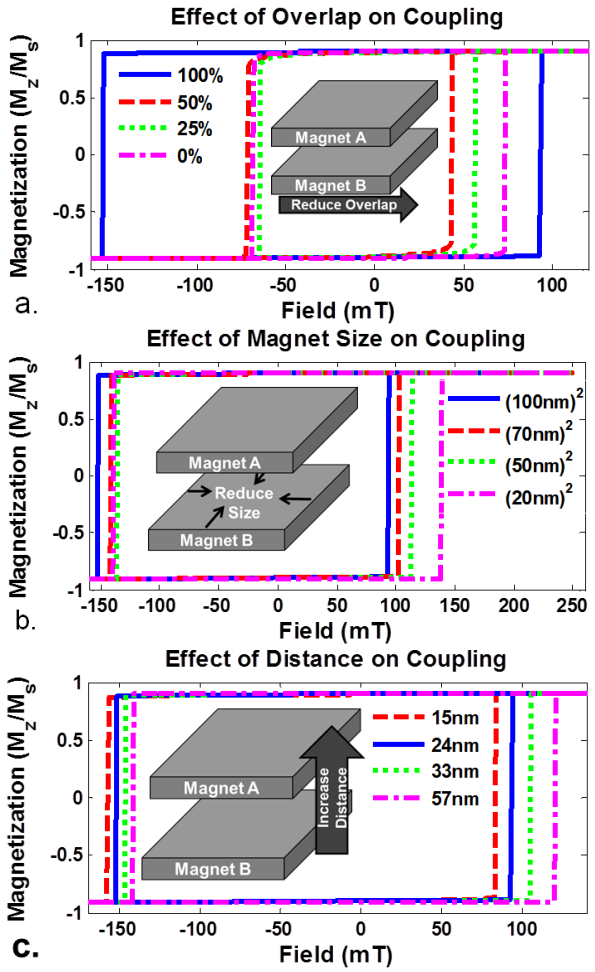


Fig. 3. Simulation results that demonstrate the effects of three important parameters for 3D pNML circuit design: overlap, size, and distance. In (a), we shift Magnet $B$ to vary the amount of overlap with Magnet $A$; (b) illustrates the effect of size on coupling by reducing the length and width of Magnet $B$; (c) shows the effect of distance between devices on the coupling.

layers. Fig. 3c shows that as the distance between layers increases, the coupling between the magnets decreases. While one may expect a greater field margin (difference between $H_A^0$ and $H_A^1$) by placing the functional layers close, our final observation demonstrates that another factor needs to be considered when determining the distance between layers.

More specifically, our final observation is related to the effects of strong in-plane fields from nearby AF-coupled magnets on a magnet in a different layer. In Fig. 4a, we show a more complex pNML layout with four devices. Magnets $A$, $B$, and $C$ are each $50 \times 50 \times 6$ nm$^3$ while Magnet $D$ is $190 \times 70 \times 6$ nm$^3$. Furthermore, the two layers are separated by 15 nm, and in the bottom layer we assume 10 nm spacing between devices $A$, $B$, and $C$. Magnets $A$, $B$, and $C$ are held at logic '0', '1', and '1', respectively.

AF-coupling between Magnets $A$ and $B$ produces a strong in-plane field in one half of Magnet $D$. This in-plane field can create a magnetic "torque," which could help Magnet $D$ transition to a new state. Conversely, Magnets $B$ and $C$ produce conflicting fields, which essentially cancel each other (i.e., produce no torque). The net effect of this input combination can cause Magnet $D$ to form multiple magnetic domains – although magnets considered so far are supposed to be single-domain (characterized by their uniform magnetization)

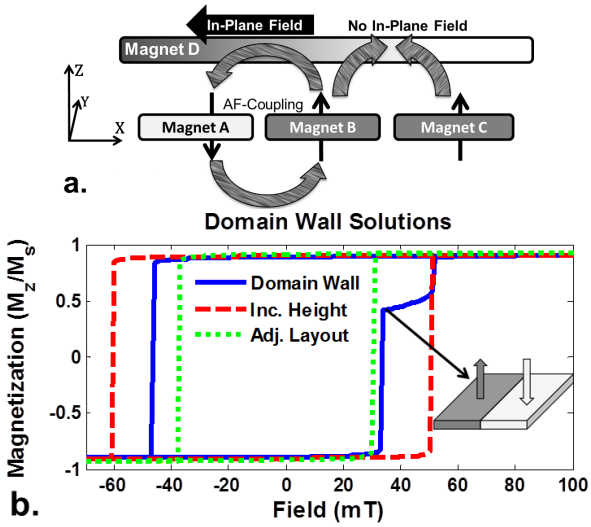


Fig. 4. (a) Illustration of how in-plane fields are produced by the AF-coupling of magnets in lower layers, which can cause domain walls. (b) Simulation of the 3D pNML circuit in (a). The solid line shows a stable domain wall when transitioning from a logic '0' to logic '1'. Domain walls can be avoided by increasing the height to avoid in-plane fields (dashed line) or be adjusting the circuit layout to reduce or prevent AF-coupling (dotted line).

– separated by a domain wall (e.g., the inset in Fig. 4b).

In pNML devices, the formation of a domain wall is dependent on a device's shape, size, and nearby coupling interactions [19]. While a domain wall can be removed via the global clocking field, the required field magnitude could be relatively high when compared to the single-domain switching field of the magnet [18]. For example, Fig. 4b captures simulation results associated with the circuit configuration illustrated in Fig. 4a. The solid line shows the formation of a domain wall when Magnet $D$ is switching from a logic '0' to a logic '1'. The part of Magnet $D$ that experiences the in-plane field (no cancelation) transitions to a logic '1' at 34 mT. However, the other half of the magnet experiences no initial torque, and remains in a logic '0' state until the clock field magnitude reaches 52 mT and removes the domain wall. The overall field margin for this situation is $H_D^0 = 47$ mT and $H_D^1 = 52$ mT, which appears to favor a logic '0'. However, intuitively, one would expect a logic '1' state to be preferred since Magnet $D$ should experience stronger F-coupling from Magnets $B$ and $C$ combined. Therefore, when designing pNML circuits, the possibility of a domain wall must be considered.

There are two ways to remove domain walls. The first is to increase the inter-layer distance. The dashed line in Fig. 4b shows that by increasing the height from 15 nm to 30 nm, a domain wall does not form and $H_A^1 < H_A^0$, as expected. The second is to redesign the layout to reduce or prevent AF-coupling between input magnets. The dotted line in Fig. 4b corresponds to shifting Magnet $B$ by 40 nm to reduce the overlap in the y-direction with Magnets $A$ and $C$. Magnet $D$ is also widened by 40 nm to overlap with $B$. Again, $H_A^1 < H_A^0$.

### *B. Threshold Logic based pNML*

In NML, the fundamental logic gate is a majority gate – i.e., a threshold logic gate (TLG). Furthermore, when considering pNML circuits that span multiple dimensions, more sophisticated threshold logic functions (i.e., with increased fan-in) could also be easily realized. In general, a threshold logic function is an $n$-input, one-output logic gate. The gate

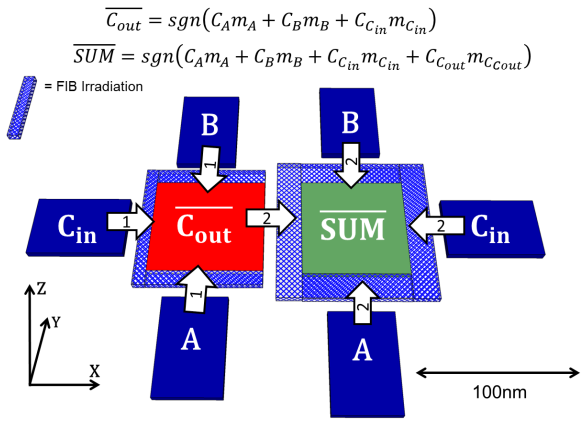


Fig. 5. 2D pNML threshold full adder. $\overline{C_{out}}$ is computed first from the inputs (arrows with 1s). Afterwards, $\overline{SUM}$ is computed from the four surrounding inputs (arrows with 2s). FIB irradiation is used for directed signal flow.

takes the weighted sum of its $n$-inputs, and outputs a logic '1' if threshold $T$ is exceeded or logic '0' otherwise. This is summarized by Eq. (1) – where $x_i \in \{0, 1\}$ are the inputs, and $w_i$ are the corresponding weights of each input [11].

$$F^T(x_1 \dots x_n) = 1 \text{ if } \sum_{i=1}^{n} w_i x_i \geq T$$
$$F^T(x_1 \dots x_n) = 0 \text{ if } \sum_{i=1}^{n} w_i x_i < T \quad (1)$$

When considering pNML TLG implementations, input devices will be placed in close proximity to the output device. The collective fringing-field interactions between output and input devices determine the preferred magnetization (logic) state. The weight of an input nanomagnet is its effective coupling field, which depends on factors such as size and distance between the output and input devices. The collective coupling field, $B_{out}$, from the inputs can be expressed by Eq. (2) – where $m_i \in \{-1, 1\}$ is the z-directed magnetization normalized by the saturation magnetization ($M_z/M_s$) and $C_i$ is the effective coupling field of the $i^{\text{th}}$ input.

$$B_{out} = C_1 m_1 + C_2 m_2 + \cdots + C_n m_n \quad (2)$$

$B_{out}$ is the net field that couples with the output magnet. It affects the clock field magnitude needed to switch the output.

As a brief example, Fig. 5 illustrates a 2D realization of a one-bit pNML full adder that utilizes two TLGs. The TLG expressions are given at the top. The first TLG has 3-inputs and computes the carry-out ($\overline{C_{out}}$). This is essentially a traditional 3-input majority gate (equally weighted inputs). The second TLG has 4-inputs and computes $\overline{SUM}$. Here, a logic '1' represents a positive magnetization state ($+M_z$) and a logic '0' represents a negative magnetization state ($-M_z$). Note that for the computation of $\overline{SUM}$, the weight of $\overline{C_{out}}$ is twice of that of other inputs and, thus, the $\overline{C_{out}}$ magnet is sized accordingly.

Per observations from Sec. III-A for 3D pNML structures, both F and AF-coupling are possible. If AF-coupling occurs between the $i^{\text{th}}$ input and the output, we have $C_i < 0$, and vice versa. In 3D designs, inputs can be sized or placed in different layers to affect their weight on the output device. Thus, 3D pNML TLGs provide additional benefits such as increased fan-ins and easier signal routing via multiple layers. Using insights from Sec. III-A and Sec. III-B, we now discuss a design process for 3D pNML circuits.

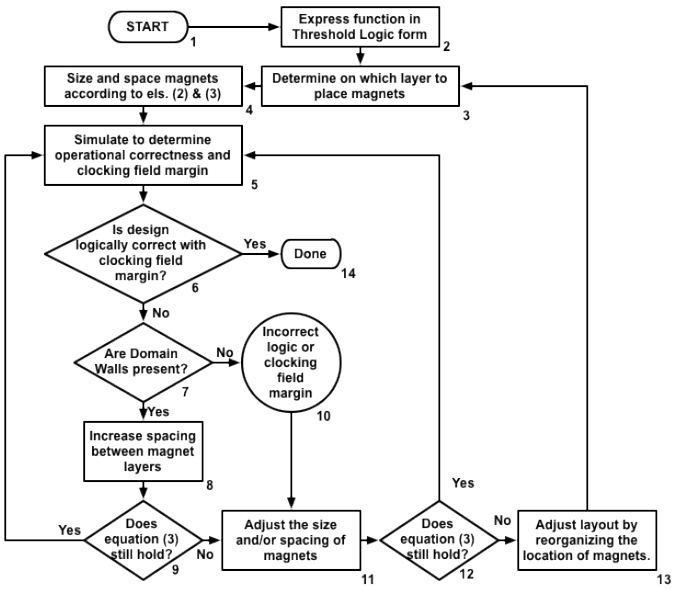


Fig. 6. Design process for 3D pNML circuits.

### C. Design Process

Our design flow is a 3-stage iterative process that will result in a 3D pNML circuit that functions correctly in micromagnetic simulations with a uniform clocking field for all input combinations. More specifically, we establish two conditions a pNML circuit must satisfy to be operational:

C1: $\forall i \in I \ (H_i^c < H_i^{\bar{c}})$

C2: $\min_{i \in I} (H_i^{\bar{c}}) - \max_{i \in I} (H_i^c) > \Delta_H$

where $I$ is the set of all possible input combinations, $H_i^c$ (resp., $H_i^{\bar{c}}$) is the clock field magnitude needed to switch the output from an incorrect (resp., correct) to correct (resp., incorrect) state for input combination $i$, and $\Delta_H$ is the field margin needed to tolerate fabrication variations, thermal noise, etc.

The 3-stage process is depicted in Fig. 6. The output of Stage 1 (steps 1-4) is an initial layout, while Stage 2 (steps 5, 6 and 14) and 3 (steps 7-13) iteratively update the initial layout such that it is operational in simulation subject to the above constraints. The key design parameters to consider are magnet overlap, size, and spacing (discussed in Sec. III-A). Additionally, in a 3D pNML circuit, layer assignment can significantly impact routability and circuit area. Our design process uses the observations discussed earlier to help make proper design choices. Below we discuss each stage in detail.

In Stage 1, we first decide in which layers input and output magnets should reside based on routability and area reduction. For simple circuits, we typically put input devices on one layer and output devices in another. This reduces area and provides different coupling options (F or AF). For more complex circuits with cascaded functions, it may be advantageous to place intermediate outputs and inputs on alternate layers to exploit different coupling options. After input and output layers are established, we determine the magnet arrangements within each layer, and select the magnet sizes and spacings based on the weights derived from the threshold logic functions (Sec. III-B). In general, one can just place and size the input magnets according to their desired weights in the output function.

In Stage 2, we examine if the given layout is operational per conditions C1 and C2. Micromagnetic simulation is used to test all possible circuit input combinations. It may be possible to find non-operational layouts more quickly by analyzing input

combinations and ranking them according to the expected level of difficulty in satisfying C1 and C2. Furthermore, some input combinations are identical by symmetry and can be omitted. If both C1 and C2 are satisfied, we have a operational circuit and the process stops. Otherwise, we invoke Stage 3.

Stage 3 aims to resolve design issues that lead to non-operational circuits. A design is considered non-operational if it experiences one or more of the following three problems: (i) existence of domain walls, (ii) logically incorrect outputs (i.e., C1), and/or (iii) insufficient clocking field margins (C2). Our design process works to correct these problems in an incremental fashion based on observations in Sec. III-A. Per Fig. 6, if a domain wall exists, we increase the distance between the layers. Increased distance reduces the in-plane fields that cause domain walls as discussed in Sec. III-A (see Fig. 4 and the associated description). Depending on the design, there is a height where domain walls will no longer be created from in-plane fields. However, as coupling between two layers becomes weaker as the distance increases, Eq. (2) may no longer hold. If the equation is no longer holds, there are two options, which are also applicable for logic errors.

There are two main steps (11 and 13) involved when working to correct either a logically incorrect output or an insufficient clocking field margin across all inputs. Step 11 focuses on adjusting magnet size and spacing (in the same layer). If changes from step 11 do not make the design operational, additional changes are required. This is done in step 13 where the given layout is altered by (a) reorganizing the magnets, and (b) adjusting magnet sizes and spacings. Such adjustments are carried out based on the observations discussed in Sec. III-A. Knowledge of pNML switching behavior is important to avoid a full design space exploration. We now consider a case study.

## IV. 3D Threshold Full Adder Case Study

Here, we present the design of a 3D threshold full adder. We begin with an initial 3D design and then discuss revisions made following the design process illustrated in Fig. 6 to obtain an operational circuit.

The threshold logic form of the full adder function is given in Fig. 5. To decide the layer assignment (step 3 in Fig. 6), we note that $\overline{C_{out}}$ serves as both an output and an input while $SUM$ is simply an output. To ease signal propagation (especially in terms of a pipelined ripple-carry adder design), we place the $SUM$ magnet on a different functional layer from the other four magnets. The size and spacing of each input is chosen according to the TLG expression for both $\overline{C_{out}}$ and $SUM$. Specifically, we set the $\overline{C_{out}}$ magnet to be twice as large as the three input magnets so that its coupling to the $SUM$ magnet is twice as large as those of the other magnets. For both $SUM$ and $\overline{C_{out}}$, Magnets $A$, $B$, and $C_{in}$ must be weighted equally. The $SUM$ magnet is chosen to overlap all the magnets on the lower layer. Fig. 7 illustrates this initial 3D adder design. Following the design process, we simulated the design to see if it is operational. Due to the symmetry of our design, it is only necessary to test three input cases for correctness — 111, 001, and 010 for inputs $A$, $B$ and $C_{in}$. Unfortunately, simulation results showed that this initial design was not operational since condition C2 is violated (step 6).

As the next step (step 7), we examined the $SUM$ magnet for the existence of domain walls. We observed that the input magnets couple anti-ferromagnetically with the $\overline{C_{out}}$ magnet.

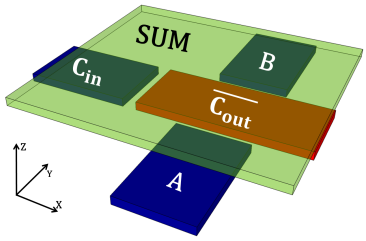


Fig. 7. Initial 3D pNML threshold full adder design. $SUM$ is placed above the three input magnets as well as the $\overline{C_{out}}$ magnetThe $\overline{C_{out}}$ magnet is twice as large as the three input magnets.

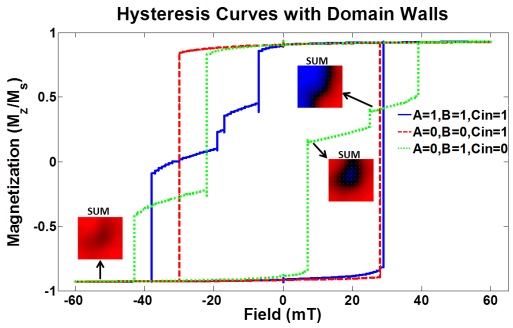


Fig. 8. Hysteresis of $M_z$ of the $SUM$ magnet (normalized to $M_s$) versus the applied clocking field for three input cases. Stable domain walls for input case $A = 0$, $B = 1$, $C_{in} = 0$, and $\overline{C_{out}} = 1$ (solid line) are highlighted. Other input cases are symmetrical to these three.

Thus, the $SUM$ magnet experiences strong in-plane fields, which makes it prone to form a domain wall, as explained in Sec. III-A. Fig. 8 is a simulation result that illustrates this problem. The hysteresis curves depict the applied clocking field necessary to switch the magnetization state of $SUM$. In the figure, the solid line corresponds to input case $A = 0$, $B = 1$, $C_{in} = 0$, and $\overline{C_{out}} = 1$. If the $SUM$ is initially a logic '0', $H^1 > 38mT$ could place it into the correct state. However, this field would make the correct outputs for other combinations to become incorrect (i.e., violate condition C2). From the solid hysteresis curve, one can see that as the magnitude of the clock increases, domain walls are formed at distinct points (i.e., 7 mT and 25 mT), which lead to this higher required clocking field. To remove domain walls, we increased the distance between the $SUM$ magnet and the inputs (step 8). But this reduced F-coupling from the input magnets and lead to incorrect logic functionality.

Following step 13, we revise our adder to the one in Fig. 9a. This design provides two additional benefits. First, we do not have to greatly increase the distance of the $SUM$ magnet from the lower layer in order to avoid the in-plane fields. The $A$, $B$, and $C_{in}$ magnets are uniformly distributed on one side of the $\overline{C_{out}}$ magnet. Thus, we can leverage the in-plane fields to provide an initial magnetic "torque", which results in a lower clocking field magnitude while also avoiding domain walls from opposing in-plane fields.

After simulating the new design, we found that our input cases are logically correct with no domain walls; however, conditional C2 can still not be satisfied (step 10). We now proceed to step 11. Through inspection of input cases, it was observed that the $C_{in}$ magnet is not weighted equally to the $A$ and $B$ magnets. To balance the weight (i.e., the coupling) of the input magnets, we have two options. (1) Reduce the size of the $A$ and $B$ magnets. However, this would reduce their influence on the $\overline{C_{out}}$ magnet. (2) Move the $C_{in}$ magnet to

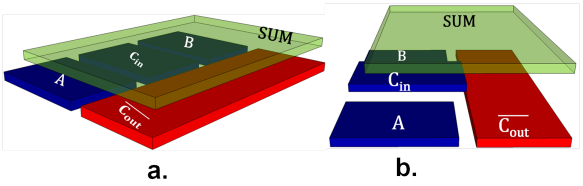


Fig. 9. a. Second 3D pNML threshold full adder design. b. Operational 3D pNML threshold full adder.

a higher functional layer. However, this could also reduce the influence of the $C_{in}$ on the $\overline{C_{out}}$ magnet.

Our solution is a combination of both options (Fig. 9b), which leads to a fully operational (for both $SUM$ and $\overline{C_{out}}$) 3D pNML full adder. To perform a full add, we first apply an oscillating field of 132 mT. This sets the state of $\overline{C_{out}}$ for all possible input combinations. We then apply another oscillating field of 42 mT. This correctly sets the state of $SUM$ for all possible input combinations. (The design functions correctly until the fields exceed 137 mT and 45 mT respectively.) This design consists of 3 functional layers ($SUM$ layer, $C_{in}$ layer and $A/B/\overline{C_{out}}$ layer). Though the $C_{in}$ and $\overline{C_{out}}$ magnet are not on the same layer, 3D routing (see [9]) can be readily employed to facilitate signal propagation.

## V. Discussion

We now compare the design presented above to other adder NML adder designs. We first consider critical path delays. To date, most projections for iNML and pNML adders assume a three majority gate-based adder design (see [20]). Notably, [20] suggests that at least 12 magnet switching events would be required to perform a 1-bit full add with iNML. In comparison, the critical path through the 3D pNML adder requires just 2 magnet switching events. However, the value of $C_{out}$ is calculated after one clock pulse, and the value of Sum is calculated after a second pulse. Per Fig. 2a, each pulse could facilitate two magnet switching events. Because we do not assume anything about the initial magnet state, we must wait two full cycles to guarantee we compute the correct value of $C_{out}$ and Sum. Thus, the delay for a 1-bit 3D adder is essentially 4 magnet switching events. Additionally, [7] reports the experimental demonstration of a three majority gate-based, 2D pNML adder. A clocking requirement of three clock pulses (or 6 magnet switching events) is reported [7]. However, with the design in [7], bit slices cannot be easily concatenated as the $C_{out}$ signal cannot be routed to the $C_{in}$ device in the next bit slice (see schematic in [7]). As such, critical path delays would realistically increase.

In terms of area, we compare our 3D design to a TLG based pNML adder in [8]. In the experiments discussed in [8], the realized adder has a total area of approximately 1.95 $\mu m^2$. However, for this proof-of-concept experiment, magnet sizes were larger, and had a minimum feature size of approximately 150 nm, and a minimum device-to-device spacing of approximately 50 nm. This is three and five times larger (respectively) than the minimum magnet feature size and device-to-device spacings assumed in our simulations. Thus, to make an "apples-to-apples" comparison with respect to area, we scale the area of the design in [8] by a factor of three. A scaling factor of three is used instead of five as (i) magnet area dominates the design in [8], and (ii) scaled spacings are still relatively similar – i.e., 10 nm vs. 17 nm.

Analysis suggests that in addition to having a reduced critical path, our 3D design (130 nm $\times$ 190 nm) has a footprint that is almost 9X smaller than the scaled 2D design above. Note that this comparison puts the 3D design at a significant disadvantage. More specifically, in the 2D design, the $C_{in}$ magnet is surrounded by other magnets (see images in [8]), and additional overhead and/or re-design would be required to route the $C_{out}$ to an identical/adjacent bit slice. Bit slices can be easily concatenated with the 3D approach.

To conclude, we have presented several observations on 3D pNML device interactions. Based on these observations, we have developed a design process for 3D pNML circuits. As long as no single device spans across multiple layers and there is sufficient separation between layers (as is the case with our adder), there is a clear path to fabricating more sophisticated designs. Moreover, interconnect overhead can be reduced. Targeted output devices could be interrogated via MRAM-like read methods. In future work, we will consider error rates/clocking margins in more detail and perform additional analysis with respect to clock energy.

Even though the $C_{out}$ magnet is in a different layer than the $C_{in}$ magnet (per Fig. 9b), simulations show that the $C_{out}$ magnet can correctly set the state of the $C_{in}$ magnet in a concatenated bit slice.

## References


[1] A. Imre *et al.*, "Majority logic gate for magnetic quantum-dot cellular automata," *Science*, vol. 311, no. 5758, pp. 205–208, 2006.

[2] M. T. Niemier *et al.*, "Nanomagnet logic: progress toward system-level integration," *J. of Physics: Cond. Mat.*, vol. 23, no. 49, p. 493202, 2011.

[3] J. Kiermaier *et al.*, "Electrical input structures for nanomagnetic logic devices," *J. of App. Phys.*, vol. 111, no. 7, pp. 07E341–07E341–3, 2012.

[4] S. Liu *et al.*, "A design space exploration of the magnetic-electrical interfaces for nanomagnet logic," *IEEE T. on Nano.*, vol. 12, 2013.

[5] G. Csaba *et al.*, "Field-coupled computing in magnetic multilayers," *Journal of Computational Electronics*, vol. 7, no. 3, pp. 454–457, 2008.

[6] I. Eichwald *et al.*, "Nanomagnetic logic: Error-free, directed signal transmission by an inverter chain," *IEEE T. on Mag.*, vol. 48, 2012.

[7] S. Breitkreutz *et al.*, "Experimental demonstration of a 1-bit full adder in perpendicular nanomagnetic logic," *IEEE T. on Mag.*, vol. 49, 2013.

[8] S. Breitkreutz *et al.*, "1-bit full adder in perpendicular nanomagnetic logic using a novel 5-input majority gate," *Joint European Magnetic Symposium, available: http://www.jems2013.org/usb/*, August 2013.

[9] I. Eichwald *et al.*, "Towards a signal crossing in double-layer nanomagnetic logic," *IEEE T. on Mag.*, vol. 49, no. 7, pp. 4468–4471, 2013.

[10] S. Breitkreutz *et al.*, "Nanomagnetic logic: compact modeling of field-coupled computing devices for system investigations," *Journal of Computational Electronics*, vol. 10, no. 4, pp. 352–359, 2011.

[11] C. Lageweg *et al.*, "A full adder implementation using set based linear threshold gates," in *Electronics, Circuits and Systems, 2002. 9th International Conference on*, vol. 2, 2002, pp. 665–668 vol.2.

[12] M. Becherer *et al.*, "Magnetic ordering of focused-ion-beam structured cobalt-platinum dots for field-coupled computing," *Nanotechnology, IEEE Transactions on*, vol. 7, no. 3, pp. 316–320, 2008.

[13] X. Ju *et al.*, "Nanomagnet logic from partially irradiated co/pt nanomagnets," *IEEE T. on Nano.*, vol. 11, no. 1, pp. 97–104, 2012.

[14] S. Breitkreutz *et al.*, "Nanomagnetic logic: Demonstration of directed signal flow for field-coupled computing devices," in *European Solid-State Device Research Conference*, 2011, pp. 323–326.

[15] X. Ju *et al.*, "Systolic pattern matching hardware with out-of-plane nanomagnet logic devices," *IEEE T. on Nano.*, vol. 12, p. 399, 2013.

[16] M. Niemier *et al.*, "Systolic architectures and applications for nanomagnet logic," in *Silicon Nanoelectronics Workshop*, 2012, pp. 1–2.

[17] M. J. Donahue *et al.*, *OOMMF User's guide, Version 1.0, Interagency Report NISTIR 6367.*

[18] X. Ju *et al.*, "Error analysis of co/pt multilayer based nanomagnetic logic," in *11th IEEE Conf. on Nanotechnology*, 2011, pp. 1034–1037.

[19] O. Hellwig *et al.*, "Domain structure and magnetization reversal of antiferromagnetically coupled perpendicular anisotropy films," *J. of Magnetism and Magnetic Materials*, vol. 319, no. 1-2, pp. 13–55, 2007.

[20] D. Nikonov and I. Young, "Uniform methodology for benchmarking beyond-cmos logic devices," in *Int. Elec. Dev. Meet.*, pp. 25.4.1–25.4.4.