Characterizing Power Delivery Systems with On/Off-Chip Voltage Regulators for Many-Core Processors

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Abstract—**Design of power delivery system has great influence on the power management in many-core processor systems. Moving voltage regulators from off-chip to on-chip gains more and more interest in the power delivery system design, because it is able to provide fast voltage scaling and multiple power domains. Previous works are proposed to implement power efficient on-chip regulators. It is also important to analyze the characteristics of the entire power delivery system to explore the tradeoff between the promising properties and costs of employing on-chip regulators. In this work, we develop an analytical model to evaluate important characteristics of the power delivery system, including on-chip/off-chip voltage regulators and the passive on-chip/on-board parasitic. Compared with SPICE simulations, our model achieves a fast system-level evaluation with comparable accuracy. Based on the model, geometric programming is utilized to find the optimal power efficiency of different architectures of power delivery systems under constraints of output voltage stability and area. Experiments show that compared with the conventional architecture using off-chip regulators, the hybrid one using both on-chip and off-chip voltage regulators achieves 1.0% power efficiency improvement and 68% area reduction of voltage regulators on average. We conclude that the hybrid architecture has potential for high power efficiency and small area at heavy workload, but careful account for the overhead of on-chip regulators is needed.**

I. INTRODUCTION

Due to the power dissipation limitation, many-core processor system becomes promising to improve performance and power efficiency instead of feature size scaling alone. Power delivery system is a key subsystem within it, and voltage regulators are the essential components of a power delivery system. Traditionally regulators are contained in board-level with large inductors or capacitors. However, the costs and sizes of off-chip regulators severely limit their use for multiple power domains. The large inductors and capacitors also slow down their feedback control. Hence, there is an interest in developing fully integrated on-chip voltage regulators [1].

In recent years, there is a surge of interest to implement on-chip integrated voltage regulators [1] [2]. An on-chip regulator can allow the filter components to be integrated entirely on chip or on package, due to its high switching frequency. It is enable to provide fast voltage scaling and multiple on-chip

power domains. However, the potential benefits are tempered by the lower power efficiency from high switching frequency and low-quality inductor, and the increased susceptibility to the load transient response. The design of voltage regulators is difficult due to the wide design space. Modeling and optimization provides an effective method to find the optimal design variables and investigate characteristics of voltage regulators [3] [4]. Previous works focus on the implementation of on-chip voltage regulators. It is also important to characterize the entire power delivery system, including on/off-chip regulators and the passive on-chip/board parasitics, and to explore the tradeoff between the promising characteristics and costs of using on-chip regulators in many-core processor systems.

In this paper, an analytical model of the power delivery system is proposed to investigate important characteristics, e.g. power efficiency and load transient response. It achieves a fast evaluation with comparable accuracy, compared with SPICE simulations. Based on our model, the characteristics of different architectures of power delivery systems are optimized and compared under design constraints. The hybrid architecture shows the potential of high power efficiency and small area, but careful account for the cost of on-chip regulators is needed.

II. MODELING OF POWER DELIVERY SYSTEM

With the development of on-chip voltage regulators, engineers have more choices to build up the customized power delivery systems for many-core processors. On-chip regulators are recommended for power delivery of many-core processors,
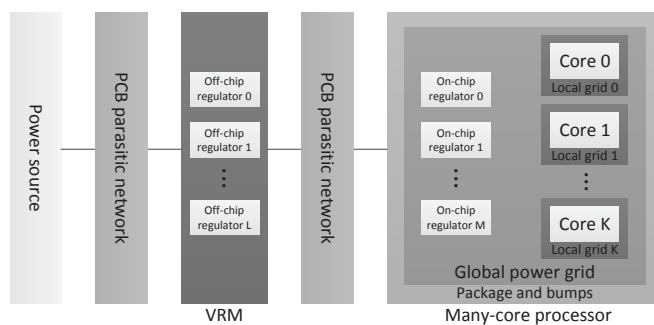

Fig. 1: Overview of a two-stage power delivery system

because they can provide multiple power domains and fast voltage scaling. The conventional design using only off-chip voltage regulators directly steps the power supply voltage down to the core voltage. While a multi-stage power delivery system using both off-chip and on-chip regulators shown in Figure 1 becomes promising. Off-chip regulators perform the initial step-down to an intermediate voltage. The intermediate power supply then drives on-chip regulators to further step down to the core voltage. The analysis and comparison of different power delivery systems will be discussed in Section IV.

Tight steady state and dynamic tolerance requirements set a big challenge for powering high performance processors. Interleaved multi-phase buck converter becomes popular to supply high-current processors [5]. Each phase of the regulator is implemented with fixed switching frequency and pulse width modulation, which eliminates undesirable noise in certain frequency band. The type-III feedback control is adopted. Similar phases of the regulator will be operated in parallel with a common output capacitance shown in Fig. 2. By applying a $360°/N$ phase difference between the adjacent phases, the output ripple can be canceled out while maintaining fast transient response. N is the number of the parallel phases. Because we focus on high performance many-core processors, continuous mode operation of regulators is assumed.

Power efficiency is one of the most important features of regulators, which directly influences the power efficiency of the entire power delivery system. Generally speaking, there are some important kinds of power losses, e.g. switching loss and resistive loss of the power bridge, switching loss of the bridge driver circuit, conductive loss of the inductor, power of the control circuit and static power [6]. The estimation of those power losses in one phase is presented as follows.

$$P_{driver} = (C_L + C_G)V_{driver}^2 f_{sw} \tag{1}$$

$$P_{bridge} = (DR_{ds,p} + (1-D)R_{ds,n})(I_{ind}^2 + \frac{\Delta I_{ind}^2}{12}) \tag{2}$$

$$P_{ind} = R_{ind}(I_{ind}^2 + \frac{\Delta I_{ind}^2}{12}) \tag{3}$$

$$P_{control} = I_{peri}V_{driver} \tag{4}$$

where C_L and C_G is the parasitic load capacitance of the bridge and drivers, and f_{sw} is the switching frequency. V_{driver} is the supply voltage of the drivers and control logic. $R_{ds,n}$ and $R_{ds,n}$ are the on-resistance of the NMOS and PMOS transistor of the bridge, and R_{ind} is the resistance of the inductor. D is the duty ratio of the gate signal. I_{peri} stands for the load current of the control circuit per phase. I_{ind} and ΔI_{ind} are the average and peak-to-peak values of the inductor current. The detailed device models are discussed in Section III for efficient design space exploration . The other variables can be derived according to principles of buck converters.

$$D = \frac{V_{out}}{V_{in}}\frac{R_{ind} + DR_{ds,p} + (1-D)R_{ds,n} + R_{load}}{R_{load}} \tag{5}$$

$$\Delta I_{ind} = \frac{(V_{in} - V_{out})D}{f_{sw}L_{ind}} \tag{6}$$

The direct path loss is neglected, because dead-time control for gating signals usually makes it negligible [7]. Besides the power efficiency, there are other important characteristics, e.g. the area and output voltage stability. Output ripple is one
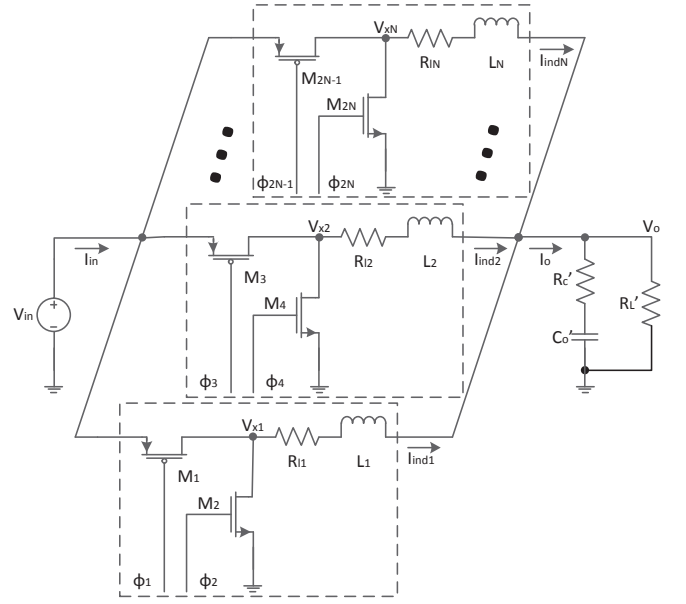

Fig. 2: Circuit schematic of multi-phase buck converters

criterion of the output voltage stability. Assuming that all of the inductor currents flow through the filter capacitor C_{out}, the output ripple decreases due to the interleaving technique [8].

$$\Delta V_{out,ripple} = \frac{\Delta I_{ind}}{8f_{sw}C_{out}}\frac{0.25}{D(1-D)}\frac{1}{N^2} \tag{7}$$

Load transient response is another important criterion to maintain the stability. If a regulator is integrated on-chip, the output voltage drops much more in response to the load current step [1]. This is because the on-chip capacitor is much smaller than off-chip regulators. The voltage drop is derived in Eq. 8 [9]. The worst case voltage drop tends to approach the open-loop value, when the response of the feedback control is sluggish. α is an user-specified empirical factor to bring the open-loop estimation into agreement with the actual voltage drop. It is about 0.6 using the voltage mode feedback control at switching frequencies of hundreds of MHz [2].

$$\Delta V_{out,tr,on} = \alpha \cdot \Delta I_{out,tr} \cdot \sqrt{\frac{L_{ind}}{C_{out}}} \tag{8}$$

In order to characterize the entire power delivery system, we also pay attention to the parasitics of the power delivery network. A ladder RLC network is utilized to capture the parasitics, which consists of PC board, socket, package, and off-chip decoupling capacitors [10] [11]. The parasitics of the power delivery network will be linearly scaled to be consistent with the power consumption of processors.

III. DESIGN OPTIMIZATION OF POWER DELIVERY SYSTEMS AND MODEL VALIDATION

The analytical model of the power delivery system is derived including the voltage regulators and the parasitics of the power delivery network. Because of the wide design space, a method based on geometric programming (GP) is adopted to find the optimal regulator design [3]. Without losing generality, the optimization of the hybrid architecture using on/off-chip regulators shown in Fig. 1 is illustrated.

Algorithm 1 Optimization of the hybrid architecture

Require: workload of power domains, design specs, parameters of device models, intermediate voltage levels

1: minimize $\frac{P_{in}}{P_{out}}$
2: subject to
3: $W_{min,on} \leq W_{pMOS/nMOS,on,ij} \leq W_{max,on}, \forall i,j$
4: $f_{sw,on,min} \leq f_{sw,on,ij} \leq f_{sw,on,max}, \forall i,j$
5: $L_{ind,on,min} \leq L_{ind,on,ij} \leq L_{ind,on,max}, \forall i,j$
6: $\frac{V_{out,ij}}{V_{b,j}} \frac{R_{load,on,ij}+R_{ind,on,ij}+R_{pin,on,ij}+R_{ds,on,ij}}{R_{load,on,ij}} \leq$
   $D_{on,ij}, \forall i,j$
7: $\frac{(V_{b,j}-V_{out,ij})\cdot D_{on,ij}}{f_{sw,on,ij}\cdot L_{ind,on,ij}} = \Delta I_{ind,on,ij}, \forall i,j$
8: $(C_{L,on,ij} + C_{G,on,ij})V_{b,j}^2 f_{sw,on,ij} + (R_{ds,on,ij} + R_{ind,on,ij} + R_{pin,on,ij})(I_{out,ij}^2 + \frac{1}{12}\Delta I_{ind,on,ij}^2) + P_{stat,on,ij} + V_{b,j} \cdot I_{peri,on,ij} \cdot N_{on,ij} + Z_{grid,ij} \cdot I_{out,ij}^2 + V_{out,ij} \cdot I_{out,ij} \leq V_{b,j} \cdot I_{on,ij}, \forall i,j$
9: $\frac{\Delta I_{ind,on,ij}}{8f_{sw,on,ij}C_{out,on,ij}} \frac{0.25V_{b,j}}{D_{on,ij}(V_{b,j}-V_{out,ij})} \frac{1}{N_{on,ij}^3} \leq$
   $V_{ripple,on,max}, \forall i,j$
10: $\alpha_{on} \cdot \Delta I_{out,tr,on,ij} \cdot \sqrt{\frac{L_{ind,on,ij}}{C_{out,on,ij}}} \leq V_{tr,on,max}, \forall i,j$
11: $A_{bridge,on} \sum_i \sum_j (W_{pMOS,on,ij} + W_{nMOS,on,ij}) + A_{peri,on} \sum_i \sum_j N_{on,ij} + A_{ind,on} \sum_i \sum_j L_{ind,on,ij} N_{on,ij}^2 + A_{cap,on} \sum_i \sum_j C_{out,on,ij} \leq A_{on,max}$
12: $\sum_i^{M_j} I_{on,ij} \leq I_{off,j}, \forall j$
13: $W_{min,off} \leq W_{pMOS/nMOS,off,j} \leq W_{max,off}, \forall j$
14: $f_{sw,off,min} \leq f_{sw,off,j} \leq f_{sw,off,max}, \forall j$
15: $L_{ind,off,min} \leq L_{ind,off,j} \leq L_{ind,off,max}, \forall j$
16: $\frac{V_{b,j}}{V_{in}} \frac{R_{load,off,j}+R_{ind,off,j}+R_{ds,off,j}}{R_{load,off,j}} \leq D_{off,j}, \forall j$
17: $\frac{(V_{in}-V_{b,j})\cdot D_{off,j}}{f_{sw,off,j}\cdot L_{ind,off,j}} = \Delta I_{ind,off,j}, \forall j$
18: $(C_{L,off,j}+C_{G,off,j})V_{drvier,off,j}^2 f_{sw,off,j} + (R_{ds,off,j} + R_{ind,off,j})(I_{off,j}^2 + \frac{1}{12}\Delta I_{ind,off,j}^2) + P_{stat,off,j} + V_{driver,off,j} \cdot I_{peri,off,j} \cdot N_{off,j} + (Z_{package} + Z_{PCB}) \cdot I_{off,j}^2 + V_{b,j} \cdot I_{off,j} \leq V_{in} \cdot I_{in,j}, \forall j$
19: $\frac{\Delta I_{ind,off,j}}{8f_{sw,off,j}C_{out,off,j}} \frac{0.25V_{in}}{D_{on,ij}(V_{in}-V_{b,j})} \frac{1}{N_{off,j}^3} \leq$
   $V_{ripple,off,max}, \forall j$
20: $\alpha_{off} \cdot \Delta I_{out,tr,off,j} \cdot \sqrt{\frac{L_{ind,off,j}}{C_{out,off,j}}} \leq V_{tr,off,max}, \forall j$
21: $A_{bridge,off} \sum_j (W_{pMOS,off,j} + W_{nMOS,off,j}) + A_{peri,off} \sum_j N_{off,j} + A_{ind,off} \sum_j L_{ind,off,j} N_{off,j}^2 + A_{cap,off} \sum_j C_{out,off,j} \leq A_{off,max}$
22: $\sum_j \sum_i (V_{out,ij} \cdot I_{out,ij}) = P_{out}$
23: $\sum_j I_{in,j} \cdot V_{in} \leq P_{in}$

A. design optimization of power delivery system

The optimization is conducted to optimize the design parameters and conversion ratios of on/off-chip voltage regulators, provided the supply voltage of the power delivery system V_{in}, the driver voltage V_{driver}, the load distribution of on-chip power domains $V_{out,ij}$ and $I_{out,ij}$, the design specs and the parameters of device models. The assignment of on/off-chip regulators is based the principle of load balance. The design specs includes the maximum output ripples $V_{ripple,on,max}$ and $V_{ripple,off,max}$, the maximum transient voltage drop $V_{tr,on,max}$ and $V_{tr,on,max}$, the area constrain $A_{on,max}$ and

TABLE I: Model comparison between the analytical model and SPICE simulation at 130nm technology.

Vout/Vin (V/V)	R_{load} (Ω)	SPICE Efficiency	Model Efficiency	SPICE V_{ripple} (mV)	Model V_{ripple} (mV)	SPICE V_{tr} (mV)	Model V_{tr} (mV)
1/1.8	0.25	86.4%	87.2%	9.0	8.9	104	100
1/1.8	0.125	86.4%	87.3%	8.3	7.9	100	99
1/2.2	0.25	84.1%	84.7%	1.2	1.3	97	100
1/2.2	0.125	84.5%	85.1%	0.6	0.7	97	100

$A_{off,max}$, and the boundaries of design parameters. In order to apply GP, the device models have to be compatible. Our model leverages the transistor models in [3] and inductor model in [6]. All parameters are found for each process technology by numerical fitting to SPICE simulation data. The drivers for the power bridge is designed to be fan-out of 4.

The optimization of power delivery systems selects not only the design parameters of regulators, but also the conversion ratio in a multi-stage power delivery system. The intermediate voltage level, V_b, tradeoff the power efficiency between the stages, but it is incompatible with GP. Given a combination of V_b, the power efficiency of the power delivery system will be optimized using GP shown in Alg. 1. The formulation for optimizing on-chip regulators are described in Lines 3-11 referring to Section II. The area is constrained in Line 11, where $A_{bridge,on}$, $A_{peri,on}$, $A_{ind,on}$ and $A_{cap,on}$ are the unit area of power bridge and drivers, control logic, inductor and capacitor. The formulation for optimizing off-chip regulators is similar in Lines 12-21. The optimal power efficiency under different V_b will be derived to find the highest power efficiency of the system and the corresponding conversion ratios.

B. analytical model validation

The analytical model will be compared with SPICE simulations to evaluate the accuracy of the optimized results. The parameters of the transistor, inductor and capacitor model are discussed in Section IV. According to the specs in Table I, we optimize the design parameters of a two-phase interleaved buck converters using 130nm technology [12]. The SPICE model is built up with the optimized design parameters. Table I shows a comparison between SPICE simulation and our model in terms of the power efficiency, output ripple and transient voltage drop due to load step of 50% load current. The optimized results based on the analytical model are well matched with SPICE simulations within 5% difference.

IV. QUANTITATIVE ANALYSIS AND COMPARISON OF DIFFERENT POWER DELIVERY SYSTEMS

The analytical model provides a fast and accurate evaluation of the characteristics of power delivery systems. The evaluation and comparison of different architectures will be conducted to explore the tradeoff of using on-chip regulators.

The transistor models of power bridge of off-chip regulators are estimated according to [13], and that of control logic and drivers uses $1.5\mu m$ process [12]. The transistors of on-chip regulators are implemented using $130nm$ process [12]. The parameters of the inductor and capacitor of on-chip regulators
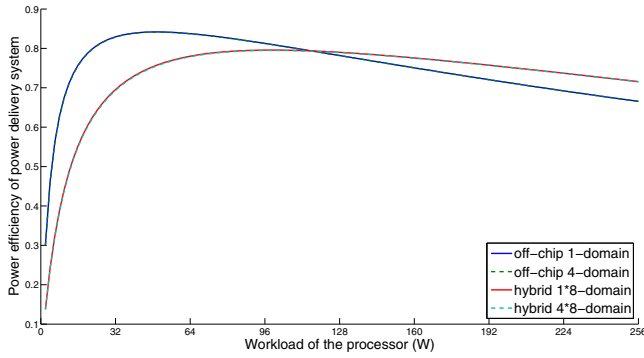
Fig. 3: Power efficiency curve of different architectures of power delivery systems optimized at workload of 128W

Fig. 4: Design tradeoff between power efficiency and area for different architecture

are derived based on [2]. The bulky inductor and capacitor of off-chip regulators is estimated from commercial products. The overhead of the control logic is estimated [2] [3].

The core voltages and currents of high performance processors are approaching 1V and 130A [5]. As a case study, the power delivery system is designed to support a 64-core homogeneous processor with 128W average power consumption, stepping down from 12V to 1V. The voltage of the drivers of off-chip regulators is 5V. The parasitic resistance of on-chip power grid is $0.1m\Omega$ for the whole processor, and that of the package and PCB trace are $1.3m\Omega$ and $0.1m\Omega$ [10]. The maximum output ripple is 10% of its output voltage. The maximum transient voltage drop is also 10%, due to a load step of 50% load current [2]. The maximum area of on-chip and off-chip regulators is $110mm^2$ and $2700mm^2$ [14].

The design parameters of different architectures are optimized at the workload of 128W to maximize the power efficiency under the constraints of output ripple, transient voltage drop and area. Different configurations of the same architecture will also be evaluated, e.g. the hybrid architecture with 1 off-chip regulator and 8 on-chip regulators per off-chip regulator, labeled as $hybrid\ 1 * 8 - domain$. The power efficiency curves of the optimized power delivery systems are shown in Fig. 3. The hybrid architecture achieves a flat power efficiency curve within a large range of workload.

The conduction loss from the package and PCB plays an important role. It increases quadratically with the increase of workload, and can not be alleviated by off-chip regulators. While, the hybrid architecture decreases the loss by reducing the current flowing off-chip, and improves the power efficiency by decreasing the conversion ratio of on-chip regulators. Compared with conventional architecture, the hybrid one achieves 1.0% power efficiency improvement and 68% area reduction of voltage regulators on average at 128W workload. The power efficiency of different configurations of the same architecture is similar, because it supports a homogeneous processor.

The hybrid architecture also alleviates the design requirements of off-chip regulators by decreasing its load [14]. Fig. 4 shows the minimum area of regulators in different architectures, with different power efficiency constraints at 128W workload. Compared with the conventional architecture,
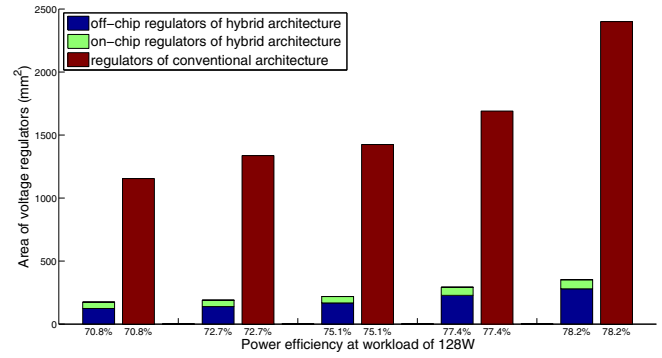
the area of regulators in hybrid architecture decreases from 82% to 85% with tighter requirement of power efficiency.

V. CONCLUSION

In this paper, an analytical model is proposed to fast evaluate important characteristics of power delivery system with comparable accuracy. Based on our model, geometric programming is used to optimize the power efficiency of different architectures, and to explore the tradeoff between the promising characteristics and costs of utilizing on-chip regulators in many-core processor systems. It is concluded that the hybrid architecture using both on/off-chip regulators has potential for high power efficiency and small area, but careful account of the overhead of on-chip regulators is needed.

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