Package Geometric Aware Thermal Analysis by Infrared-Radiation Thermal Images

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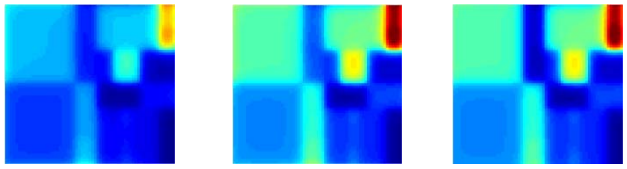
***Abstract*—Since packages affect the amount of heat transfer, it is important to include package and heat sink in thermal analysis. In this paper, we study the full-chip thermal response with different packages. We first discuss the difficulties of obtaining accurate package models for simulation. To facilitate a designer to perform thermal simulation with different packages, we propose to use a matrix called the package-transfer matrix which can transform a temperature profile of one package to another temperature profile of the desired package. To estimate and verify a package-transfer matrix, we propose an efficient method which uses Infrared Radiation (IR) images from two carefully design test chips with PBGA packages. Our experimental results show that the default package model CBGA in HotSpot can be accurately transferred to any other package through the package-transfer matrix.**

I. Introduction

In high density integrated circuits, the total power as well as power density can increase dramatically. The power consumption is converted into heat which increases the temperature of integrated circuits. High temperature degrades the performance or causes reliability problems in a chip. Therefore, it is important to accurately analyze thermal behavior, with which appropriate cooling techniques can be determined.

Accurate thermal analysis for a chip requires the knowledge of what package and heat sink will be adopted, because they affect the capability of heat transfer [1]. The package with low thermal resistance quickly transfers the heat generated by the chip while the high thermal resistant package leads to the heat accumulated in the chip.

Despite the need in adopting the package into thermal simulation, there are two major difficulties. First, most thermal analysis tools for chip designers provide very few choices of package types. For example, a tool such as HotSpot [2], only provides one model, the Ceramic Ball Grid Array (CBGA) package. Due to the scarcity of package models, most published papers analyze the chip thermal behavior using the default setting of HotSpot (that is the CBGA package) and then optimize their designs with the thermal behavior. Since the package can alter heat transfer, the results can be very different depending on which packages are applied. In addition, accurate modeling of a package thermal conductance is very difficult due to the compound materials of a package and the complicated geometry of metal lines [3, 5].



(a) ev6 with CBGA (b) ev6 with PBGA (c) ev6 with *package transfer matrix*

Fig. 1. Transferring result of CBGA to PBGA package

On the other hand, it has been shown that a high-speed infrared radiation (IR) image can provide accurate temperature profiles of a manufactured chip with the desired package. Since IR can be applied only after a chip is manufactured, an IR image cannot be obtained in the design stage in which the architecture trade-off or cooling device trade-off is determined.

Because simulation with accurate package models is difficult, we propose a novel methodology in this paper allowing designers to obtain temperature profiles whose qualities are similar to those of IR images in the design stage. The proposed methodology builds a matrix, called the *package-transfer matrix* (*PT-matrix*) for every two packages. The *PT-matrix* of two packages can transfer a temperature profile using one package to a temperature profile using the other package. As a result, a designer can simulate a chip using the default package model such as CBGA in HotSpot and then translates the temperature profile of the default package to the other desired package available using the *PT-matrix*. For example, Fig. 1 (a) shows the temperature profile with the default CBGA package by HotSpot, and Fig. 1 (b) shows the temperature profile of the same design with *Plastic Ball Grid Array (PBGA)* package. Fig. 1 (c) shows the result of translating Fig. 1 (a) by our *PT-matrix*.

The contributions of this paper are summarized as follows.

- We propose a novel methodology which allows designers to translate the temperature profiles between two packages. With this methodology, a designer can translate any temperature profile of one package to the other package.
- We develop a special matrix, called the *package-transfer matrix (PT-matrix)* to perform translations. We also show that the *PT-matrix* has a special property which allows us to approximate the *PT-matrix* efficiently.
- We carefully design two thermal test chips with PBGA package. The special design allows us to accurately control and estimate the power consumption on each module. Through the use of high speed IR image of thermal test chips, we can obtain a *PT-matrix* by one test chip and then verify our methodology by the other one. The experimental results show that the *PT-matrix* can accurately transfer the simulated temperature profile with CBGA package to the temperature profile with PBGA package, with only 1.04% of the maximum temperature error.
- Our experiments show that even when manufacturing process and size of chips are different, the proposed methodology still can provide highly accurate simulated temperature profiles.

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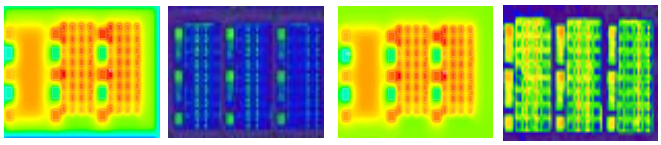
The rest of this paper is organized as follows. In section II, we first introduce the problem of how a package affects a temperature profile, and then explain the package-chip thermal model adopted in this paper. In section III, we formulate the problem and the challenges for package-chip simulation. In section IV, we describe how to obtain a *PT-matrix*. Then we summarize overall PT-matrix application and verification in section V. The experimental results are shown in section VI. Section VII presents our conclusion.

II. PRELIMINARIES

A. Package-Induced Temperature Profile

Thermal simulation of a chip needs to take the package effect into consideration because a package can influence the thermal conductivity at the boundary between the edge of the die and the package. As a result, the thermal conductivity for a spreader would be 188 W/mK for copper and 301 W/mK [6] for alloy.

The widely used standard for modeling temperature profiles of a board level system is JEDEC JESD 51-14 standard [6]. The standard describes the construction methodology of identifying the package resistances. The diverging points of the structure functions or the derivatives of the measured transients in JEDEC JESD 51-14 standard can provide reproducible results at critical points in the whole system including the die, the package, the heat sink, and the PCB substrate.



(a) Simulation (b) IR image (c) Simulation (d) IR image

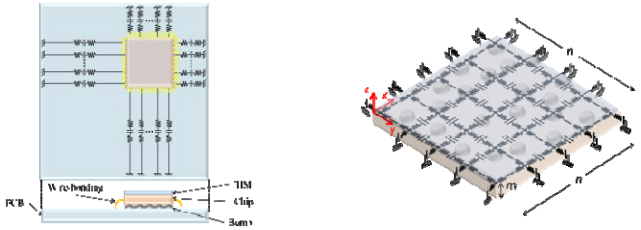
Fig. 2. Simulation and IR images of different package types

In the JEDEC JESD 51-14 thermal model for a board level system, the actual package geometry is neglected; only the volume of the package and the coverage area of the chip are considered [6]. To apply this model to the chip level thermal analysis, several issues should be considered. First, the boundary conditions are very difficult to set up. Moreover, the diverging point is hard to find when the cooling surface area is significantly larger than the chip. Therefore, this model is only suitable for the package with a uniform capability of thermal dissipation.

For example, Fig. 2 (a), (c) show that the temperature profiles of a chip with two different packages by using a traditional package model which is constructed of only a few thermal resistors. Although the chip is wrapped in different kinds of packages, the simulated temperature profiles are quite similar. Conversely, Fig. 2 (b) and (d) show very different IR images of the same chip with two different packages when using an accurate high-speed IR machine. The results show that a traditional package model cannot accurately model package thermal conductance.

B. Thermal Model of a Chip with package

To enhance the accuracy of the JEDEC JESD 51-14 thermal model for the chip, we add additional thermal resistors, called *peripheral thermal resistors*. Fig. 3 presents the package model with different peripheral thermal resistors at peripheral chip nodes. A peripheral thermal resistor is used to model the thermal resistance between a peripheral node at chip boundary and a node at package boundary. Therefore, a peripheral thermal resistor varies according to the location of a chip in package as shown in Fig. 3(a). By adding several peripheral thermal resistors, our package thermal model has much better accuracy than JEDEC JESD 51-14 when dealing with a package having non-uniform geometry. We note that non-uniform geometry of a package is quite common because most chips are not placed at the central area of their packages. Since the distances from the chip center to the package edges are different, the thermal resistors of the package at the peripheral nodes are not the same.



(a) Top and side view of a package-chip (b) The package model of a chip

Fig. 3. The package model with non-uniform impedance of package geometry

Given the package model in Fig. 3, we can use the duality of electrical-thermal relationship to solve the steady-state thermal circuit by *Kirchhoff's Circuit Laws (KCL,) Kirchhoff's Voltage Law (KVL,)* and *Branch Constitutive Equations (BCE.)* We can obtain the following matrix representation:

$$\boldsymbol{A} * \boldsymbol{T} = \boldsymbol{P} \qquad \text{EQ (1)}$$

Since there are N grid nodes in the package model of a chip (where N = n × n shown in Fig. 3), vector P and T in EQ (1) have N elements to represent the system power and temperature profiles, respectively. Meanwhile, A is an N × N thermal conductance matrix of which elements represent the meshed thermal resistors of the chip with package.

III. PROBLEM DESCRIPTION

Let us consider two different packages pkg_1 and pkg_2 with the same size. Also, let T_{pkg1} (T_{pkg2}) be the temperature profile of a die. For ease of understanding, one can assume pkg_1 is the CBGA package defined by the HotSpot tool. T_{pkg1} is the simulated temperature profile of the die wrapped in the CBGA. A temperature profile T_{pkg1} can be obtained by simulating a power profile in HotSpot through EQ (1).

We define a matrix called the *package-transfer matrix (PT-matrix)* between two packages satisfying the following equation.

$$\boldsymbol{T_{pkg2}} = \boldsymbol{PT} * \boldsymbol{T_{pkg1}} \qquad \text{EQ (2)}$$

From EQ(2), we can use *PT-matrix* and the temperature profile of any chip with pkg_1 to derive the corresponding temperature profile of the same chip with pkg_2. In general, *PT-matrix PT* in EQ(2) is strongly related to the material and structural properties of a die and package but is weakly related to the design in the die. It is because that the wires and transistors in a die occupy a relatively low volume fraction of a system comprising a die and package. Therefore the thickness and material of the system dominate the equivalent thermal property. In other words, the thermal resistance and capacitance of a system comprising a die and package are almost independent to the topologies of wires and transistors in the design of the die [7]. As a result, the *PT-matrix* can be applied to a die and package which has the same material and structural properties, the die of which can implement any design. Therefore, the *PT-matrix* of specific two package types can be applied to general chip designs. We describe how this special characteristic works in Section IV A.

Because there are N^2 entries in a *PT-matrix*, from EQ (2), we can solve all N^2 entries of *PT-matrix* as long as we can obtain N authentic temperature profiles of T_{pkg1} and T_{pkg2}. Since IR images are known to have accurate temperature profiles, in this paper, we intend to use IR images of T_{pkg2} and the corresponding simulated temperature profiles of T_{pkg1} to derive *PT-matrix*. The reason for not using the IR image for

T_{pkg1} is that *PT-matrix* will be adopted later in the design stage where T_{pkg1} is obtained from simulation.

There are two challenges in the above procedure to derive *PT-matrix*, in which we use the IR image of a test chip with pkg_2 and the corresponding simulated temperature profile with pkg_1. First, we need to design a special test chip which allows us to feed the same power profile into both the simulator and the test chip. We describe how the test chip is designed in Section VI. Secondly, obtaining N steady-state temperature profiles is very time-consuming and impractical in the current IR measurement environment. For example, each IR image may take 1 minute to heat the package to a specific steady-state temperature, and the other 30 minutes to cool down the whole system to room temperature. Therefore, even if we assume the test chip is meshed into only a 64^2 ($64 \times 64 = n \times n$) grid of nodes, we would have to prepare 64^4 ($64^2 \times 64^2 = N \times N$) proper power profiles for obtaining 64^2 steady-state IR images. That means the repeated thermal cycles could take about 2048 hours (about 3 months). However, when our proposed *PT-matrix* is applied, the whole procedure can be totally completed in 9 hours (including preparation procedure).

IV. Efficient Method of Aproprimating a Package-Transfer Matrix

In this section, we present an efficient methodology to accurately approximate a *PT-matrix*. We first show that many elements in a *PT-matrix* are zero. This special characteristic greatly reduces the efforts of obtaining a *PT-matrix*. Then, for the rest of non-zero elements, we describe a very fast method to estimate the values.

A. The Special Characterisitc of a PT-matrix

Before describing the special characteristic of a *PT-matrix*, we categorize the grid nodes in a chip into two types: 1) an edge node, and 2) a non-edge node. An edge node is defined as a node connected to the package; otherwise, a node is called a non-edge node. For example in Fig. 4, the edge nodes are the blue nodes while the non-edge nodes are those nodes in red. As shown in the Fig., there are 25 grid nodes, and 16 of those are edges nodes. In this example, the dimensions of the vectors T_{pkg1} and T_{pkg2} are 25×1 while the dimension of the *PT-matrix* is 25×25.

Let node s be a grid node. $T_{pkg2}(s)$ can be expressed as $T_{pkg2}(s) = \sum_{t=1}^{\#nodes} PT(s,t)T_{pkg1}(t)$ from EQ (2). This equation expresses that the temperature of grid node s in package pkg_2 is a linear combination of temperatures of all nodes in package pkg_1. We will show that only temperatures of edge nodes in package pkg_1 are needed to compute the temperature of node s in package pkg_2.

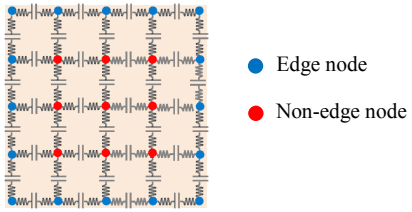


Fig. 4. Edge and non-edge nodes in the grid of a chip

Theorem 1: The element *PT(s, t)* in a *PT-matrix* is zero if grid node t is a non-edge node and grid node s is not equal to grid node t.

Proof: Let us consider that a power profile P is applied to two identical chips with two different packages pkg_1 and pkg_2 and the resulting temperature profiles are T_{pkg1} and T_{pkg2}. We have the following equations:

$$\boldsymbol{A_{pkg2} * T_{pkg2} = A_{pkg1} * T_{pkg1} = P} \qquad \text{EQ (3)}$$

where A_{pkg1} and A_{pkg2} are conductance matrices of the two identical chips with pkg_1 and pkg_2, respectively. As a result, the difference between A_{pkg1} and A_{pkg2} is the peripheral thermal impedance of the packages. Note that the peripheral impedance is located at the principal diagonals of matrices A_{pkg1} and A_{pkg2}. Therefore, we have the following relationship:

$$\boldsymbol{A_{pkg1} = A_{pkg2} + D} \qquad \text{EQ (4)}$$

where D is a diagonal matrix with at most N non-zero elements representing all the heat transfer characteristics of packages, heat sinks and heat spreaders.

Then, we substitute EQ (4) into EQ (3) to eliminate A_{pkg1}:

$$T_{pkg2} = A_{pkg2}^{-1} * (A_{pkg2} + D) * T_{pkg1}$$

$$T_{pkg2} = (I + A_{pkg2}^{-1} * D) * T_{pkg1} \qquad \text{EQ (5)}$$

Hence, the *PT-matrix PT* can be derived as follows:

$$\boldsymbol{PT = I + A_{pkg2}^{-1} * D} \qquad \text{EQ (6)}$$

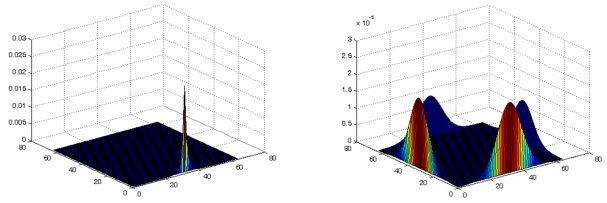
From EQ (6), we can find that the *PT-matrix PT* is related only to the material and structural properties, A_{pkg2} and D. Furthermore, the element *PT(s, t)* in a *PT-matrix* can be obtained by following equation:

$$\boldsymbol{PT(s,t) = I(s,t) + \sum_{i=1}^{\#nodes} A_{pkg2}^{-1}(s,i) * D(i,t)} \qquad \text{EQ (7)}$$

If grid node t is a non-edge node, then *D(i, t)* is zero for all i. As a result, the $\sum_{i=1}^{\#nodes} A_{pkg2}^{-1}(s,i) * D(i,t)$ term in EQ (7) is zero. Consequently, *PT(s, t)* can be expressed as follows:

$$\boldsymbol{PT(s,t) = \begin{cases} I(s,t) = 1, & s = t \\ 0, & s \neq t \end{cases}} \qquad \text{EQ (8)}$$

where grid node t is a non-edge node. ■



(a) Grid node (32, 1) 32th row of *PT-matrix*

(b) Grid node (32, 32) 2016th row of *PT-matrix*

Fig. 5. Plotting the row of *PT-matrix* in a 64×64 matrix

For example in Fig. 5, the chip is meshed into a 64 × 64 grid of nodes, and the corresponding *PT-matrix* is a 4096 × 4096 matrix. The 4096 elements in s^{th} row of the *PT-matrix* represent the relationship between grid node s and others. For example, the temperature difference of T_{pkg1} and T_{pkg2} at the grid node s can be obtained through the s^{th} row of a *PT-matrix* by the following equation:

$$T_{pkg2}(s) = PT(s,1)T_{pkg1}(1) + PT(s,2)T_{pkg1}(2) + \cdots + PT(s,4096)T_{pkg1}(4096) \qquad \text{EQ (9)}$$

To explain the characteristic of *PT-matrix* more clearly, we take the s^{th} row plot of a *PT-matrix* in a 64 × 64 grid for example. Fig. 5 shows that the value of $\sum_{i=1}^{\#nodes} A_{pkg2}^{-1}(s,i) * D(i,t)$ in EQ (7) can be calculated and plotted at the z-axis when i is 4096. Fig. 5 (a) provides the 32th row in a *PT-matrix* which represents the relationship between grid node (32, 1) and other nodes in the chip. By the same concept, we also plot the 2016th row of a *PT-matrix* in Fig. 5 (b), which represents

the relationship between grid node (32, 32) and other nodes in the chip. It can be found from s^{th} row plot that the value of $\sum_{i=1}^{\#nodes} A_{pkg2}^{-1}(s,i) * D(i,t)$ in EQ (7) is zero if grid node t is a non-edge node.

Consequently, through Theorem 1, we can reduce the complexity of establishing a *PT-matrix* greatly by ignoring the elements with zero and exactly one values. In the next section, we further propose an approach to obtain the other elements in a *PT-matrix*.

B. The Approximation of a PT-matrix

In this section, for those non-zero elements in a *PT-matrix*, we propose an approximation methodology to obtain those values. We will show that the *PT-matrix* can be approximated by utilizing only one temperature profile of a chip.

Our approximation methodology requires the use of the heat equation with the solution by Green's function. In the heat equation, the temperature profile is governed by the following thermal diffusion equation:

$$\boldsymbol{\rho C_p \frac{\partial T(x,y,z,t)}{\partial t}} = \boldsymbol{\nabla \cdot [k(x,y,z,T)\nabla T(x,y,z,t)] + g(x,y,z,t)} \quad \text{EQ (10)}$$

where T is the temperature (°C), C_p is the specific heat (J/kg·°C), ρ is the density of the material (kg/m³), k is the thermal conductivity (W/(m·°C)), and g is the power density per unit volume (W/m³). In general, the silicon chip is relatively much thinner than the total device which includes the package, therefore g can be reasonably assumed to be zero. In addition, since we focus on the steady state temperature profile, the time variant term can be removed.

V. EXPERIMENTS

In this section, we first describe the design of the two thermal test chips and the IR camera in our experiment in Section V.A. Then, in Section V.B, we show the experimental results of transferred temperature profiles by adopting the *PT-matrix* of the thermal test chip, and we also verify the results with the measured IR-images.

A. Thermal Test Chips and Infrared Radiation Camera

We describe the design principles and the specifications of the two thermal test chips. A thermal test chip in our methodology must satisfy two requirements. First, to feed the same power profile into both a test chip and the simulation model, we need to accurately estimate the power consumption of each module in the test chip. Secondly, in a test chip, we should have the ability to create different locations of hotspots. Therefore, the two thermal test chips are designed in the way that we can independently control the power consumption of each active component.

1) Standard Thermal Test Chip for PT-matrix Establishment

The first test chip is called *Standard Thermal Test Chip (STTC)*. This chip is fabricated by TSMC in 0.18µm 1P4M mixed-mode process technologies, and the chip size is 5000µm × 5000µm. The package of this chip adopts 256-pin PBGA. The bottom of the chip is covered by the package glue.

2) Power Thermal Test Chip for PT-matrix Verification

To verify the proposed *PT-matrix*, we design the other thermal test chip, which is named *Power Thermal Test Chip (PTTC)*. The package of this chip uses PBGA as well. In order to show the feasibility of the proposed *PT-matrix*, the size of PTTC is 873µm × 873µm, which is much smaller than that of STTC. Due to a smaller size, this PTTC has higher temperature than the previous STTC.

B. Package-Tramsfer Matrix Establishment and Package-Chip Simulation

Table 1 provides detail analysis of our experimental results. From the table, the maximum error is only 1.04%. The experimental results show that our *PT-matrix* can accurately transfer a simulated temperature profile of one package to the corresponding temperature profile of the other package.

Table 1. Experimental results

Name	Measured PBGA by IR Camera		Simulated PBGA by *PT matrix*		Max error	Avg. error
	Max Temp.	Min Temp.	Max Temp.	Min Temp.		
H1	104.8	100.9	105.8	101.8	0.95%	0.89%
H2	103.5	100.1	104.5	101.0	0.97%	0.90%
H3	104.3	100.3	105.3	101.2	0.96%	0.90%
H4	105.5	101.2	106.6	102.1	1.04%	0.89%
H5	101.6	96.3	102.6	97.1	0.98%	0.83%
H6	100.8	95.9	101.7	96.7	0.89%	0.83%
H7	102.3	97.2	103.3	98.0	0.98%	0.82%

VI. CONCLUSION

In this paper, we propose a novel methodology which allows designers to simulate chips using a default package model and translate to the other desired package by applying the *PT-matrix*. By using a special property of the *PT-matrix* of each package, we can obtain it by utilizing at least 1 steady-state temperature profile. The experimental results show that we can use the proposed *PT-matrix* to transfer the default package model CBGA in HotSpot 5.0 to other packages quickly and precisely. In addition, we further design and realize the thermal test chips with diverse power sources to accurately obtain temperature profiles of a variety of package models for obtaining a corresponding *PT-matrix*. As a result, the experiments show that even when manufacturing process and size of chips are different, the proposed methodology still can provide highly accurate simulated temperature profiles.

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