A Novel Low Power 11-bit Hybrid ADC using Flash and Delay Line Architectures

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***Abstract*—This paper presents a novel low power 11-bit hybrid ADC using flash and delay line architectures, where a 4-bit flash ADC is followed by a 7-bit delay-line ADC. This hybrid ADC inherits accuracy and power efficiency from flash ADCs and delay-line ADCs, respectively. Also, in order to reduce the power of the first stage flash ADC, a power-saving technique is adopted by biasing the DC tail current of the pre-amplifiers at 5μA instead of the operational current, 47μA in stand-by mode. The hybrid ADC was designed and simulated in a commercial 65nm process. With 1.1 V supply and 100 MS/s, the ADC achieves an SNDR of 60 dB and consumes 1.6 mW, which results in a figure of merit (FOM) of 19.4 fJ/conversion-step without any calibration technique. Also, Monte Carlo simulations are performed with a 3σ device mismatch for the SNDR estimation, and the SNDR is observed to be better than 58.5 dB.**

Keywords - Analog-to-digital converter (ADC), delay line ADC, flash ADC, hybrid ADC

I. Introduction

Analog-to-digital converters (ADCs) are widely used in many applications, such as high-definition video systems, mobile communication devices, and local/wide area network equipment. High-resolution, high-speed and low power analog-to-digital converters are required to meet stringent demands for resolution, speed, and power-efficiency.

However, with the continued improvement of integrated circuit fabrication technology, the deep submicron regime comes with various complex effects which impede analog circuit scaling [1], [2]. In the literature, voltage-based ADCs, which includes flash, pipeline and successive approximation (SAR) ADCs have been widely studied for various applications [3]–[11]. However, with advances in process technology, voltage-based ADCs cannot be scaled down in terms of power and speed as can digital circuits [12]. Flash ADCs usually use small feature sizes to reduce the power consumption with a higher sampling rate. However, small size devices have the mismatch issue among components due to process variations. On the other hand, SAR ADCs need to utilize the time-interleaved technique to achieve a high sampling rate, where a calibration technique is needed to eliminate the mismatch among the parallel paths. Therefore, the voltage-based ADCs cannot be scaled as well as digital circuits when the process features shrink.

Time-domain analog-to-digital conversion techniques, which include the voltage-to-time-to-digital approach and the voltage-to-delay-to-digital approach, have recently become attractive, especially for deep submicron technologies [1], [2], [12]. The voltage-to-time-to-digital conversion utilizes a voltage-to-time converter and a time-to-digital converter (TDC) to digitize the input signal. On the other hand, the voltage-to-delay-to-digital scheme controls the delay of buffers instead of the time window. The input voltage is digitized by the number of delay cells that the signal passes through in a fixed time window T. In this paper, the delay line ADC used is a voltage-to-delay-to-digital ADC, shown in Figure 1. Generally, time-domain ADCs receive advantages from advances in fabrication technology. A GHz sampling rate can be easily derived [2], [12]. However, non-linearity is still an issue, so that the resolution is hardly more than 4 bits with a hundred MHz sampling rate.

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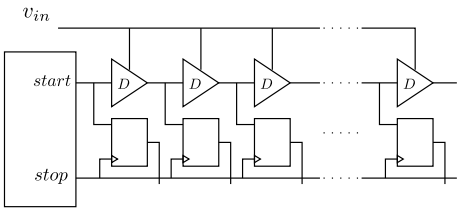

Fig. 1: The diagram of voltage-to-delay-to-digital ADCs.

In this paper, we propose a novel low power 11-bit hybrid ADC architecture, where a 4-bit flash ADC is followed by a 7-bit delay line ADC. In order to reduce the power of the first stage flash ADC, a power-saving technique is adopted by biasing the DC tail current of the pre-amplifiers at 5μA instead of the operational current, 47μA in stand-by mode. In the second stage delay line ADC, the delay cell is the dual-input delay cell (DIDC), and the delay line is a weight-adjusted DIDC chain, where a constant delay can be derived starting from the second delay cell to improve the linearity of the delay-line ADC. Without any calibration, the SNR of the delay line ADC is 28.7 dB, and the SFDR = 29.0 dB.

In our experiments, we present an 11-bit hybrid ADC simulated in a commercial 65-nm CMOS process. At 1.1-V supply and 100 MS/s, the ADC achieves a signal-to-noise-plus-distortion ratio (SNDR) of 60.0 dB and consumes 1.6 mW, which results in a figure of merit (FOM) of 19.4 fJ/conversion-step, which is competitive with other state-of-the-art ADCs. Also, Monte Carlo simulations are performed with a 3σ device mismatch for the SNDR estimation, and the results show that the SNDR is better than 58.5 dB. Therefore, the proposed ADC inherits accuracy and power efficiency from the flash ADC and the delay-line ADC, respectively. These inherited advantages strongly support the scalability of the proposed ADC to provide better performance with low power in further scaled fabrication processes.

The remainder of this paper is organized as follows. Section II introduces our hybrid ADC architecture. Section III discusses the noise shaping of the hybrid ADC. The proposed implementation is described in Section IV. Section V gives the simulation results. Finally, the concluding remarks are made in Section VI.

II. Hybrid ADC architecture

Figure 2 shows the diagram of the hybrid ADC, where a 4-bit flash ADC is followed by a 7-bit delay-line ADC. In the first stage, the 4-bit flash ADC quantizes the input, v_{in} to a 4 bit digital result,

x_1 and then the 4-bit digital-to-analog converter (DAC) converts x_1 to an analog signal, v_1, where $v_1 = x_1 = v_{in} + e_1$, and e_1 is the quantization noise of the 4-bit flash ADC. Let d_1 denote the digital output corresponding to x_1, where $d_1 \in \{0, 1, 2, ..., 15\}$. Then, $x_1 = d_1/16 \times V_{FS}$ where $V_{FS} = \max(v_{in}) - \min(v_{in})$. Next, between the first stage and the second stage, a subtracter implemented by a switched-capacitor circuit generates the residue of the flash ADC, $v_r = v_{in} - v_1$, and amplifies v_r by 8X. In the second stage, the 7-bit delay-line ADC receives the amplified residue, v'_{in} from the first stage flash ADC, and quantizes v'_{in} to x_2. Furthermore, x_2 is divided by 8. Finally, x_1 and $x'_2 = x_2/8$ are combined into the overall output of the hybrid ADC, x_{out}.

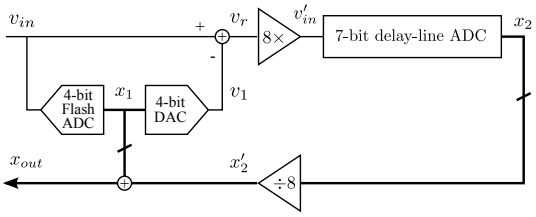

Fig. 2: The hybrid ADC architecture.

Also, x_2 is the quantization result of the delay line ADC but not the number of delay cells the signal passes though in a given time T, N_T. The relation between x_2 and N_T is $x_2 = \frac{N_T}{m+1} \times \frac{V_{FS}}{2}$ where $m = N_T(\max(v_{in})) - N_T(\min(v_{in}))$ and $V_{FS} = \max(v_{in}) - \min(v_{in})$. Thus, we can derive $x_{out} = x_1 + x_2/8 = \frac{d_1}{16} \times V_{FS} + (\frac{N_T}{m+1} \times \frac{V_{FS}}{2})/8$. For simplicity of implementation, the overall digital output, d_{out}, is simplified to $(m+1)d_1 + N_T$. Note that $m = 41$ in the simulation.

III. Noise Shaping of the Hybrid ADC

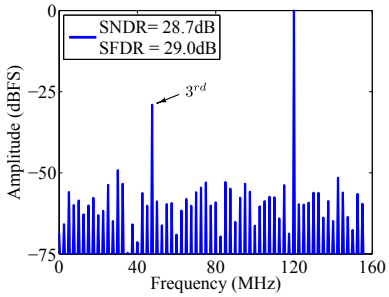

Fig. 3: The spectrum of a 7 bit delay ADC.

To demonstrate the noise shaping of the hybrid ADC, we only consider the third harmonic distortion introduced by the second stage delay-line ADC, since Figure 3 also shows that the third harmonic distortion of the delay line ADC limits the overall resolution, while the others are under the noise floor. For simplicity of analysis, we assume no gain error in the delay-line ADC and other components in the hybrid ADC are ideal. Thus, the quantization result of the delay line ADC, x_2 can be simplified as follows.

$$x_2(v_{in}) = v_{in} + b_3 v_{in}^3 + e_2$$

Note that the even terms of harmonic distortions can be easily cancelled in a differential circuit. In Figure 2, we know that the input of the delay-line ADC, $v'_{in} = -8e_1$. Thus, the quantization result, x_2 can be written as follows.

$$x_2(v'_{in}) = -8e_1 - 8^3 b_3 e_1^3 + e_2$$

Then, the overall output, x_{out} can be derived as follows.

$$\begin{aligned} x_{out}(v_{in}) &= v_{in} - 8^2 b_3 e_1^3 + e_2/8. \\ &= v_{in} - 4 \times 8^2 \times \text{HD3} \times e_1^3 + e_2/8 \end{aligned}$$

where HD3 = $\frac{1}{4} \times b_3 = -29$ dB. Thus, we know that two noise sources, $NS_1 = -256 \times \text{HD3} \times e_1^3$, and $NS_2 = e_2/8$ are in the output, x_{out}. We assume that the distributions of the quantization noises of two ADCs are uniform. The power of NS_1 and NS_2, P_{NS_1} and P_{NS_2} can be derived as follows.

$$P_{NS_1} \approx 256^2 \times \text{HD3}^2 \times \frac{2}{7}(\frac{V_{FS}/16}{2})^7 \quad (1)$$

$$P_{NS_2} \approx \frac{1}{64}\frac{2}{3}(\frac{\frac{V_{FS}}{2}/42}{2})^3 \quad (2)$$

From Equations 1 and 2, we know that P_{NS_2} is 4.03X bigger than P_{NS_1}. That implies that the quantization noise of the second-stage delay-line ADC dominates the noise introduced by the harmonic distortion of the delay-line ADC in the proposed hybrid ADC. So, the best SNDR ≈ 57.1 dB, and the best ENOB ≈ 9.19 bits. For the differential input, the best SNDR ≈ 63.1 dB and the best ENOB ≈ 10.19 bits.

IV. Proposed Implementation

The fundamental building blocks of the hybrid ADC are a sample and hold (S/H) circuit, a 4-bit flash ADC, a 4-bit DAC, a subtracter, and a delay line ADC, which will be described in the next subsections.

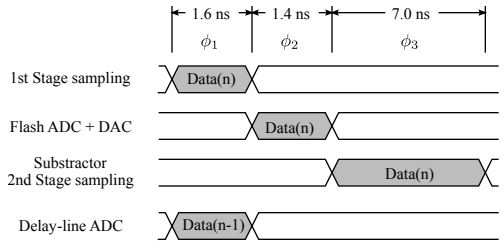

Fig. 4: Proposed timing diagram for the hybrid ADC.

Figure 4 illustrates the timing diagram of the hybrid ADC. There are three timing phases, ϕ_1, ϕ_2, and ϕ_3. First, the S/H circuit samples the input signal in ϕ_1, and then the Flash ADC starts to quantize and the DAC converts the quantized result to an analog signal in ϕ_2. In ϕ_3, the subtracter generates the amplified residue of the first stage, and meanwhile the S/H circuit of the second stage holds the result. In ϕ_1 of the next cycle, the second stage delay-line ADC generates the fine result, while the S/H circuit of the first stage is sampling the next input.

A. S/H circuit

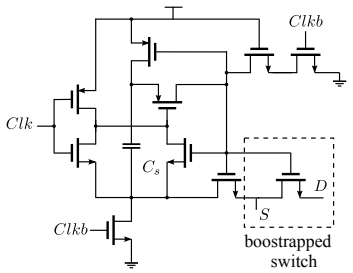

Fig. 5: Bootstrapped switch.

Figure 5 shows the diagram of the bootstrapped switch [3], [4]. At the very beginning of each conversion cycle, the bootstrapped switch tracks the input signal and then holds the signal value when the bootstrapped switch is off. During tracking, the bootstrapped capacitor can ensure the gate-source voltage of the sampling transistor is at the supply voltage (V_{DD}). That maintains the on-resistance of the switch at a small value, so that the switch linearity is improved.

B. 4-bit Flash ADC and 4-bit DAC

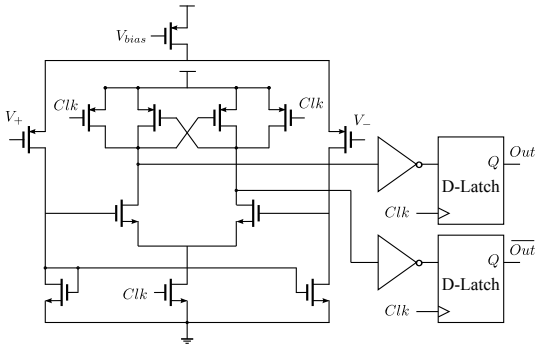

Fig. 6: The schematic of the comparator.

The first stage of the hybrid ADC uses a 4-bit flash ADC to digitize the input and then converts the digital result to an analog signal by a 4-bit DAC. The 4-bit flash ADC is composed of 15 comparators, and each comparator compares the input with a reference voltage. Figure 6 shows the diagram of the comparator. First, the input signal is pre-amplified and then the regenerative latch compares the two inputs. Finally, the result is stored in the D-latch. The gain of the pre-amplifier is ∼20 dB, which can lower the input referred offset of the latch and attenuate kickback noise from the latch. The DC tail current of the pre-amplifier is biased at 47 μA. In order to reduce the power of the pre-amplifier, the bias voltage, V_{bias} is set to 250 mV after the regenerative latch operates, which can significantly reduce the tail current to 5 μA. To ensure the pre-amplifier works properly, V_{bias} is restored to a normal voltage at the time of 3.1 ns before the latch starts to work. Note that V_{bias} when the latch does not operate is set to 250 mV rather than 0 mV, since the restoration time of V_{bias} from 0 mV to the normal voltage is much longer and the tail current has been greatly reduced when being biased to 250 mV.

Also, when Clk is high, the regenerative latch compares the two outputs from the pre-amplifier and forces one output to high and the other to low according to the comparison result. When Clk is low, the D-latch stores the result, and meanwhile, the outputs of the regenerative latch are reset to high. After the 4-bit flash ADC generates the thermometer code, T<15:1>, the 4 bit DAC converts T<15:1> to a corresponding analog value according to two neighboring bits, shown in the left-hand side of Figure 7, and the analog signal is fed to the subtracter as an input, shown in the right-hand side of Figure 7.

C. Subtracter

The right-hand side of Figure 7 shows the subtracter, which is a switched-capacitor circuit, and whose inputs are the sampled signals of input, v_{in} and the DAC result. At the beginning of the conversion, ϕ_1, the subtracter samples v_{in}, and then at ϕ_3, the subtracter amplifies the difference of v_{in} and the DAC output by 8X, and connects the output to the second stage. Note that $C_s/C_f = 8$.

Figure 8 shows the operational amplifier (OPAMP), which is a two-stage folded cascode amplifier, used in the subtracter. The input

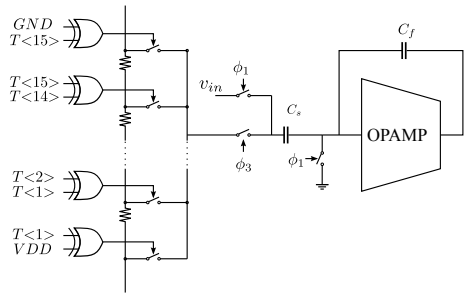

Fig. 7: The 4-bit DAC and the subtracter.

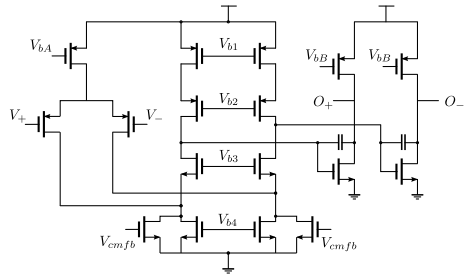

Fig. 8: The operational amplifier in the subtracter.

and output common-mode voltages are designed to be 0.55 V, and the differential inputs of OPAMP is PMOS, while the inputs of the second stage is NMOS, since the transition frequency of NMOS is higher, which allows the second pole of OPAMP further from the first pole to improve the stability of OPAMP. Also, a Miller-compensation capacitor is used to improve the stability of OPAMP. According to the simulation result, the DC gain is around 60 dB for the whole input range. The closed-loop bandwidth and the phase margin are 192 MHz and 76 degrees, respectively. The OPAMP consumes a DC power of around 264 μW.

D. Delay-line ADC

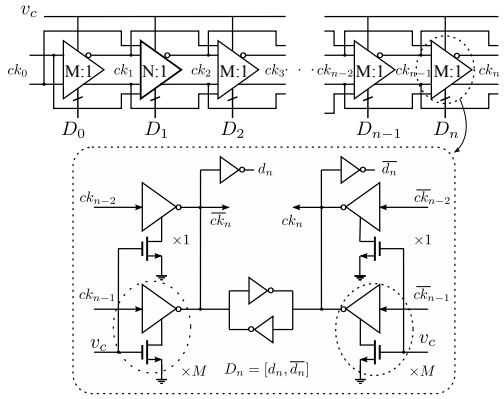

Fig. 9: DIDC and weight-adjusted DIDC chain.

Technology	65nm CMOS
Supply Voltage	1.1V
Sampling Rate	100MS/s
Number of Bits	11
Differential input range	0.8V p-p
SNDR @ 43 MHz	60.0dB
SFDR @ 43 MHz	66.9dB
Power Consumption	1.6mW

TABLE I: Performance summary of the hybrid ADC.

Reference	[7]	[8]	[9]	[6]	[10]	[11]	This work
Architecture	Pipelined	Pipelined	SAR	SAR	Pipelined	Pipelined SAR	Hybrid
Technology	90nm	65nm	65nm	65nm	65nm	40nm	65nm
Supply Voltage (V)	1.2	1.2	1.0	1.2	1.0	1.1	1.1
Sampling Rate (MS/s)	100	100	50	100	200	250	100
Resolution (bit)	12	10	10	10	10	11	11
SNDR (dB)	63.2	59.0	56.6	56.0	57.0	56.0	60.0
Power (mW)	6.2	4.5	0.82	1.13	5.37	1.7	1.6
FOM (fJ/Conv.-step)	52.7	61.8	27.7	15.5	46.4	13.2	19.4

TABLE II: Performance comparison of state-of-the-art work.

In this subsection, we will discuss the second stage delay-line ADC. The delay cell is the core of the delay line ADC, which determines the speed and the resolution of the delay line ADC. The delay cell used in this paper is the dual-input delay cell (DIDC), and the delay line is a weight-adjusted DIDC chain [13], where A constant-delay characteristic can be derived starting from the second delay cell, which can improve the linearity of the delay line. Figure 9 shows the diagram of DIDC and a weight-adjusted DIDC chain. In the simulation result, without any calibration technique, SNDR is 28.7 dB with sampling rate 312.5 MHz, shown in Figure 3.

V. Simulation results

The proposed hybrid ADC is designed and simulated in a commercial 65 nm CMOS process. Table I shows the summary of the simulation results. The differential non-linearity (DNL) and integrated non-linearity (INL) are shown in Figure 10, and the ranges of DNL and INL are 0.47/-0.2 LSB and 0.52/-0.6 LSB, respectively. The high frequency simulation is done by applying a 43 MHz sinusoidal input. Figure 11(a) illustrates the spectrum of the simulation result. The signal-to-noise-plus-distortion ratio (SNDR) and the spurious free dynamic range (SFDR) are 60.0 dB and 66.9 dB, respectively, which provide an effective number of bits (ENOB) = 9.67 bits.

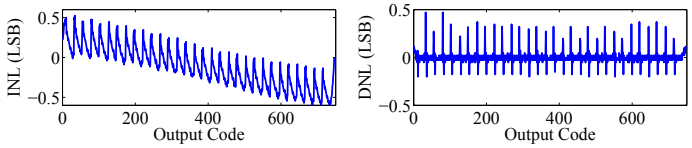

Fig. 10: Simulated DNL and INL.

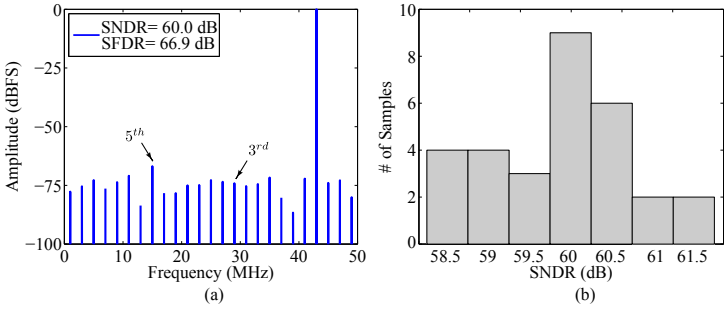

Fig. 11: (a) Output spectrum of a 43 MHz sinusoid input. (b) The SNDR histogram of the Monte Carlo simulations.

Table II shows the comparison between the proposed hybrid ADC and other state-of-the-art ADCs [6]–[11]. The figure of merit (FOM) of the proposed hybrid ADC is 19.4 fJ/conversion-step at 100MS/s and 1.1 V supply. It shows that the hybrid ADC can achieve a competitive FOM with other state-of-the-art ADCs. Also, Monte Carlo simulations using statistical models are performed with a 3σ device mismatch for the SNDR estimation, and the results are shown in Figure 11(b). The SNDR is observed to be better than 58.5 dB when applying a 43 MHz sinusoidal wave.

VI. Conclusion

In this paper, we propose a novel low power 11-bit hybrid ADC, consisting of a 4-bit flash ADC followed by a 7-bit delay-line ADC. In the simulation results, the hybrid ADC yields a FOM of 19.4 fJ/conversion-step, which is competitive with other state-of-the-art ADCs. Also, advantages inherited from flash ADCs and delay-line ADCs strongly support the scalability of the hybrid ADC and its better performance in further scaled fabrication processes.

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