Model Based Hierarchical Optimization Strategies for Analog Design Automation

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***Abstract*—The design of complex analog circuits by using flat optimization-based approaches is inefficient, even impossible, due to the high number of design variables and the growth of the cost of performance evaluation with the circuit size. Over the past two decades, top-down hierarchical design approaches have been developed and applied. They are based on hierarchical circuit decomposition and specification transmission from top-level to lower level blocks. However, such specification transmission is usually performed with little knowledge on the feasibility of the specifications, leading, therefore, to costly redesign iterations. Even if the specification transmission is successful, there is no guarantee that it is optimal in terms of e.g., power consumption or area occupation. To palliate this problem, two novel model-based hierarchical synthesis methods are proposed in this paper: Model-Based Hierarchical Optimization (MBHO) and Improved Model-Based Hierarchical Optimization (IMBHO). They are based on the concurrent design at higher and lower hierarchical levels and appropriate communication between the different processes. Experimental results on a filter example comparing the new approaches and the conventional top-down design approach are provided.**

I. Introduction

Integrated circuit design has become a challenging process with aggressive down-scaling of silicon technology, which results in very complex device models. When these devices are put together, the circuit behavior becomes even more complicated and highly nonlinear. In addition to the complexity, design time is also another constraint for analog designers and long design cycles are not acceptable, especially for commercial applications. Due to the nonlinearity of analytical models, simulation-based and optimization-based circuit design techniques have gained importance over the last two decades [1], [2], [3], [4], [5]. Device-level simulation-based optimization of complex circuits takes excessive (even unacceptable) computation times due to the large design space and the growth of the simulation time with the circuit size. A hierarchical synthesis approach similar to that applied by human designers is commonly accepted as an appropriate approach to deal with this complexity. The idea behind the hierarchical approach is dividing large-scale systems into sub-blocks and searching the optimal solution for each sub-block [3]. Top-down approaches are commonly used for hierarchical design due to their manageable simulation and optimization complexity at each hierarchical level [4], [5], [6], [7], [8], [9], [10]. The synthesis starts at the system-level with system design variables (design parameters and sub-block specs). In general, sub-blocks are represented by behavioral models. Once the optimal solution at a given level is achieved, the required sub-block specs are transmitted to the lower level. Then, the lower level optimization tries to meet the specifications sent by the higher level and finds its optimal solution. Thanks to the application of behavioral modelling techniques, the computational effort is acceptable at higher hierarchical levels. However, conventional top-down approaches also have some limitations. The first one is that specifications are transmitted from the top-level to the bottom-level without knowing if such specifications are feasible or not. If the lower level optimizer cannot satisfy these specifications, redesign iterations would be needed, which delays the synthesis process. The second limitation of top-down approaches is that specifications are transmitted at higher levels without sufficient information about essential parameters like area and power consumption. Very frequently a different specification transmission may lead to better global power and area figures. Furthermore, parallelization of a hierarchical optimization is also feasible and will reduce optimization time further. In this study, two different types of multilayered hierarchical optimization approaches are proposed to address the limitations of the conventional top-down approach. These are Model based Hierarchical Optimization (MBHO) and Improved Model based Hierarchical Optimization (IMBHO).

The paper is organized as follows. In Section II, some background on modeling and optimization is provided. In Section III, the proposed hierarchical optimization strategies are explained in detail. In Section IV, as an example of hierarchical optimization, a 3rd order Butterworth filter is introduced. Experimental results of the filter, which was optimized via flat, top-down, MBHO, and IMBHO approaches are given and discussed. Finally, conclusions are given in Section V.

II. Background

A. Circuit Optimizer

The optimization-based circuit synthesis tool proposed in [11] is used at each level of this approach. The optimizer is based on the evolutionary strategies (ES) algorithm and

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has been implemented in MATLAB. The fitness of candidate solutions found by the optimizer is calculated by using the electrical simulator HSPICE at lower hierarchical levels. Equations have been selected for evaluation at the top-level. The flow diagram of the optimizer is shown in Figure 1. The optimizer searches for the optimal solution with respect to the design objectives determined by the user. The process starts by randomly initializing the individuals. Then, the design parameters (W, L, bias voltages) of these individuals are written to a file and HSPICE is called for circuit performance evaluation. In the next step, cost calculation is performed for the received candidate considering the circuit design objectives and operating point of devices. This process continues until convergence is reached, when the loop breaks and an optimal solution is obtained.

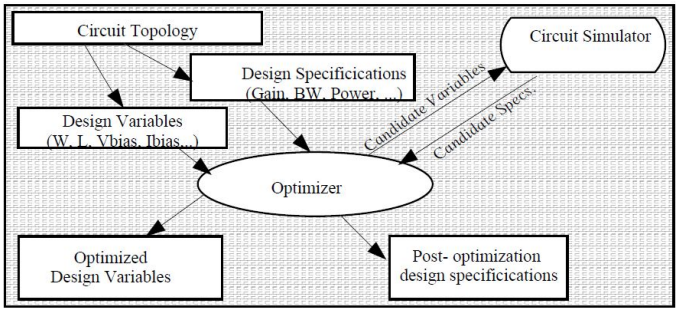

Fig. 1: Optimizer Block Diagram

B. Modeling

Full device-level synthesis of complex blocks or systems is inefficient due to the increased simulation time. The model based approaches can rapidly be processed in terms of exploration of the large design space. Thanks to the considerable flexibility, accuracy, and speed, they are commonly used in the hierarchical system synthesis. Thus, hierarchical optimization approaches promise faster process time with sufficient accuracy. In general, models are prepared by the designer manually, but complex systems lead to a lot of higher order equations, which are quite difficult to derive, manually. Symbolic circuit analysis tools can be utilized for extraction of these equations. However, they cannot be applied to circuits having nonlinear characteristics. A detailed overview that discusses the modeling strategies for both linear and nonlinear systems is provided in [12].

III. Hierarchical Optimization Strategies

Hierarchical design makes possible to solve large scale problems by dividing into sub-problems. A hierarchical system may include either two layers, the high and the low levels, or multiple layers, one top level and multiple lower layers, depending on the structure of the system. Communication among the populations located in the different layers is highly important to accelerate the convergence speed of the algorithm to the optimal solution and diminish the total computation time. Therefore, an efficient coordination among the layers has to be developed to enhance the optimizer performance.

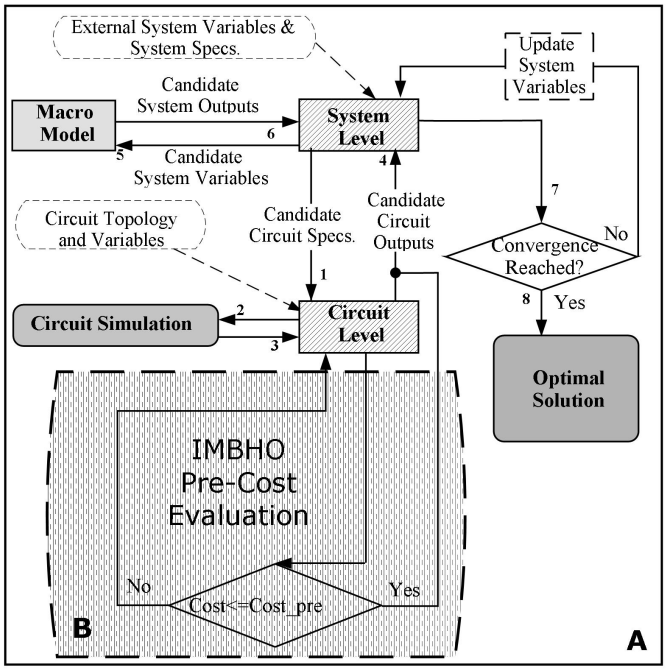

Fig. 2: Model Based Hierarchical Optimization Flow Diagram

A. Model Based Hierarchical Optimization (MBHO)

MBHO is based on modeling lower level blocks using behavioral models to be inserted into the higher level. The synthesis flow for two layers is shown in Figure 2. The numbers in the layer A refer to the order in which each step is executed. The synthesis process starts at the system level by initializing the block specifications of the individuals of the system level population. These are then sent to the circuit level as candidate circuit specifications. These individuals are ordered according to the system cost values and circuit level synthesis starts from the individual having the lowest cost. Then, they are optimized through the circuit variables considering the block specifications sent from the system-level. As a result of the circuit level optimization, the performance and cost of each block is determined. These are then sent back to the system level. Top-level optimization restarts accounting for the external system variables. The system level optimizer considers sub-block costs for the overall cost calculation. This process continues until both circuit-level cost and system-level cost drop to the desired level.

B. Improved Model Based Hierarchical Optimization (IMBHO)

The underlying mechanism for this method is similar to MBHO. The main difference is that circuit-level optimization is not fully carried out in IMBHO. This is based on the well-known fact that ES-based optimization approaches provide the vicinity of the solution within a few generations, thus giving a rough idea about the final cost of the total design. As the circuit cost needs not be accurately calculated in intermediate iterations, the synthesis time may be significantly decreased if the low-level circuit optimization process is stopped earlier. In addition to the general view of the MBHO that is shown

TABLE I: Design Specifications

Aprroach	Device Level	Top Level
Flat	R-C ratios, Cut-off frequency, Power, Area	—
Top-Down	Gain, Bandwidth, Rout	R-C ratios, Cut-off frequency, Power, Area
MBHO	Gain, Bandwidth, Rout, Power, Area	R-C ratios, Cut-off frequency, Power, Area
IMBHO	Gain, Bandwidth, Rout, Power, Area	R-C ratios, Cut-off frequency, Power, Area

in Figure 2 (layer A), a pre-cost evaluation part (layer B) is included to represent the IMBHO flow.

IV. Implementation of Hierarchical Optimization Approaches

In order to test the proposed hierarchical optimization approach, a third-order Butterworth low-pass filter with Sallen-Key topology, shown in Figure 3, will be used.

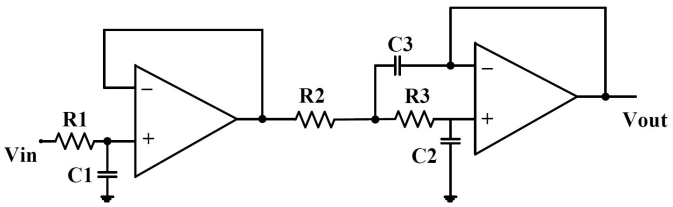

Fig. 3: Third Order Butterworth Low Pass Filter with Sallen-Key Topology

Accounting for the non-ideal performances: gain and output impedance, the transfer function of the Op-amp is

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{K_3 Z_2 s^2 + K_3 Z_1 s + K_3 Z_0}{s^3 + \frac{K_2}{K_3} s^2 + \frac{K_1}{K_3} s + \frac{K_0}{K_3}} \qquad (1)$$

where the coefficients K_i depend on the external resistor and capacitor values as well as finite gains and output resistances of the Op-Amp. The equations for each K are quite long and are not given in this paper. However, they can be easily obtained using symbolic analysis tools.

Simulations were performed with HSPICE using $0.18\mu m$ model parameters. An Intel I7 chipset with 2.80GHz clock frequency was utilized during the synthesis process. In all approaches, filter cut-off frequency, resistor and capacitor ratios are given to the optimizer as the design objectives, whose values are 10kHz, 2, and 4, respectively. In addition to these targets, the optimizer tries to minimize power consumption and area occupation in the flat, MBHO, and IMBHO methods at the device level. On the other hand, system level tries to minimize the total power and area for all approaches. Design specifications of all approaches for different layers are summarized in Table I. To test the flat approach the Butterworth filter was described at full transistor level. The selected test circuit is sufficiently simple so that the flat synthesis approach is feasible and the synthesis results can be used as a comparison benchmark. However, it has to be considered that for more complex circuits, a flat synthesis approach cannot be used due to the complexity of the design space and the exponentially increasing simulation times. For the top-down, MBHO, and IMBHO approaches, equations based circuit models were developed for the top-level modeling. Considering the top-down approach, after the system level optimizer achieves the optimal point, the required specifications of the Op-Amps are sent to the circuit level, where they are realized. Optimization is completed after the circuit level optimization. On the other hand, in MBHO, Op-Amps are the sub-blocks in the hierarchy and are optimized at the circuit level first. Then, the sub-block specifications (Gain, Bandwidth, Output Resistance, Power, and Area) are sent to the model. Cost calculation and performance evaluation are performed at the top level considering equations of the top level and simulation results of the circuit level. If convergence is reached, the synthesis is completed and optimal solution is achieved. If convergence is not reached, the variables of system and circuit level are updated and synthesis restarts. Considering IMBHO, in order

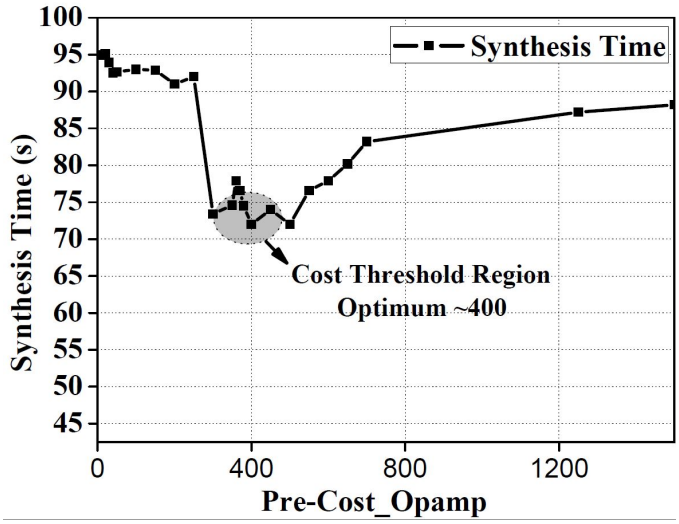

Fig. 4: Synthesis Time versus Pre-Cost Value of the Device-Level

to achieve a better synthesis time, the sub-blocks (Op-Amps) are optimized down to a sub-optimal point where the Op-amp is sufficiently close to the optimal point; thus the optimizer gets rid of unnecessary computation for final optimization. The cost at this sub-optimal point is called pre-cost. The sub-optimal point does not have to be very precise and can be determined heuristically by stopping the optimization at a point where improvement along several iterations is low. To show the dependence of the overall optimization system on the pre-cost value, several simulations were done with different sub-optimal points. As can be seen from Figure 4, the threshold cost value is determined as $\approx$ 400. Larger threshold values result in wrong estimations for the Op-Amp costs, misleading the filter optimizer, whereas smaller values result in overly accurate estimations leading to unnecessary long optimization times. Very small threshold values results in the same algorithm as

TABLE II: Synthesis Results for 7 Runs

Design Specification	Flat		Top-Down		MBHO		IMBHO	
	Mean	Std. dev.	Mean	Std. dev.	Mean	Std. dev.	Mean	Std. dev.
Synthesis Time $[s]$	324.62	25.7	175.445	41.4	191.28	15.9	165.78	14.38
Cut-off Frequency$[kHz]$	10.52	0.38	10.12	0.15	9.65	0.29	9.74	0.73
Rmax/Rmin	2.16	0.26	2.87	0.49	1.96	0.45	1.91	0.38
Cmax/Cmin	3.91	0.35	6.48	0.37	4.38	0.52	4.52	0.46
Power Consumption $[mW]$	0.8532	0.06	1.381	0.4	0.8148	0.06	0.8712	0.046
Chip Area $[10^{-9}m^2]$	2.2	0.14	4.84	2.11	3.72	0.48	3.96	0.29

MBHO.

Being stochastic algorithms, a statistical study has been performed. As expected, the worst approach in terms of synthesis time is the flat synthesis method. The first proposed approach (MBHO) is faster than the flat, but slower than the top-down approach due to the increased number of simulations at the lower level. However, it also has to be considered that a single iteration has been considered in the top-down approach. If new redesign iterations were to be performed, either because unfeasible Op-Amp specifications are obtained or because results have to be improved, the synthesis time would increase substantially. The improved version (IMBHO) speed is quite comparable with the top-down approach thanks to the pre-cost evaluation, although the top-down approach does not iterate between levels.

Power consumption, chip area, and resistance and capacitance ratios as well as the cut-off frequency are important to evaluate the performance of the approaches. Therefore, a comparison table including the mean values and standard deviations of 7 independent runs is provided in Table II. As can be seen from this table, all methodologies approach the desired cut-off frequency (10kHz), resistor and capacitor ratios (2 and 4, respectively). However, the top-down method has trouble in satisfying the capacitor ratio as well as not being able to minimize power consumption and area. At last, there is not a meaningful difference in terms of performance between MBHO and IMBHO; however, IMBHO provides good results in less time.

V. Conclusion

Due to the diverse and vast design variable space, flat optimization-based approaches may become inefficient for medium to large analog circuits due to the long optimization. Hierarchical optimization-based approaches promise better performances; however, conventional top-down approaches may lead to sub-optimal solutions due to determination of the lower level specifications at the higher level without information regarding their feasibility. This case leads to redesign iterations causing increase in total synthesis time. On the other hand, although the lower level specifications can be realizable, the converged point may be far from the optimal point in terms of system specifications (power and area). In order to overcome this problem, two model based approaches (MBHO and IMBHO) that provide a better transmission of specifications between the layers, are proposed. Furthermore, IMBHO promises better synthesis CPU times thanks to pre-cost evaluation without loss of performance. Experimental results show that the proposed approaches satisfy the objectives as good as the flat approach. Moreover, the synthesis time performance of the IMBHO approach is as good as the conventional top-down approach.

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