ACM SIGDA / EDAA PhD Forum at DATE 2013 in Grenoble

The ACM SIGDA / EDAA PhD forum is part of the DATE Conference and hosted by ACM SIGDA and the European Design Automation Association (EDAA). It offers the opportunity for PhD students to present their thesis work to a broad audience in the design, automation and test community from academia and industry. During the presentation at the DATE Conference, it helps students to establish contacts. Also, representatives from industry and academia get a glance of state-of-the-art research in design, automation and test. The review process resulted in the selection of the PhD students listed below. We thank ACM SIGDA, EDAA, and DATE for making this Forum possible.

Peter Marwedel (Chair, ACM SIGDA / EDAA PhD Forum at DATE 2013)

PhD Forum Committee

Peter Marwedel (Chair), TU Dortmund, Germany

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Sander Stuijk, TU Eindhoven, Netherlands

Miroslav Velev, Aries Design Automation, USA

Norbert Wehn, TU Kaiserslautern, Germany

Admitted Presentations

1. Laurent Bousquet (Tima Laboratory, Grenoble, France): Energy Consumption Information in High-level Models
2. Paolo Burgio (Università di Bologna, Italy): OpenMP extensions to Exploit HW Acceleration on Shared-Memory Many-Core Clusters
3. Weiwei Chen (UC Irvine, USA): Out-of-order Parallel Simulation for Electronic System-Level Design
4. Wang Chundong (National University of Singapore, Singapore): On Efficient Management of Flash Memory for Long Lifetime and High Performance
5. Masoud Daneshtalab (University of Turku, Finland): Low-latency, Memory-Efficient, and Congestion-Aware On-Chip Network with Adaptive Interfaces
6. Prasanjeet Das (University of Southern California, USA): A Resilient Framework for Post-Silicon Delay Validation of High Performance Circuits
7. Onur Derin (University of Lugano, Switzerland): Self-adaptivity of Applications on Network on Chip Multiprocessors: The Case of Fault-Tolerant Kahn Process Networks
8. Emad Ebeid (University of Verona, Italy): Modeling and Synthesis of the Network in Distributed Embedded Systems
9. Masoumeh Ebrahimi (University of Turku, Finland): Path-based Partitioning Methods for 3D NoCs with Minimal Adaptive Routing
10. Felipe F. Ferreira (Lyon Institute of Nanotechnology, France): Architectural Exploration Methods and Tools for Heterogeneous 3D-IC
11. John Jose (IIT Madras, India): Working With Adaptive NoC Routers
12. Steve Kerrison (University of Bristol, United Kingdom): Energy-Aware Multi-Threaded Software Systems: An Overview
13. Ioannis Koutras (National Technical University of Athens, GR): On Optimizing Dynamic Memory Allocators

14. Christos Kyrkou (University of Cyprus, Cyprus): FPGA-based Hardware Accelerators for Embedded Object Detection Systems
15. Asma Laraba (Tima Laboratory, Grenoble, France): Built In Self Test of Pipeline Analog-to-Digital Converters
16. Hoang Le (University of Bremen, Germany): Automated Techniques for Verification-driven Design at the Electronic System Level
17. Paolo Manfredi (Politecnico di Torino, Italy): High-Speed Interconnect Models with Stochastic Parameter Variability
18. Bojar Maric (Barcelona Super Computer Center, Spain): Microarchitectures for Hybrid High and Ultra-low Voltage Operation
19. Benjamin Menhorn (Ulm University, Germany): Design Entropy
20. Srobona Mitra (IBM Pvt. Ltd., India): Formal Methods for Aiding Verification of Local Design Changes in Digital Integrated Circuits
21. Subhankar Mukherjee (IIT Kharagpur, India): Assertions: From a Mixed-Signal Perspective
22. Purushotham Murugappa (Telecom Bretagne, Brest, France): Towards Optimized Flexible Multi-ASIP Architectures for LDPC/Turbo Decoding
23. Mircea Negrean (University of Braunschweig, Germany): Performance Analysis of Complex Real-Time Applications on Multi-Core Systems with Shared Resources
24. Ashkan Beyranvand Nejad (Delft University of Technology, Netherlands): Composable Execution of Mixed-Criticality Embedded Applications With Mixed-Models-of-Computation
25. Andrew Nelson (Delft University of Technology, Netherlands): Composable Application-level Power Management for Real-Time Embedded Systems
26. Luis Olivera (University of Porto, Portugal): RSSI-based Localisation of Mobile Robots With Online Channel Estimation
27. Santosh Onkaraiah (CEA-LETI MINATEC, Grenoble, France): Improving Performance of FPGAs Using Resistive Switching Memory (RRAM) Based Low Power Circuit Architectures
28. Mwaffaq Otoom (Yarmouk University, Jordan): Capacity Metric for Chip Heterogeneous Multiprocessors
29. Karthik Parashar (INRIA Bretagne Atlantique, Rennes, France): System-Level Approaches for Fixed-Point Refinement of Signal Processing Algorithms
30. Marcel Pockrandt (TU Berlin, Germany): Model Checking Memory-Related Properties of SystemC Transaction Level Designs
31. Julian Pontes (Universidade Católica do Rio Grande do Sul, Brazil): Soft Error Mitigation in Asynchronous Networks on Chip
32. Paulo Possa (University of Mons, Belgium): A Reconfigurable Low-Latency Architecture for Real-Time Image and Video Processing
33. Petar Radojkovic (Barcelona Super Computer Center, Spain): Thread Assignment of Network Applications in Multithreaded Processors: A Statistical Approach
34. Semeen Rehman (Karlsruhe Institute of Technology, Germany): Reliable Software for Unreliable Hardware
35. Hesham Saadawi (Carleton University, Ottawa, Canada): Verification of Hybrid DEVS Models
36. Mohammadsadegh Sadri (University of Bologna, Italy): MiMAPT: Adaptive Multi-Resolution Thermal Analysis at RT and Gate Level
37. Amit Kumar Singh (Nanyang Technological University, Singapore): Run-time Mapping Techniques for NoC-based Heterogenous MPSoC Platforms
38. Kasyab Parmesh Subramaniyan (Chalmer University, Sweden): Variability, Regularity and DFM Metrics
39. Jai Narayan Tripathi (Indian Institute of Technology Mumbai, India): Power Integrity Analysis and Discrete Optimization of Decoupling Capacitors
40. Christos Ttofis (University of Cyprus, Cyprus): Disparity Estimation Hardware Architectures and Design Techniques for Embedded Stereo Vision Applications
41. Martijn van den Heuvel (Eindhoven University of Technology, Netherlands): Composition and Synchronization of Real-Time Components Upon one Processor
42. Xinsheng Wang (Harbin Institute of Technology, Harbi, China): Low Power and High Performance Current Mode On-Chip Interconnect System Design and Optimization