An Enhanced Double-TSV Scheme for Defect Tolerance in 3D-IC

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***Abstract*—Die stacking based on Through-Silicon Via (TSV) is considered as an efficient way to reducing power consumption and form factor. In the current stage, the failure rate of TSV is still high, so some type of defect tolerance scheme is required. Meanwhile, the concept of double-via, which is normally used in traditional layer to layer interconnection, can be one of the feasible tolerance schemes. Double-via/TSV has a benefit compared to TSV repair: it can eliminate the fuse configuration procedure as well as the fuse layer. However, double-TSV has a problem of signal degradation and leakage caused by short defects. In this work, an enhanced scheme for double-TSV is proposed to solve the short-defect problem through signal path division and VDD isolation. Result shows that the enhanced double-TSV can tolerate both open and short defects, with reasonable area and timing overhead.**

Keywords—TSV; 3D-IC; open-defect; short-defect; defect tolerance; yield improvement

I. INTRODUCTION

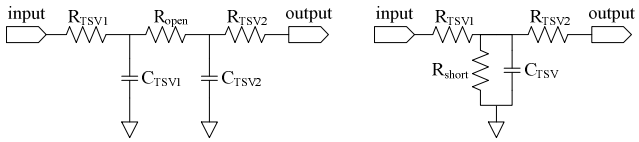
In recently year, mobile device becomes popular, and the requirements of mobile device become important, such as low power consumption, high energy efficiency, and small form factor. According to [1], 3D integration based on TSV can be an efficient way to achieve these requirements. Hence, the 3D integration based on TSV is a trend in the future.

In the past few years, some information about TSV has been reported in [2]-[4]. From these references, the failure rate of TSV is still high, so some type of defect tolerance scheme is required. In [5], a switching repair method has been used to enhance the TSV stacking yield for 3D DRAM. Similar method is also used on NoC links and on chip router in [6] and [7] respectively. Another repair method by TSV shifting has been proposed in [8]. However, all repair methods require the record of failure information and the fuse configuration. Those requirements lead to extra cost for fuse or even manufacturing flow. In addition to TSV repair, [9] tries to compensate the signal coming from the defective TSV. However, it still requires the test and configuration procedure. Furthermore, [10] encodes the multi-bit data into multi-level signal, and then sends the signal through multi TSVs, and finally decodes the signal at the receiver. Although it eliminates the fuse configuration procedure, the encoder and decoder increase the complexity.

From the experience in traditional IC design, double-via is a normal way to tolerate defect. This method doesn't require the fuse configuration and it can be implemented easily. However, when the interconnection changes from layers to dies, the double-via/TSV meets some new problems. First, the TSV area is much larger than the traditional via, so whether the double-TSV makes sense remains unknown. Second, short or pinhole defect, which doesn't exist in traditional via, can possibly occur in TSV [11]. In this paper, we first evaluate the value of double-TSV, and then propose a method to solve the short-defect problem. In Sec. II, the defect model is introduced. In Sec. III, the cost comparison for double-TSV is reported. In Sec. IV, the method to solve the short-defect problem is proposed, and it is proved in the Sec. V. The experiment is in the Sec. VI. Then the conclusions are in the final section.

II. DEFECT IN TSV

This section describes the defect and the defect model used in the remaining content. The first subsection describes open-defect and the second subsection describes short-defect.



(a) Open defect model. (b) Short defect model.

Figure 1. Defect model used in this work.

A. Open-defect

Open-defect can possibly exist because of the break of conductor [12], the void between TSV and bonding pad [13], or misalignment during bonding process [11]. The open-defect leads to large TSV resistance. It can be modeled by serially connecting a resistance, R_{open}, with TSV model as Figure 1(a) shows. This defect model is also used in [14].

B. Short-defect

Short-defect can possibly exist because of the pinhole at the insulator [12], Cu extrusion from the bonding pad [13], or misalignment during bonding process [11]. The short-defect leads to signal degradation and large leakage current. It can be modeled by connecting a resistance, R_{short}, from TSV to

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substrate as Figure 1(b) shows. This defect model is also used in [9] and [15].

III. Cost Analysis for Double-TSV

In this section, the cost analysis is made to confirm that double-TSV can reduce the cost of stacking if it can tolerate both open-defect and short-defect. In the first subsection, the comparison is made between double-TSV and single TSV. In the second subsection, the comparison is made between double-TSV and the switching repair from [5].

A. Single TSV and Double-TSV

IV. TABLE I. TSV Information

	HRI 2009 [2]	IMEC 2006 [3]	IBM 2005 [4]
TSV Pitch	50 um	10 um	0.4 um
TSV Failure Rate	0.6 ppm	40 ppm	14 ppm
Stacking Yield / With Double-TSV	99.85% / ----	88.69% / 99.9995%	95.89% / 99.9999%
TSV Area / With Double-TSV	2.5 mm^2 / ----	0.1 mm^2 / 0.2 mm^2	160 um^2 / 320 um^2

The analysis based on the TSV information reported from [2]-[4]. The used information is listed in Table 1. The stacking yield can be calculated from the TSV failure rate, TSV number, and the stacking number of die. In addition, the TSV area can be calculated from the pitch of TSV. With the assumption of 1000 TSVs and 4 die stacking, the stacking yield and TSV area are calculated and recorded in Table 1.

According to Table 1, although small TSVs, such as IMEC2006 or IBM2005, has higher TSV failure rate than HRI2009, they can have lower area cost and higher stacking yield than HRI2009 with double-TSV scheme. This shows that double-TSV can reduce the manufacturing cost.

A. Double-TSV and Switching Repair

V. TABLE II. Comparison for Switchiing Repair and Double-TSV

	Switching Repair [5]	Double-TSV
TSV Number	300	
Stacking Number	4	
Area for Functional Circuit	96.176 mm^2	
TSV Pitch	80 um	
TSV Failure Rate	0.0063	
Stacking Yield	~98%	98.81%
Area Overhead	~2%	1.996%

[5] reports some information about the switching repair. It stacks 4 dies with 300 signal TSVs, and the TSV pitch is 80um. Without switching repair, the stacking yield is 15%. Hence the TSV failure rate is about 0.0063. With switching repair, the stacking yield achieves about 98%, and the area overhead is ~2% with 80 um of TSV pitch. With the total chip size (10.9 mm*9.0 mm), the area for functional circuit can be get: 96.176 mm^2.

For double-TSV, it has 300 redundant TSVs, 1.92 mm^2 of area based on 80um of TSV pitch. Hence the area overhead is about 1.996%. With 0.0063 TSV failure rate, the stacking yield is about 98.81%. The overall data is collected in Table 2. It can be observed that double-TSV is comparable to switching repair on stacking yield and area overhead.

VI. Double-TSV Enhancement

Before describing the TSV enhancement, we describe the targeting problem in the first subsection. Then the enhancement (Figure 2) is illustrated in the second and the third subsections. In figure 2, since the *path 1* and the *path 2* are symmetric, we only detail the *path 1*.

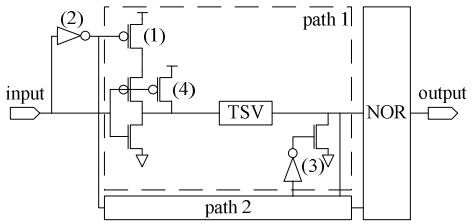


Figure 2. Double-TSV enhancement.

A. Traditional Double Via/TSV Problem

In the traditional IC design, double or even multiple via is useful for defect tolerance. However, as the interconnection environment moves from layers to dies, the material around via changes from insulator to semiconductor. It becomes possible that some defects can make TSV short to ground. If there is short-defect grounding one of double-TSV pair, the signal through the other TSV may be degraded or even stuck at 0, because these two TSVs share the same node. In addition, this short-defect can also produce a large leakage current. In summary, although traditional double-TSV can tolerate open-defect, it has week tolerance against short-defect. To simplify the problem, we assume the substrate around TSV is connected to ground in this work.

B. Path Division and VDD Isolation

To prevent the signal degradation from defective TSV in TSV pair, the signal path is divided into two paths: the *path 1* and the *path 2* in Figure 2. The input nodes of TSV pair are separated by two driving circuits which are implemented by inverters in this work. The output nodes of TSV pair are separated by receiving circuit which has OR or NOR behavior. With the assumption that the substrate around TSV is connected to ground, only stuck at 0 fault can possibly occur from short-defect. Hence an OR/NOR gate can filter the fault behavior and recombine the signal. With this scheme, the healthy TSV is guarded by driving and receiving circuits from defective TSV.

For the leakage current, the driving circuit should be turned off in the end of TSV signal transition. Since we assume that the substrate around TSV is connected to ground, it is impossible that TSV shorts to VDD. Hence, only the VDD driving path must be turned off. That is achieved by the *VDD switch* in Figure 2. In addition, a *switch controller* for the *VDD switch* is required. In this work, this controller is the inverse of the input signal with a delay time which is designed larger than the rising time of TSV voltage transition. With the *VDD switch*, the leakage current path from VDD to substrate would be turned off in the end of voltage transition.

C. ZERO Driving Path

Although the path division and VDD isolation can solve the short-defect problem, it induces another problem: floating node causing from open-defect. If there is an open-defect in one of TSV pair leading to floating node at the output of this defective TSV, the result of signal recombination after OR/NOR gate can possibly be wrong. The error occurs only if the floating node has dominant value of OR/NOR gate, because the signal will be masked by the dominant value.

To overcome this problem, a signal path between TSV pair should be implemented. Fortunately, the masking effect appears only if the signal of healthy TSV has non-dominant value which is logic zero for OR/NOR gate. Hence the signal path that can pass the logic zero is required. That is achieved by *ZERO driving path* in Figure 2. However, the signal path also transmits short-defect effect if there is short-defect in one of TSV pair. Hence a *VDD keeper* is required, and it should be stronger than the *ZERO driving path*.

With the overall enhancement, the signal degradation is restricted through the path division, and the leakage current is reduced to the current of *VDD keeper*, which is much smaller than the main driving component.

VII. Defect Tolerance Theorem

In this section, a proof for the double-TSV enhancement is developed. The behavior model of Figure 2 is analyzed first. Then the proof is demonstrated by three cases: open-defect, short-defect, and no defect.

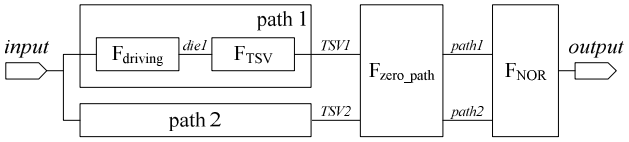


Figure 3. Behavior model.

A. Behavior Model

The overall enhancement scheme can be modeled as Figure 3 shows. $F_{driving}$ is for the driving circuit. In the case of no defect or open-defect, the driving circuit is exactly an inverter. In addition, since the driving circuit has a VDD switch, the output of driving circuit becomes logic zero as there is short-defect in the driven TSV. Hence, the function $F_{driving}$ can be described as Equation (4).

F_{TSV} is for the TSV channel. It can be seen as a buffer if there is no defect. On the other hand, if there is short-defect in TSV, the output of TSV channel is logic zero with the assumption that short-defect has resistance equal to 0 for simplifying the analysis. If there is open-defect in TSV, the output of TSV channel is a floating node with the assumption that open-defect has resistance equal to infinite. Hence, F_{TSV} can be described as Equation (5).

F_{zero_path} is for the *ZERO driving path*. It passes logic zero from one to another in the double-TSV pair. In addition, the driving strength of this path is weaker than *VDD keeper*, so the input logic one from TSV still remains the same value if there is conflict causing from short-defect in another TSV. Hence, the function F_{zero_path} can be written as Equation (6) and it can be further expressed to Equation (7).

F_{NOR} is simply a NOR function. As a result, the overall enhancement behavior is fully transformed to description language as Equation (4) to (7), and the proof of defect tolerance theorem can be done based on these equations in the following subsection.

$$F_{driving}(input, defect) = (defect==short)?\ 0:{\sim}input \quad (4)$$

$$F_{TSV}(die1, defect) = (defect==open)?\ Z:((defect==short)?\ 0:die1) \quad (5)$$

$$F_{zero\_path}(TSV1, TSV2) = [(TSV1==1)?\ 1 : ((TSV2==0)?\ 0:TSV1),\ (TSV2==1)?\ 1 : ((TSV1==0)?\ 0:TSV2)] \quad (6)$$

$$F_{zero\_path}([TSV1, TSV2]) = \text{case } (TSV1==X, TSV2==0)\text{: } [0, 0]\ \text{case } (TSV1==0, TSV2==X)\text{: } [0, 0]\ \text{others: } [TSV1, TSV2] \quad (7)$$

B. Proof of Double-TSV Enhancement

All possible conditions can be covered by three cases: no defect; short-defect in one of double-TSV pair; open-defect in one of double-TSV pair. In the case of no defect, assume that *input* is *s*. According to Equation (4) and (5), both TSV*1* and *TSV2* are ~*s*. Hence both *path1* and *path2* are also ~s from Equation (7), so *output* would be *s*.

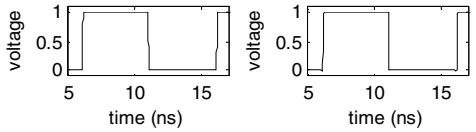
In the case of short-defect, assume that the signal of *input* is *s*. Since the two paths are symmetric, we only discuss the defect injection in path 1. The *TSV1* becomes *0* due to the short-defect, and the *TSV2* remains ~*s*. Hence [*path1*, *path2*] are [*0*, ~*s*]. With the receiver of NOR, *output* is also *s*.

In the case of open-defect, assume that the signal of *input* is *s*. With the feature of symmetry, we only discuss the defect injection in path 1. The *TSV1* becomes *X* due to the short-defect, and the *TSV2* remains ~*s*. Hence two results are possible for *path1* and *path2* depending on the value of *TSV2* (~*s*). If ~*s* equals *1*, [*path1*, *path2*] is [*X*, *1*]. If ~*s* equals *0*, [*path1*, *path2*] is [*0*, *0*]. Either case makes the *output* become *s*.

From these three cases, we demonstrate that the function of enhanced double-TSV is correct theoretically, and it can tolerate either one short-defect or one open-defect.

VIII. Experiment

In this section, a verification based on circuit simulation is done. The enhancement scheme and baseline are built according to Figure 2 and traditional double-TSV respectively by TSMC 90nm transistor library. The TSV model is from IMEC report [16]. The fault models of short and open-defect are described in the Sec. II. In the verification, three cases have been done: no defect, short-defect, and open-defect. Figure 4 verifies the function of input and output for no defect. Figure 5 shows the waveform for short-defect as the defect value sweeps from 10 to 10K by log scale. With low defect resistance, the output value of baseline is stuck at 1, which means that TSV is stuck at 0, while the output is still correct with the enhancement.



(a) Input signal. (b) Output signal.

Figure 4. Simulation result of double-TSV enhancement for no defect.

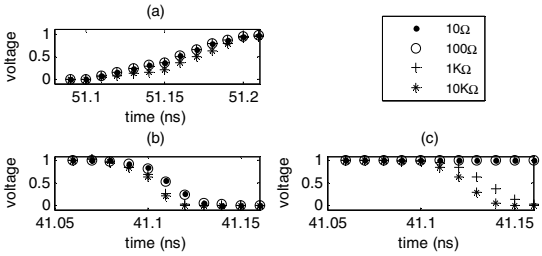


Figure 5. Simulation result for short-defect: (a) rising transition of double-TSV enhancement; (b) falling transition of double-TSV enhancement; (c) falling transition of baseline.

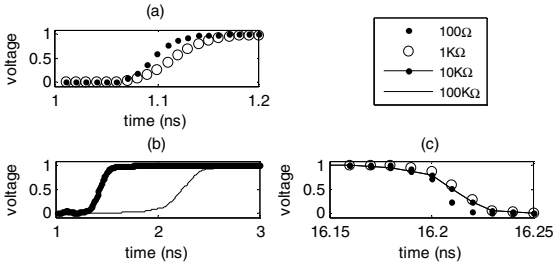


Figure 6. Simulation result of double-TSV enhancement for open-defect: (a) rising transition for 100 and 10K of open-defect; (b) rising transition for 10K and 100K of open-defect(c) falling tansition

Figure 6 shows the waveform for open-defect as the defect value sweeps from 100 to 100K by log scale. It can be observed that the rising transition delay increases with the defect value. Furthermore, the current comparison for short-defect is reported in Table 3. The enhancement scheme reduces the current consumption to *VDD keeper*.

From the experiment, we validate that the double-TSV enhancement solves the problems causing from short-defect with some timing penalty. Although the area overhead from enhancement scheme may makes double-TSV larger than repair method according to the rough calculation in Sec. II, double-TSV can eliminate the fuse configuration as well as the cost from the fuse layer. Furthermore, it has the ability for on-line tolerance during whole period of production life.

TABLE III. CURRENT CONSUMPTION FOR SHORT-DEFECT

Circuit \ Resistance (Ohm)	**10**	**100**	**1K**	**10K**
Baseline (mA)	1.04e-0	9.80e-1	4.20e-1	5.67e-2
With Enhancement (mA)	7.65e-2	7.54e-2	6.25e-2	5.44e-2

IX. CONCLUSIONS

Cost analysis shows that defect tolerance of TSV is required for reducing manufacturing cost. Double-TSV can be one of the feasible defect tolerance methods. However, the traditional double-TSV scheme has short-defect problem. With the enhancement proposed in this work, the short-defect problem can be solved. This enhancement is not only proved theoretically, but also verified by circuit simulation. In addition, as the enhanced double-TSV is implemented at circuit level, it eliminates the need of fuse, thus the associated cost. The enhancement scheme also has on-line tolerance capability. As a result, the enhanced double-TSV is an efficient way to reducing the manufacturing cost of TSV based 3D-IC.

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