Automatic Circuit Sizing Technique for the Analog Circuits with Flexible TFTs Considering Process Variation and Bending Effects

Yen-Lung Chen Wan-Rong Wu Guan-Ruei Lu Chien-Nan Jimmy Liu

Dept. of Electrical Engineering, National Central University, Jung-Li City, Taiwan, ROC
{995401004, 995201021, 100521013}@cc.ncu.edu.tw; jimmy@ee.ncu.edu.tw

ABSTRACT

Flexible electronics are possible alternative for portable consumer applications with many advantages. However, the circuit design for flexible electronics is still challenging, especially for sensitive analog circuits. Significant parameter variations and bending effects of flexible TFTs further increase the difficulties for circuit designers. In this paper, an automatic circuit sizing technique is proposed for the analog circuits with flexible TFTs. The process variation and bending effects of flexible TFTs are considered simultaneously in the optimization flow. As shown in the experimental results, the proposed approach can further improve the design yield and significantly reduce the design overhead.

I. INTRODUCTION

Flexible electronics are possible alternative to conventional silicon electronics for portable consumer applications with many advantages. The most commonly used active device in flexible electronics is the thin-film transistor (TFT). However, as mentioned in the survey paper [1], the circuit design for flexible electronics is challenging for several reasons. Due to quite different properties of flexible TFTs, conventional CMOS design techniques cannot be used directly on flexible electronics. Moreover, the variations on key transistor parameters such as threshold voltage (V_{th}) and mobility (μ) are much greater than the variations in silicon CMOS technologies, which significantly increase the difficulty of designing analog circuits. Therefore, a robust circuit design methodology is essential to implement more complex applications with flexible electronics.

The most challenging issue for designers is the unstable mobility of TFTs due to their flexible property. Many researches [2] have shown that the mechanical strain may change the TFT's mobility significantly. As illustrated in Fig. 1, different bending schemes also have different impacts on the mobility change. In the compressive mode, the mobility of amorphous-silicon (a-Si) TFTs is reduced up to 25% [2]. In the tensile mode, the mobility is increased up to 10% [2]. In other words, the mobility change is a non-symmetrical distribution, which violates the typical assumption of normal distribution. In conventional CMOS technology, the transistor mobility is almost fixed. Therefore, special attention should be paid on this unstable mobility issue while designing the analog circuits with flexible TFTs.

In the literature, most of the approaches to increase the reliability of flexible electronics are adding self-tuning mechanism in the circuits to deal with process variations during circuit operations [3, 4].

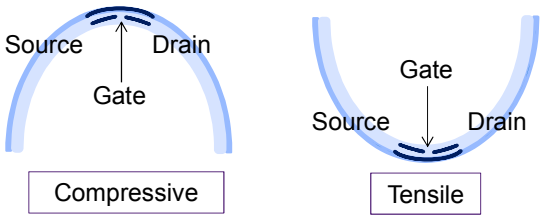

Figure 1. Different bending schemes in flexible TFTs [2]

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Although this kind of feedback approaches may increase the performance, changing the original circuit structures may require extra design efforts and circuit overhead. For silicon CMOS circuits, design-for-yield (DFY) techniques are proposed to consider the process variation effects in the design phase, especially for analog circuits. By carefully adjusting the device sizes and nominal design point of the circuit, the tolerance to process variations can be improved significantly without changing the circuit structure.

In the literature, many robust optimization techniques for analog circuit are proposed based on simulation-based synthesis approaches [5, 6]. Although these approaches have accurate results, they often require much more computation time due to the large number of simulations in the optimization process. As reported in previous studies, several hours are often required to optimize a typical-sized circuit. Equation-based optimization, such as geometric programming (GP) based analog circuit synthesis [7, 8], is another popular approach with fast computation time. In [9, 10], the traditional design centering concept is included in the GP-based analog circuit synthesis by maximizing the distance to all the boundaries. However, as studied in many related researches [11], the center of feasible space is not necessarily the nominal point with maximum yield. Because the process sensitivity of different circuit performance could be different, the weight of the distance to each feasible boundary should be different, too.

In [5, 11], the concept of worst-case distance (WCD) is introduced to provide a quick estimation of the design yield. The similar concept is also applied to performance space, which is called the process capability (C_{pk}) in [6], for yield evaluation. The key idea is to normalize the distance to the feasible boundary by the standard deviation (δ) of its performance distribution to consider different process sensitivity. Using this metric to evaluate the design yield could be more accurate than using the row distance only, as illustrated in Fig. 2. However, the performance distribution and process sensitivity may vary at different nominal point. The corresponding C_{pk} should be recalculated also at different nominal point. Since C_{pk} is not a fixed equation, it can only be used with the simulation-based optimization in previous approaches [5, 6] to guide the yield-aware analog circuit synthesis, which requires more computation efforts.

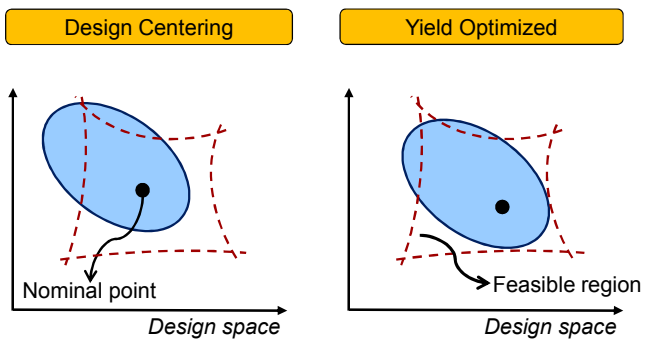

Figure 2. Yield optimization with different process sensitivity

In this paper, an automatic synthesis methodology is proposed for the analog circuits with flexible TFTs. The different properties of flexible TFTs such as bending and large V_{th} variation are considered in the optimization algorithm to solve the main difficulty of designing the analog circuits with flexible electronics. All the assumptions and probability calculations are re-examined in this work to deal with non-symmetrical variations. A modified equation-based variance analysis approach is also proposed to calculate the C_{pk} of each performance without simulations. Therefore, C_{pk} can be used in equation-based optimization as well to improve the accuracy of yield prediction for each possible solution. As demonstrated in the experimental results, accurate prediction of performance distribution can effectively guide the yield-aware synthesis to a point with optimized performance and less over-design.

The rest of this paper is organized as follows. The key ideas of the proposed optimization approach are explained in Section 2. In Section 3, the equation-based variance analysis is presented for the evaluation of design yield. Section 4 demonstrates the experimental results and shows the improvements compared to the previous approach. Finally, a conclusion is drawn in Section 5.

II. PROPOSED YIELD-OPTIMIZED SYNTHESIS

One of the major problems in GP-based analog synthesis approaches is the regression errors while fitting those GP equations. Large prediction errors often exist in some transistor parameters, such as g_{ds} and g_m, which can lead to significant prediction errors in some circuit performance. As reported in previous work [8], g_m can be quite different with different transistor width, whose relationship is not a simple linear function. However, there is another parameter g_m/I_d in the basic transistor equations, which is a universal value that is independent to the device sizes. Once the three node voltages of a transistor is determined, its g_m/I_d value is almost a constant no matter what its size is. If g_m/I_d is used instead of g_m, the modeling issue may become easier to be solved. Therefore, this concept has been used in analog design for a few years [12].

In this paper, this g_m/I_d design concept is applied on equation-based optimization to solve the accuracy issue with less overhead. Because the g_m/I_d value is determined by the node voltages of the transistor, the unknown variables in the performance equations are transformed to the bias voltage of each internal node and the DC current of each path from VDD to ground. Once these variables are obtained, the W/L ratio of each device can be easily determined by its node voltages and required current. By using this approach, the convergence problem of DC operating points can be solved automatically. Since only the three terminal voltages of a transistor are required to model those transistor parameters, lookup-table (LUT) based models are adopted in this work to avoid the regression errors while building the GP equations. A table-assisted sizing approach is then performed to determine the device sizes according to those node voltages. The details of each step will be explained in the following sections.

A. Bias-Driven Sizing Approach

In order to explain how the unknown variables in the performance equations are transformed to the bias voltage of each internal node and the DC current of each path, the OPA with flexible TFTs shown in Fig. 3 [13] is used as an example to discuss the whole procedure. The formulations for other circuits can be derived by the similar way. Due to the symmetry property of the circuit, many matching groups are identified before the design flow. In DC analysis, the input voltages (V_{i-}, V_{i+}) and output voltage (V_o) are set as their common mode voltages, which are often 1/2 VDD. The left unknown node voltages are V_{B1}, V_{B2}, V_{d1}, V_{d5}, V_{d6} and V_{d10}. Besides the node voltages of a transistor, its current from drain to source (I_{ss}) is also required to determine its device size. Therefore, I_{ss} is added as the unknown variables in the following equations.

In all approaches, the first constraint is to keep each device in the proper working mode. The external bias voltage V_{B1} is to provide enough voltage so that M_5 can be turned ON. In the similar way, the external bias voltage V_{B2} is to provide enough voltage so that M_{10} can be turned ON. About the internal voltages V_{d1}, V_{d5}, V_{d6} and V_{d10}, they cannot be directly set from users like V_{B1} and V_{B2}. Therefore, designers have to adjust proper device sizes such that those internal voltages can keep all transistors operate in saturation mode.

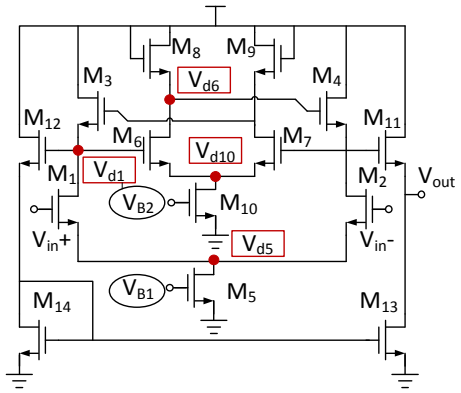

Figure 3. OPA schematic [13]

However, operating in saturation mode does not guarantee that the circuit performance can reach the required specifications, especially for tough specifications. It implies that keeping each device in the desired working mode is not enough to find proper bias points. More constraints should be derived from the target specifications. Referring to the previous studies [13], the performance equations of this OPA circuit can be derived in the g_m/I_d form. They are used in the optimization engine to check if the present design meets all specification as shown in Eq. (1), in which P_j is the equation of performance j and $Spec_j$ is the specification of this performance. The $\frac{g_m}{I_d}$, $\frac{g_{ds}}{I_d}$ and $\frac{C}{I_d}$ of each transistor can be obtained via its node voltages (V_g, V_d, V_s) through pre-built transistor parameter models, as shown in Eq. (2).

$$\left|\mathrm{P_j}\left(\frac{\mathrm{g_m}}{\mathrm{I_d}},\frac{\mathrm{g_{ds}}}{\mathrm{I_d}},\frac{\mathrm{C}}{\mathrm{I_d}},\mathrm{I_d}\right)-\mathrm{Spec_j}\right|\le 0 \tag{1}$$

$$\left(\frac{\mathrm{g_m}}{\mathrm{I_d}},\frac{\mathrm{g_{ds}}}{\mathrm{I_d}},\frac{\mathrm{C}}{\mathrm{I_d}}\right)_\mathrm{i}=\mathrm{Table}(\mathrm{V_{g,i}},\mathrm{V_{d,i}},\mathrm{V_{s,i}}) \tag{2}$$

After the bias voltage of each node and the drain current (I_d) for each transistor are identified, the size of each transistor can be determined also. Because there are two variables (W/L) that determine the MOS current, analog designers often fix the channel length (L) at a proper value and leave only one variable (W) in the sizing flow to simplify the problem. The same assumption is also adopted in this work at this step.

Actually, deriving the corresponding device size from the basic MOS current equation is not accurate due to the non-ideal second-order effects. Therefore, this work adopts a table-based approach to find the corresponding transistor sizes. Under different combinations of node voltages, the corresponding I_d of a unit-size transistor is recorded in a pre-built table. Then, multiplied by its bias current can obtain the approximate transistor size for this case. Using this approach, the device sizes can be obtained quickly and accurately. Since building the sizing table is a one-time effort that can be built in advance, this approach greatly improves the efficiency of circuit sizing and optimization.

B. Yield-Aware Optimization Flow

Fig. 4 shows the proposed optimization flow for the analog circuit sizing problem in flexible electronics. Given the circuit database (netlist, performance equations and process information) and the

required specifications, the constraints and cost function for the mathematical solver are setup at the first step. After that, the best bias voltages and bias currents that make the circuit satisfy all specifications with optimized cost are identified by a non-linear programming (NLP) solver with the pre-built tables of transistor parameters. The C_{pk} of each possible design point is also calculated directly in the mathematical solver to optimize the design yield simultaneously, which will be explained in the next section. Finally, the size of each transistor is determined by the bias voltage and bias current with a pre-built sizing table. Without yield consideration, the optimization object is to minimize the power consumption of this circuit, e.g. $min\ (V_{dd} \cdot \sum_i I_{ss,i})$.

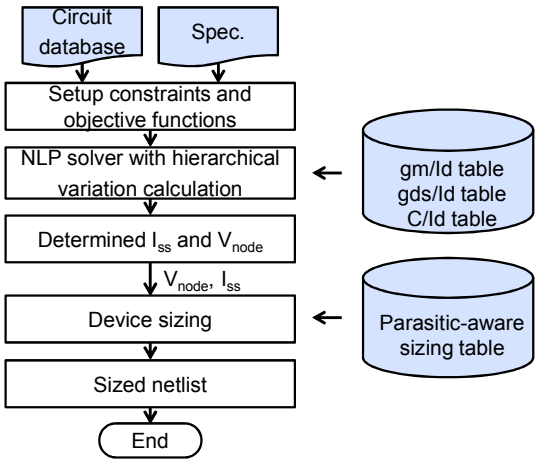

Figure 4. Proposed yield-optimized synthesis flow

III. EQUATION-BASED VARIANCE ANALYSIS

Because different process sensitivity is not considered in previous approaches, maximizing the row distances to all feasible boundaries may not achieve the highest yield. In order to normalize the distance to each feasible boundary by its standard deviation (δ), the performance distribution at present nominal point should be evaluated first. The typical approach is to collect the statistical data through simulating many instances of the circuit. However, this approach requires large computation efforts and cannot be used with equation-based optimization to provide fast yield optimization.

In this paper, an equation-based variation analysis method is proposed to calculate the variance of each performance in flexible electronics without simulations. This allows C_{pk} to be used in equation-based optimization as well to improve the accuracy of yield prediction and still keep the efficiency. Although there are some analytical variance calculation methods [14] proposed in the literature, they have a basic assumption that the probability distribution is a normal distribution. However, the mobility change of the flexible TFTs under bending is not a symmetrical distribution (-25%~10%), which violates the assumption of normal distribution in previous works. Therefore, log-normal distribution is adopted in this work to model the parameter variations. All the calculation steps are modified in this work deal with non-symmetrical variations.

In order to calculate the C_{pk}, the system behavior is modeled as a 3-level hierarchy without losing generality, as shown in Fig. 5. The bottom level represents the variations of process parameters, such as width (W), length (L), threshold voltage (V_{th}), mobility (μ), etc. Those data can be obtained from the process model. The intermediate level represents the variations of transistor parameters, such as transconductance (g_m), drain current (I_d), output conductance (g_{ds}), etc. Those variations are calculated from the process-level variations. The top level represents the variations of system-level performances, such as gain, bandwidth, phase margin, etc. Those variations are calculated from the intermediate-level variations.

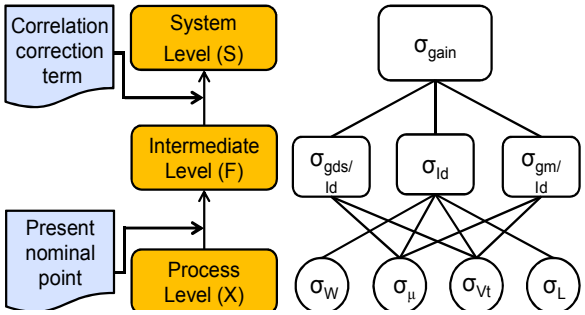

Figure 5. Hierarchical variance calculation

Because the process-level variations are given as independent random variables in the process model, they are also assumed as independent variables in this work. For each intermediate parameter F_i, $C_{X_i}^{F_j}$ is defined as its partial derivative with respect to a process parameter X_i, as shown in Eq. (3). By using the first order Taylor series expansions, the intermediate parameter F_i can be written as Eq. (4). The variance of this intermediate parameter (σ^2_{Fj}) can be defined as Eq. (5), in which μX_i is the mean value of process parameter X_i. Once the present nominal point of the design is determined, the partial derivation and the mean value of each X_i are determined. It implies that the variance of each intermediate parameter can be calculated through the following equations without simulations.

$$C_{X_i}^{F_j} = \frac{\partial F_j}{\partial X_i}\Big|_{(X_1, X_2, \dots)} \tag{3}$$

$$\mathrm{F}_j = \mathrm{F_j}(\mu_{\mathrm{X1}}, \mu_{\mathrm{X1}}, \dots) \tag{4}$$

$$\sigma_{F_j}^2 = \mathrm{E}\left\{\left[\sum_{i=1}^{n_x} C_{X_i}^{F_i}\left(X_i - e^{\mu_x + \frac{\sigma_x^2}{2}}\right)\right]^2\right\}$$

$$= \sum_{i=1}^{n_x} C_{X_i}^{F_i} C_{X_i}^{F_i} e^{(2\mu_x + \sigma_x^2)} \cdot (e^{\sigma_x^2} - 1) \tag{5}$$

$$\sigma_H^2 = \sum_{j=1}^{n_F} \sigma_{F_j}^2 + CCT \tag{6}$$

$$\mathrm{CCT} = \sum_{i=1}^{n_X} \sum_{\substack{j,h=1,\\ \mathrm{j}\neq\mathrm{h}}}^{n_F} \left(C_{F_j}^H C_{X_i}^{F_j}\right)\left(C_{F_h}^H C_{X_i}^{F_h}\right)\sigma_{X_i}^2 \tag{7}$$

Unlike the process parameters, the intermediate-level parameters are often highly correlated to each other. While calculating the variations of system-level performances from the intermediate-level variations, the correlations between those transistor parameters should be properly considered. Therefore, an additional correlation correction term (CCT) is required in the variance calculation of system-level performances, as shown in Eq. (6). This CCT term can be derived from the intermediate-level parameters that are functionally related to this system-level parameter S_i, as shown in Eq. (7). Finally, the C_{pk} of each performance can be obtained by dividing the distance between the nominal point and its performance boundary D_k with the calculated performance variance.

With the proposed variance calculation, the overall C_{pk} of this design can be calculated immediately for each possible solution during the optimization process, as shown in Equation (8). No simulations are required at all. In traditional design centering approaches, only the row distance from the nominal point to each boundary is considered as shown in Equation (9). In this work, Equation (8) is used instead to guide the optimization results toward higher design yield. The objective function of the optimization engine is then modified as Equation (10), in which α and β are two user-defined parameters to represent the relative importance of the two costs in this design case.

$$C_{pk}(V_{gs}, V_{ds}, I_x) = \frac{|P_i - Spec_i|}{variance_i} \quad (8)$$

$$Row\_Dis(V_{gs}, V_{ds}, I_x) = \sum_{i=0}^{S_n} |P_i - Spec_i| \quad (9)$$

$$cost = \alpha \cdot Power + \beta \cdot C_{pk} \quad (10)$$

IV. EXPERIMENTAL RESULTS

In this section, the proposed circuit sizing flow for flexible electronics are demonstrated on the OPA circuit shown in Fig. 3 with ITRI a-Si 8μm technology. The circuit simulation results are obtained from HSPICE. In flexible electronics, the mobility (μ) and threshold voltage (V_t) of TFTs can have large variations. Referring to the reported data in previous researches, the variations of these two parameters are assumed as -25%~+10% (for μ) and ±20% (for V_t) respectively. The variations of the device sizes (W and L) are assumed as ±3% respectively. Those parameter variations are used to perform Monte Carlo analysis in HSPICE to evaluate the design yield. According to the proposed algorithm, a simple synthesis tool has been implemented with C++. The adopted mathematical solver to solve those convex equations is the NLP solver in Matlab. All the results are measured on the same machine with Intel Xeon quad-core processor at 2.67GHz and 4GB memory.

With the same OPA case, the optimization results of different equation-based approaches are compared in TABLE I. Simulation-based approaches are not compared in the experiments because they use quite different optimization mechanism that requires much longer computation time. In order to make a fair comparison, the three approaches use the same optimization engine mentioned in Section 2. Only their objective functions are different. The column "w/o yield" shows the power-optimized synthesis results without yield consideration. The column "distance" shows the yield-optimized synthesis results by maximizing the row distance to each performance boundary, which is similar to the approach proposed in previous papers [9, 10]. The column "C_{pk}" shows the synthesis results by the proposed approach with the objective function mentioned in Section 3, which tries to optimize the power and yield simultaneously with equal weights. The power consumption, the total transistor area, the design yield evaluated by a 1000-run Monte Carlo simulation, and the total computation time for the synthesis procedure of each circuit are reported in the row "Overall Results".

According to the yield analysis results, the original synthesis result shows low design yield (yield=53.1%) without yield consideration. Although the row distance method can improve the design yield to 71.2%, this approach cannot reach the highest design yield because the variance of performance distributions is not considered. Its power consumption and total transistor area are also the highest among all approaches, which implies that this approach may over-design too much. With accurate yield prediction from the proposed approach, the design yield of the synthesized circuit can be further improved with significant reduction on power and area overhead. Monte Carlo analysis shown in Fig. 6 also demonstrates this trend of yield improvement.

TABLE I. The optimization results on the OPA case

Performance		w/o yield	distance	C_{pk}
Gain (dB)	≥ 15	15.1	21.7	19.2
GB (kHz)	≥ 2	2.5	3.5	3.0
SR (V/ms)	≥ 2	6.26	11.5	9.6
PM (degree)	≥ 60	93.5	61.7	72.9
Overall Results	Power(mW)	142	331	155
	Overhead (%)	-	133.1	9.1
	Area (μm²)	274.3	507.7	339.0
	Overhead (%)	-	1750.3	23.7
	Yield (%)	53.1	71.2	100.0
	Time (sec.)	< 1	< 1	< 1

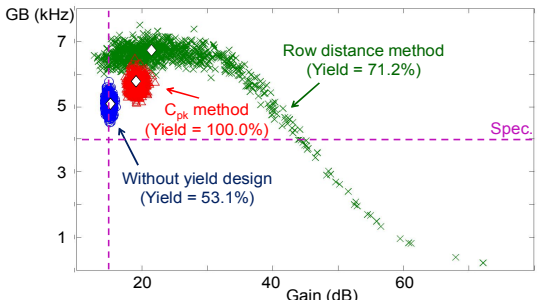

Figure 6. Performance distribution of the OPA case

V. CONCLUSIONS

In this paper, an automatic robust optimization technique is proposed for flexible electronics to deal with the severe parameter variations. The C_{pk} concept is integrated into equation-based sizing approach in this work to optimize the design yield with accurate variation consideration. The different properties of flexible TFTs are also considered in the optimization algorithm. To the best of our knowledge, this might be the first work on automatic circuit sizing for flexible electronics with reliability consideration. As shown in the experimental results, the proposed approach can further improve the design yield to almost 100% with great reduction on area and power overhead. Those results have demonstrated that the proposed approach is able to help designers solve the main difficulty of designing the analog circuits with flexible electronics.

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