A Fast and Effective DFT for Test and Diagnosis of Power Switches in SoCs

Xiaoyu Huang, Jimson Mathew, Rishad A. Shafik, Subhasis Bhattacharjee, Dhiraj K. Pradhan
Department of Computer Science, University of Bristol, UK; E-mail: csxjm@bristol.ac.uk.

***Abstract*— Power switches are increasingly becoming dominant leakage power reduction technique for sub-100nm CMOS technologies. Hence, fast and effective DFT solution for test and diagnosis of power switches is much needed to facilitate faster identification of potential faults and their locations. In this paper, we present a novel, coarse-grain DFT solution enabling divide and conquer based test and diagnosis solution of power switches. The proposed solution benefits from exponential time savings compared to previously reported solutions. Our DFT solution requires only $(2\lceil\log_2 m\rceil + 3)$ clock cycles in the worst case for test and diagnosis for m-segment power switches. These time savings are further substantiated by effective discharge circuit design, which eliminates the possibility of false test and hence significantly reducing the charge and discharge times. We validated the effectiveness of our proposed solution through SPICE simulations on a number of ISCAS benchmark circuits, synthesized using 90nm gate libraries.**

I. Introduction

Continued process technology scaling has enabled the development of ever more efficient electronic devices with high integration capacity for current and future generation systems-on-chip (SoCs). However, with these technological developments the leakage power consumption is increasingly becoming dominant in overall circuit power consumption, particularly for sub 100-nm CMOS devices. To reduce the leakage power effectively, researchers have recently proposed power gating technique [1]. The basic principle is to add header transistor switches (PMOS) or footer transistor switches (NMOS) in the circuits such that these transistors can be turned off in inactive (i.e. sleep or standby) mode of operation to reduce leakage power consumption [2]. The placement of these switches can be carried out in coarse-grained or fine-grained fashion. Recently there are proposals for fine-grained power-gating design flows mostly using the standard cell design automation tools [6], [8]. However, multiple supply voltages together with the power switches are increasingly problematic in testing and validation of the chip considering variations in process, voltage and temperature (PVT). Moreover, the area and performance overheads for fine-grained power switches can prove to be costly [4]. As an alternative the coarse grain power gating has more recenty been proposed in [6], which trades off performance and area overheads for reduced leakage power consumption.

Effective DFT solution for power gating switches is an emerging design requirement for identifying faults (i.e. stuck-open and stuck-short) and their locations (i.e. fault diagnosis). However, incorporating such DFT solution with traditional DFT rules for functional circuits can scale poorly due to the following reasons. Firstly, isolating a stuck-at fault in the power gating circuit using traditional functional DFT can be highly challenging since such fault may not affect the underlying functionality. Secondly, testing of all power management specific rules (such as validating power control signals and their mutual inter-dependence) is not feasible using traditional functional DFT solution. Hence, many EDA vendors are actively considering development of power test access mechanism (PTAM), particularly for power gating circuits [7]. However, to date there has been limited research work in this area (summary of previous works with illustrative example test patterns is shown in Section II). Recently proposed DFT solutions, such as [3], [5], [6] have the following limitations. Firstly, testing speed is limited as power switch segments are serially tested incurring more than $2m$ cycles for m-segment power switches [3], [6]. Moreover, these solutions do not identify the locations of faults in power switches.

In this paper, we propose a fast and effective DFT solution for power switches. Our proposed solution is fast as it takes only $(2\lceil\log_2 m\rceil + 3)$ clock cycles in the worst case for m-segment power switches, resulting in an exponential time savings. Moreover, the proposed solution is effective as it identifies all possible fault locations in the power switches. To the best our knowledge, this is the first proposal that considers an effective test and diagnosis solution for single stuck-open and testing of multiple stuck-short faults in power switches. The rest of the paper is organized as follows. Section II presents related works and various issues with the existing DFT solutions for testing power switches. Section III outlines the proposed testing and diagnosis solution, while Section IV discusses experimental setup and results. Finally, Section V concludes the paper.

II. Related Works and Motivation

The power switches are usually implemented using multiple transistor segments, where every segment can contain one or more transistors that share common drain, gate, source and bulk material [3]. Such segment based implementation of power switches greatly improves Design for Manufacturability (DfM) and also minimizes the power supply or ground (i.e. VDD or GND) bounce in low voltage operations [1]. Furthermore, due to this segment based switching, the problem of testing the power switches is reduced to the testing of each segment.

Goel *et al.* [3]and Kassab *et al.* [5] proposed DFT solutions for testing stuck-open and stuck-short faults in power switches. The DFT solution proposed in [3] enables testing on/off functionality of power switches in both fine-grain and coarse-grain designs. On the other hand, DFT solution in [5] addressed the problem of long discharge time, showing effective discharge

978-3-9815370-0-0/DATE13/© 2013 EDAA

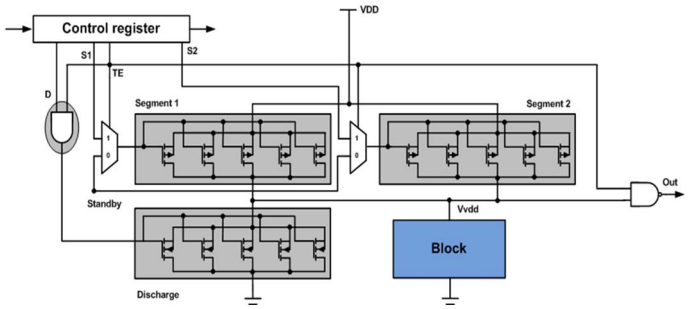

Fig. 1. Existing DFT for corase-grain power switches [6]

circuit design to improve test speed. Recently, Khursheed et al. [6] also investigated the long discharge time when power switches are turned-off, highlighting effective testing solutions for coarse-grain power switches. Fig. 1 shows a typical DFT circuit with m segments, proposed by Khursheed *et al.* [6]. It consists of a control register, a set of multiplexers to enable the test mode, an AND gate to enable testing and a discharge mode. Table I shows the test vectors to test a design shown in Fig. 1 assuming two segments (i.e. m=2). As can be seen, the first test cycle turns off both power switch segments (Seg. 1 and Seg. 2) and turns on the discharge transistors to quickly discharge the voltage at V_{vdd}. The second test cycle turns off the discharge transistors to test for stuck-short at either of the two power switch segments. The third test cycle turns on all power switches in Seg. 1, while power switches in Seg. 2 and discharge transistors are switched off. This test cycle charges up the V_{vdd} through power switches in Seg. 1 and is used to test for stuck-opens on transistors of Seg. 1 and stuck-shorts on the discharge transistors. The fourth test cycle turns off both

TABLE I

TEST PATTERNS FOR POWER SWITCHES WITH TWO SEGMENTS (m=2) [6]

	TE=1		Disch.	V_{vdd}	Out		Outcome
Cycle	S1	S2			Fault	Faulty	
1	1	1	1	0	1	0	Discharge
2	1	1	0	0	1	0	Seg.1 Short& Seg.2 Short
3	0	1	0	1	0	1	Seg. 1 Open &DT^* Short
4	1	1	1	0	1	0	Discharge & DT^* Open
5	1	0	0	1	0	1	Seg. 2 Open DT Short

DT: Discharge Transistor

power switch segments and turns on the discharge transistors to discharge voltage at V_{vdd} that was charged up in the previous test cycle. This test cycle is also used to test stuck-open fault on the discharge transistors. The last test cycle is used to test stuck-open on power switches in Seg. 2 by turning off the power switches in Seg. 1 and discharge transistors. In general $(2m + 1)$ test cycles are needed to test a design with m power switch segments and a discharge segment using the DFT (Fig. 1). For designs with more than two power switch segments, fourth test cycle (Table I) are repeated after applying stuck-open test at each segment other than the last segment, to discharge the voltage at V_{vdd} and to prepare for the next test cycle.

The above DFT solution saves the test time through balanced charge and discharge time. However, since the power switch segments are tested one by one, the test time increases linearly with the number of segments. For large number of power switch segments in complex systems, the test time overhead can be substantial. To mitigate this issue, control register needs to incorporate faster test control approach, which is the main motivation of our work. Moreover, recently proposed DFT solutions do not effectively identify the location of faults, which is much required for post-manufacturing re-configuration for improving circuit yield. Underpinning these motivations, we propose a novel DFT solution for test and diagnosis power switch segments with divide and conquer based control solution using delay information to capture the test results in consecutive cycles. As a result, significant test speedup can be achieved.

III. PROPOSED DFT SOLUTION

To reduce the large number of test cycles, the proposed DFT soluton employs divide and conquer based testing of power switch segments. Fig.2 shows the proposed DFT circuit for test and diagonosis of coarse-grain design with six segments. The 'nand2' is used to generate the reference signal (FE) when the power switch segments are turned on. This reference signal is then delayed into four consecutive cycles by the delay elements. These delayed signals are named as FE1, FE2, FE3 and FE4 with delays of $(\Delta 1)$, $(\Delta 1 + \Delta 2)$, $(\Delta 1 + \Delta 2 + \Delta 3)$, and $(\Delta 1 + \Delta 2 + \Delta 3 + \Delta 4)$, respectively. The sampling registers are triggered using these signals to capture the output of the 'nand1' (d). The delay pattern at node d indicates the test result. The delay elements are carefully designed to match delay pattern such that when a certain number of segments are turned on, there is a unique four bit output code registered at the output. For example, if three segments are turned on, the output code of the flip-flop will be '1000'; while if two segments are turned on, the output code will be '1100'. Therefore if the output code is '1100' when three segments are turned on, that means one of the three segments has stuck-open defect. For diagnosis, $(m/2)$ power switch segments are turned on in the first step, and then in each of the following steps, the number of the segments to be turned-on will be the half of the number segments in the previous step (or half plus one if the number is odd). This is carried out until we find the faulty segment. The selection of the half part from a group of segments is based on the previous output of the registers. Fig. 3 shows the flow chart of the proposed test and diagnosis solution. The flow chart demonstrates how fast testing is performed for multiple stuck-short or stuck-open faults and also how diagnosis is effectively carried out for locating the segment with stuck-open fault with an example of power switches of six segments. As can be seen, in the first step half of the six segments in the left hand side are turned on. The value of Q2='0' indicates that the three segments in the left hand side are working properly and hence, the stuck-open fault should be in the other side. If, however the value of Q2 is '1', it indicates that the faulty segment should be within the three segments in the left hand side. Assuming that the faulty segment is in the left hand side, the second step both 'Seg1 and 'Seg2' segments are turned on. After this step, if Q3 is '0', it indicates that the 'Seg1' and 'Seg2' are working properly and the segment 'Seg.3' has stuck-open fault. If however, Q3 is '1', open fault can be in either of 'Seg1' or 'Seg2' segement. In such case, the solution proceeds with the third step, which turns on only 'Seg1'. After this step, if the Q4 is '0', it shows that the 'Seg1' is working properly and the 'Seg2' has a stuck-open fault. Otherwise, 'Seg1' is deemed as faulty.

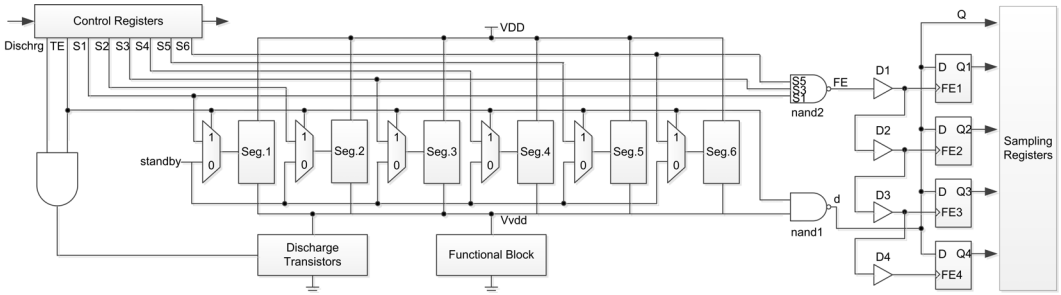

Fig. 2. Circuit diagram of test and diagnosis control in the proposed DFT solution

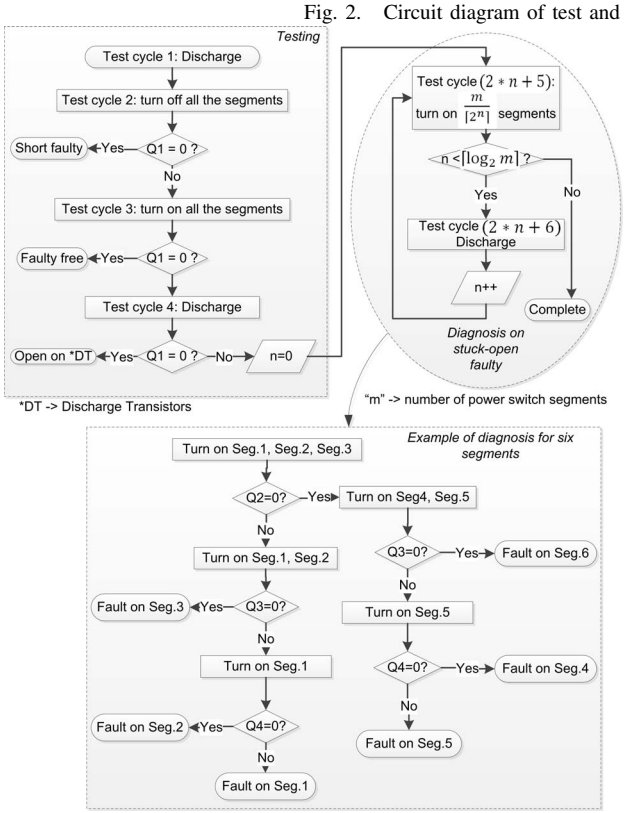

Fig. 3. Flow chart of test and diagnosis steps in the proposed DFT (Fig. 2)

The test results from the sampling registers are interpreted using the output delay signals to detect stuck-open faults. Fig. 4 shows the timing diagram generated by these delay signals. As can be seen after the delay signal FE1, if the output d is '0' (i.e. $Q1 = 0$), all six segments can be considered as functional (no fault). However, when d is '1' (i.e. $Q1 = 1$) after this delay interval (i.e. $\Delta 1$), five segments are functional, while one other is considered faulty. Similarly, after the delay signal FE2 (when the half of the segments has been enabled), if d is 0 (i.e. $Q2 = 0$), three segments are considered not faulty and when d is 1 (i.e. $Q2 = 1$) one of the segments is deemed as faulty. The other delay signals (FE3 and FE4) also generate similar timing information and generate outputs ($Q3$ and $Q4$) to indicate fault-free and faulty cases through output of the nand1, d. The final step identifies the faulty segment.

Table II shows the test vectors for a design using the proposed DFT solution (Fig.2).The first four cycles tests for the short and open defect in power switch segments and in the discharge segment, while the rest of test cycles carries out the diagnosis of the open defect in power switch segments (odd cycles) and for discharge (even cycles). The discharge cycles and the second

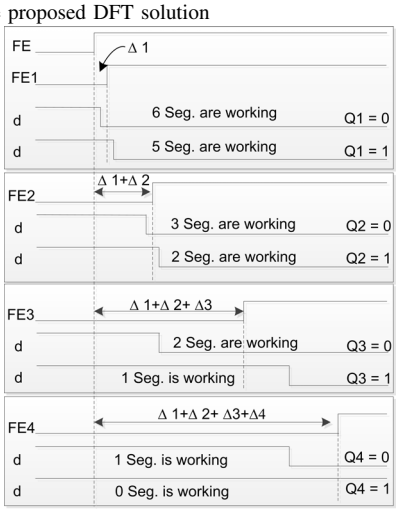

Fig. 4. Timing diagram with six segments

cycle for testing short defects on all the segments are similar to the previous test vectors shown in Table I. The values in output flip-flops Qn indicate whether group of segments being tested is faulty or not. The odd cycles (except the first cycle) are for test and diagnosis of the open defect in power switch segments. For example, as can be seen the value of $Q1$ in test cycle 3 indicates if there is open defect in all power switch segments, and the values of $Q2$ in cycle 5, $Q3$ in cycle 7 and the $Q4$ in cycle 9 shows the location of the power switch segment with open defect. Table III shows the details of the test patterns for diagnosis. In general $(2\lceil \log_2 m \rceil + 3)$ test cycles are needed to test a design with m power switch segments plus a discharge segment using the proposed DFT solution (Fig. 2). Table III shows the input and output codes of the flip-flops resulting from the test patterns (Table II) for the cases when different segment of power switches with six-segment has stuck-open fault. As can be seen, in the first step the output of the second flip-flop ($Q2$) is considered, while in the second step the output of the flip-flop in the next stage ($Q3$) is considered. The testing steps are further carried out until the faulty segment can be found out.

IV. Experimental Results

To validate the effectiveness of our proposed DFT solution (Fig. 2) a number of experiments have been carried out on various ISCAS benchmark circuits using ST 90nm process technology libraries. First, the timing data corresponding to the turn-on behaviour of the power switches is characterized using HSPICE. This data is then used for designing the delay elements, which are integrated in the circuit under test along with the power switches (Fig. 2).

TABLE II

TEST PATTERNS FOR TEST AND DIAGNOSIS OF STUCK-OPEN FAULTS

	Test cycles	Test Time (s) S1	S2	S3	S4	S5	S6	Dis.	Vdd Fault	Q Fault-free		Justification
Test	1	1	1	1	1	1	1	1	0	1	0	Discharge
	2	1	1	1	1	1	1	0	0	1	0	Short on all PS Segs.
	3	0	0	0	0	0	0	0	1	0	1	Open on PS Segs.
	4	1	1	1	1	1	1	1	0	1	0	Discharge *DT open
Diagn.	5	Step 1 diagnosis on stuck-open faulty						0	-	-	-	See Table III
	6	1	1	1	1	1	1	1	0	1	0	Dicharge
	7	Step 2 diagnosis on stuck-open faulty						0	-	-	-	See Table III
	8	1	1	1	1	1	1	1	0	1	0	Discharge
	9	Step 3 diagnosis on stuck-open faulty						0	-	-		See Table III

TABLE III

TEST PATTERNS FOR DIAGNOSIS ON STUCK-OPEN FAULT

Fault on Seg.1		Step1	Step2	Step3
Input	S1	0	0	0
	S2	0	0	1
	S3	0	0	1
	S4	0	1	1
	S5	1	1	1
	S6	1	1	1
Output	Q1	1	1	1
	Q2	1	1	1
	Q3	0	1	1
	Q4	0	0	1

Fault on Seg.2		Step1	Step2	Step3
Input	S1	0	0	0
	S2	0	0	1
	S3	0	1	1
	S4	1	1	1
	S5	1	1	1
	S6	1	1	1
Output	Q1	1	1	1
	Q2	1	1	1
	Q3	0	1	1
	Q4	0	0	0

Fault on Seg.3		Step1	Step2	Step3
Input	S1	0	0	-
	S2	0	0	-
	S3	0	1	-
	S4	1	1	-
	S5	1	1	-
	S6	1	1	-
Output	Q1	1	1	-
	Q2	1	1	-
	Q3	0	0	-
	Q4	0	0	-

Fault on Seg.4		Step1	Step2	Step3
Input	S1	0	1	1
	S2	0	1	1
	S3	0	1	1
	S4	1	0	1
	S5	1	0	0
	S6	1	1	1
Output	Q1	1	1	1
	Q2	0	1	1
	Q3	0	1	1
	Q4	0	0	0

Fault on Seg.5		Step1	Step2	Step3
Input	S1	0	1	1
	S2	0	1	1
	S3	0	1	1
	S4	1	0	1
	S5	1	0	0
	S6	1	1	1
Output	Q1	1	1	1
	Q2	0	1	1
	Q3	0	1	1
	Q4	0	0	1

Fault on Seg.6		Step1	Step2	Step3
Input	S1	0	1	-
	S2	0	1	-
	S3	0	1	-
	S4	1	0	-
	S5	1	0	-
	S6	1	1	-
Output	Q1	1	1	-
	Q2	0	1	-
	Q3	0	0	-
	Q4	0	0	-

Table IV compares the test and diagnosis times of the proposed DFT solution with previously reported DFT solution [6]. The comparison highlights the approximate test time savings in terms of number of hours saved per million tested devices using the proposed DFT solution. The same clock speed of 650 MHz is applied as the representative test clock frequency for a given circuit. The test times of the DFT solutions in comparison depend on the number of the segments m and the number of test clock cycles required for testing the power switches. The number of test clock cycles needed by [6] is $(2 * m + 1)$, while that for our DFT solution is $(2 \lceil \log_2 m \rceil + 3)$. The first column shows the different number of the segments, while the next two columns show the test time (seconds per tested device) for testing power switches using both DFT solutions. The following column shows the test time savings (i.e. hours per million tested devices) of the proposed DFT solution compared to [6] and the last column indicates the speedup of the proposed DFT solution (normalized by the previously proposed DFT [6]). As can be seen, while the test time required by [6] increases linearly with the number of the segments in power switches, our proposed DFT gives exponential savings for the same number of segments in power swithces. Moreover, when the device is fault-free, our solution completes testing in 4 cycles regardless of the number of segments. However, in the DFT solution [6], all the segments have to be tested one by one even though the device is fault-free and that will give the worst case delay of $(2m + 1)$ test cycles. Comparing the testing speeds between the DFT solutions, it can be seen that our DFT solution achieves a speedup of about three orders of magnitude for 6-segment power switches, suggesting that the proposed DFT solution is an attractive option for testing power switches for SoCs with a large number of segments. Furthermore, our proposed DFT approach effectively identifies the location of single faults through divide and conquer based test control (Fig. 3).

TABLE IV

TEST TIME COMPARISONS OF THE PROPOSED DFT SOLUTION

Total Seg(m)	Test Time (s) DFT in [6]	(a,m)	Saving (hrs) per million (Proposed DFT)	Speedup
1.00E+03	3.08E-06	3.54E-08	8.45E-04	8.70E+01
5.00E+03	1.54E-05	4.46E-08	4.26E-03	3.45E+02
1.00E+04	3.08E-05	4.77E-08	8.53E-03	6.45E+02
5.00E+04	1.54E-04	5.38E-08	4.27E-02	2.86E+03
1.00E+05	3.08E-04	5.69E-08	8.55E-02	5.41E+03
5.00E+05	1.54E-03	6.31E-08	4.27E-01	2.44E+04
1.00E+06	3.08E-03	6.62E-08	8.55E-01	4.65E+04
5.00E+06	1.54E-02	7.54E-08	4.27E+00	2.04E+05
1.00E+07	3.08E-02	7.85E-08	8.55E+00	3.92E+05

V. CONCLUSIONS

An effective DFT solution for testing and diagnosis of the power switches suitable for state-of-the-art system-on-chip (SoC) is proposed. The proposed solution employs divide and conquer based test control steps to generate unique timing pattern at the output for a given test scenario (faulty or fault-free) and to identify the fault location (when faulty). The DFT solution has been validated through circuit simulations on different ISCAS benchmark circuits, showing exponential speedup over previously reported solutions. Integrating our test solution to design flow to facilitate automatic delay segment selection is being considered for future work.

REFERENCES

[1] K. Roy *et al.*, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," in *Proc. of the IEEE*, vol.91, no.2, Feb. 2003.

[2] K. Agarwal *et al.*, "Power gating with multiple sleep modes," in *Proc. of the 7th International Symposium on Quality Electronic Design (ISQED)*, pp. 633–637, 2006.

[3] S.K. Goel *et al.*, "Testing and diagnosis of power switches in SOCs," in *Proc. of European Test Symposium (ETS)*, May 2006.

[4] K. Usami and N. Ohkubo, "A Design Approach for Fine-grained Run-Time Power Gating using Locally Extracted Sleep Signals," in *Proc. of Intl. Conf. on Computer Design (ICCD)*, pp. 155-161, Oct. 2006.

[5] M. Kassab and M. Tehranipoor, "Test of Power Management Structures," in *Power-Aware Testing and Test Strategies for Low Power Devices*, P. Girard *et al.*, Eds. Springer, ch.10, pp. 295-322, 2009.

[6] S. Khursheed *et al.*, "Improved DFT for Testing Power Switches," in *Proc. of European Test Sympoisum (ETS)*, pp. 7-12, 2011.

[7] V. Chickermane *et al.*, "A Power-Aware Test Methodology for Multi-Supply Multi-Voltage Design," in *Proc. of International Test Conference (ITC)*, Santa Clara, CA, USA, paper 9.1, Oct. 2008.

[8] R. Lin *et al.*, "Power gating design for standard-cell-like structured ASICs," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 514-519, 2010.

[9] Y. Zorian *et al.*, "Testing Embedded Core Based System Chips," in *Proc. IEEE International Test Conference (ITC)*, pp. 130-143, 1998.

[10] S.K. Goel *et al.*, "Test Infrastructure Design for the Nexperia™ Home Platform PNX8550 System Chip," in *Proc. of IEEE Design Automation and Test in Europe (DATE)*, pp. 108-113, 2004.