A Dynamic Self-Adaptive Correction Method for Error Resilient Application

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Abstract— The aggressive scaling down technology has posed transistor aging to be a new challenging to the reliability of circuits. Transistor aging could cause the gradual degradation of circuit performance and eventually lead to timing error. In this paper, a dynamic self-adaptive method is proposed to protect the circuit from the influence of transistor aging. This makes use of aging detection sensors and self-adaptive clock scaling cell. Aging sensors would automatically wake up the clock scaling cell to shift the clock phase of circuits when an error occurs. Then the timing error would be masked by a second sampling with the shifted clock. The method is simulated by Hspice using 65nm technology. The evaluation results show that this method is effective to error resilient with no impact on normal function of circuits, and it improves the MTTF by 1.16 times with 22.73% circuit overheads on average when the phase difference is 20% clock cycle.

I. INTRODUCTION

In nanometer technology, transistor scaling improves the performance of circuit; meanwhile, it also brings about some new serious challenges to the circuit reliability issues, one of which is the transistor aging.

Transistor aging would increase transistor threshed voltage, increase circuit delay and degrade circuit speed. Eventually, it would cause the timing error and circuit failure. Previous works show that transistor aging would lead to about 20% degradation of circuit performance in 10 years in the worst case [1-2].

In order to guarantee the reliability and lifetime of intergraded circuits, many researchers have focused on this problem. The main techniques in this area could be classified into two categories: one is the online aging prediction and detection [3-4], and the other is circuit aging protection [6-10].

In this paper, a dynamic self-adaptive method for error resilient application is proposed. The major contributions of it are:

(1) It analyzes the aging representation at the circuit level and concludes the basic process of circuit failure protection according to the aging features.
(2) Based on the online aging detection, it would re-sample logical signals on the data path to correct the errors. Then it automatically wakes up self-adaptive clock scaling cell to shift the global clock phase and maintain the regular operation of circuits.

The effectiveness of this method has been simulated by Hspice with 65nm PTM. And the evaluation results show that it could improve the MTTF (Mean-Time to Failure) by1.16 times with a low circuit overhead when the shifting phase is 20% of clock cycle.

The reminder of this paper is organized as follows. Section II analyzes the representation of aging at the circuit level and describes the process of aging failure protection. In section III, a specific self-adaptive failure protection method is presented. The simulation and evaluation results of this method are shown in section IV. Finally, conclusion and future work are offered in section V.

II. ANALYSIS OF AGING-INDUCED ERROR

In sequential circuits, there are about two parts of each clock cycle. One part is the delay of circuits, including contamination delay of combination logic, clock-to-q of flip-flops and so on. The other part is the timing margin. In the process of circuit aging, the primary feature on the circuit level is the increase of circuit delay and the degradation of timing margin. After the timing margin decreases to zero, it would leads to a timing violation in circuits that the transition of logic signal on the data path arrives later than the sampling edge of clock. So the memory elements would sample an error value and propagate it to a downstream stage.

Timing error would not appear in every sampling cycle. There are many dynamic variability effects impacting on circuit aging, such as workload. Some input vectors would aggravate circuit aging, while some others may partly recover aging. On the other hand, the logic signal on the data path before and after sampling may be the same value (i.e. it keeps low or high in two successive clock cycles). Under these conditions, aging-induced timing error may not occur. It is not necessary to schedule parameters of circuits permanently. Instead, a feasible way, making use of the dynamic sampling method to correct logic value while timing error occurs, to protect circuits from aging-induced failure is available. On the circuit level, the basic reason for aging-induced error is the sampling failure of memory element, not caused by the computing of combinational logic. Consequently, re-sampling by flip-flops after a proper interval could get the right value and transport the right output to downstream stage, as shown in Fig. 1.

In Fig. 1(a), the output of combinational logic is fresh, which could be stored in memory elements. While the output in Fig. 1(b) is a corrupted one, it could be re-sampled by a delayed clock as well. But the problem of simply using re-sampling to correct aging-induced error is that some potential timing faults may be caused. For example, it would shrink running time of next stage and then result in a new

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timing violation in circuits. So that, after each delayed re-sampling, the clock should be regulated synchronously to meet the timing constraint of circuits.

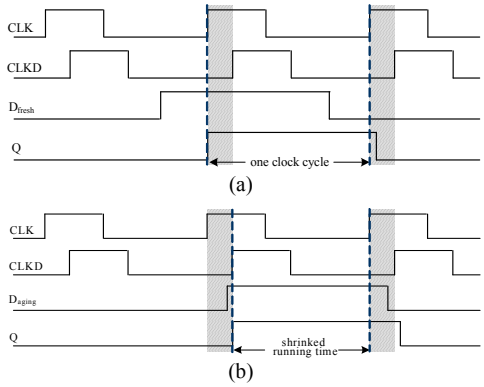

Fig. 1. Error correction by re-sampling: (a) fresh signal, (b)aging-induced error

III. A DYNAMIC SELF-ADAPTIVE METHOD TO CORRECT AGING-INDUCED ERROR

In this section, a dynamic self-adaptive method for resilient circuits is described. It uses redundant clock and dynamic clock phase self-scaling to correct aging-induced error and maintain the regular operating of circuits.

A. Structure of Dynamic Self-adaptive Correction Method

According to the analysis of aging feature on circuit level, the error correction structure for single flip-flop is designed as Fig. 2.

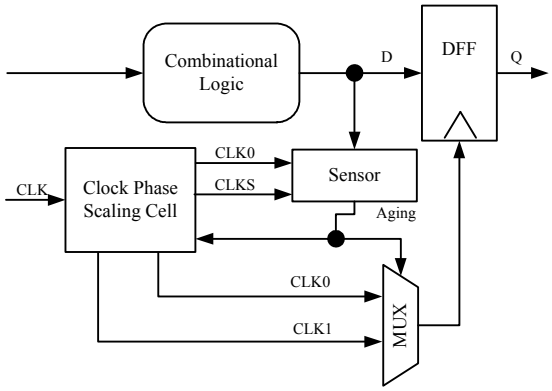

Fig. 2. Error correction structure for signal flip-flop

This signal correction unit consists of an aging detection sensor and a clock phase scaling cell (CPSC). The aging sensor is to online monitor signal on data path. There are many effective sensors in prior works, which provide a ground to our method. In this paper, we employ a classical sensor structure described in [3], which is used for circuit failure prediction. In order to detect aging-induced error, we have modified the relationship of control clocks to generate a Detection Window (DW) after clock sampling edge. Fig. 3 is the timing diagrams of the sensor application in this method. The output of aging sensor keeps the low level with no error appearing in circuits. While error occurs, it transforms to high one. The size of interval DW is determined by CLK0 and CLKS.

In the signal correction unit, CLK0 and CLK1 are two available clocks for flip-flop to sample signals. The method chooses one of them as the sampling clock according to the detection result of aging sensor. If no aging-induced error appears on data path, the former one is selected. When timing error occurs, the latter one would re-sample signal to correct corrupted value on data path.

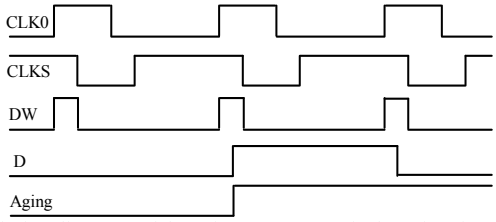

Fig. 3. Timing diagrams of detection sensor, DW is detection time window

All clocks of sensors and flip-flops are provided by the clock phase scaling cell (CPSC). The design of it is shown in Fig. 4. CPSC is composed of two parts. The first part is a compactor, used to compact the multi-detection for circuit aging. It includes a dynamic NOR gate and an aging signature counter. The dynamic NOR gate contributes to capturing errors on every data path. Since the clock phase of all flip-flops should be shifted when the timing error is corrected. The area overhead could be reduced largely with the help of dynamic NOR gate. The output of the dynamic NOR gate (which is CA) is high, while logic data is fresh. Once an error appears, it becomes low. And the aging signature counter computes the sum of errors and chooses the specific output clocks based on the count value. The second part of CPSC is to shift clock phase by delay elements. It transfers the standard clock (CLK) into n different ones. One of them is selected to be the control signal of circuits. The number of transferable clock is decided by the value of phase difference, which is equal to clock-cycle/pd, where pd is the size of phase difference. With n selectable clocks, it requires n-1 delay elements. The outputs of CPSC are three different clocks, CLK0, CLK1 and CLKS. CLK0 and CLK1 are used as the two sampling clocks of flip-flops. CLK0 and CLKS are the control clocks of sensors. Since the clock phase requires a unified regulation, just one CPSC is enough.

The specific architecture of correction method is described in Fig. 5.

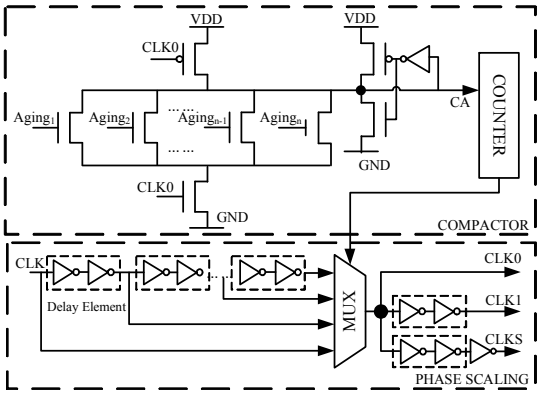

Fig. 4. Structure of clock phase scaling cell

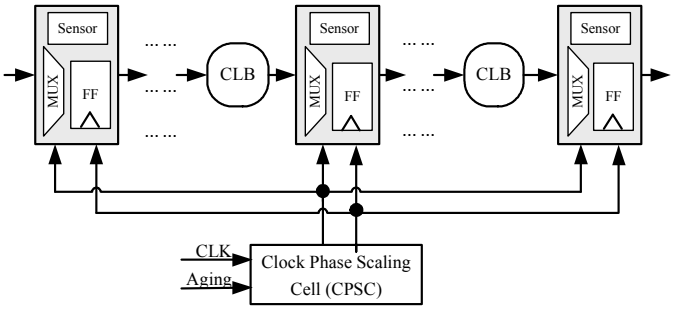

Fig. 5. Architecture of self-adaptive correcting method

B. Process Analysis of Dynamic Self-adaptive Correction Method

In this part, working process of proposed method is described. In the case of fresh circuits and aging circuits, the process would be introduced respectively.

a. Fresh Circuits

In the case of no timing error, there is not any event to modify the condition of control signal in circuits. Flip-flops would sample data path by the invariable clock. Fig. 6(a) shows the timing diagram of the working process of fresh circuits. In the diagram, the signal CLK is a standard clock, which is used to provide a reference to the variable control clock. It could be seen that without timing error, the aging detection sensor holds a low level output.

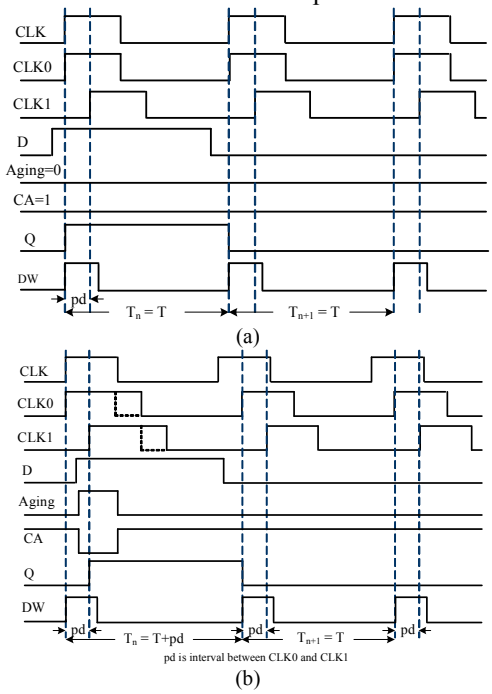

Fig. 6. Timing diagram of correction method: (a) in the case of fresh circuits, (b) in the case of aging circuits, pd is the size of phase difference

b. Aging Circuits

When an error appears, the correction mechanism invokes the redundant clock (CLK1) by the result of aging detection sensor to re-sample the data path. Just after data correction, it shifts the phases of all clocks to satisfy the timing constraint of circuits. Fig. 7(b) is the specific timing diagram of aging circuits. In the diagram, DW is the detection window. The sensor sends an alarm when transition of D is after the sampling edge of CLK0. As re-sampling by CLK1, the signal Aging falls down. Then, the aging signature counter is triggered by CA, which changes the output of MUX and shifts the phases of both CLK0 and CLK1. The phase of CLKS would be changed as well at the same time. The dashed frame in graph is the falling edge if no error occurring in circuits. The correction mechanism only extends the clock in current sampling cycle bythe size of one pd, which doesn't influence the global clock frequency in circuits.

IV. EXPERIMENTS

Experiments of dynamic self-adaptive correction method include two parts. The first part is the timing verification. The second part is the evaluation of MTTF and area overhead in benchmark.

A. Timing Verification

We have done the timing verification of proposed method by Hspice using 65nm PTM. The simulation waveform is shown in Fig. 7. The size of DW is equal to T/5, where T is the clock cycle. In the waveforms, CLK is the standard clock. CLK0 and CLK1 are two candidate clocks for sampling. In the clock cycle when aging-induced error appears, CLK1 is chosen to re-sample signal D on the data path and only the length of high level in current clock cycle is extended.

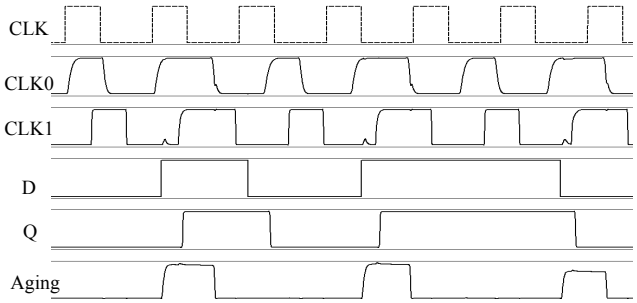

Fig. 7. Simulation waveform

B. MTTF Evaluation

According to the study in [6] and [10], the lifetime reliability of circuits is modelled with Weibull distribution. We make the same assumption as in [6] that all the data paths are independent of each other. The MTTF in lifetime is calculated by

$$MTTF = \int_0^X exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right] dt \qquad (1)$$

where α is a constant of Time-to-Failure and β is the shape factor [6][10]. In the proposed error correction method, the redundant re-sampling clock is to make a sampling guardband in circuits. So that, if the timing error occurs in the guarband, it could be corrected, i.e. with the same circuit failure rate, this method could extend the operation time of by length of $f(\sigma)$, where $\sigma=(pd/T)$. The value of MTTF is different with the variable pd. With the increasing size of pd, the value of MTTF is growing. But if pd is too large, it would raise the time of correction process and impact on the circuit working speed. We employ the growing rate of MTTF, noted as $MTTF_{INC}$, to be the evaluation metric, calculated by Equation 2, where $MTTF_{TS}$ is the value of MTTF with the protection of this method and $MTTF_{Regular}$ is MTTF without any protection.

$$MTTF_{INC} = \frac{MTTF_{TS} - MTTF_{Regular}}{MTTF_{Regular}} \quad (2)$$

Based on the characteristic of Weibull and statistic information from [6][10], the values of f(σ)with σ=1/20, 1/10, 1/5, 1/4 are as follows: f(1/20)=876， f(1/10)=8760， f(1/5)=43800， f(1/4)=87600. The parameters in Weibull distribution are calculated by:

$$\alpha_P = \alpha_N + f(\sigma) \quad (3)$$

$$\beta_P = \frac{1.38}{\ln(1+4380/(\gamma+f(\sigma)))} \quad (4)$$

where $\alpha_N \approx 39420$，$\beta_N \approx 11.72$，$\gamma=35040$. α_N, β_N are constants of Time-to-Failure and shape factors without protection. α_P, β_P are the value of them within this method. Under the condition of $X=10^9$, the $MTTF_{INC}$ is 2%, 23%, 116%, 232% at pd=T/20, T/10, T/5, T/4, respectively. Fig. 8 plots the computing results.

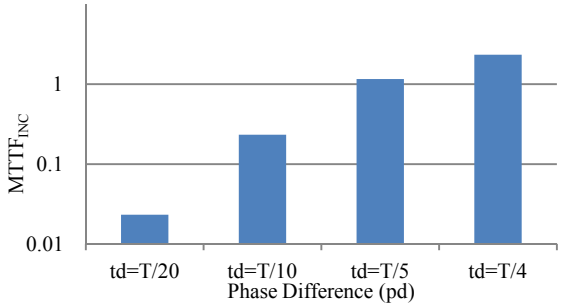

Fig. 8. $MTTF_{INC}$ at different pds

C. Area Overhead

The area of proposed correction method includes two parts, i.e. aging detection sensors and clock phase scaling cell (CPSC). The area of first part is related to the number of flip-flops in circuits. In the worst case, the number of sensors is equal to the number of flip-flops in circuits. In synchronous circuits, only one CPSC is required, since the clock is regulated synchronously during the protection. Area overhead is measured by $Area_{INC}$, by Equation 5, where $Area_{Regular}$ is the circuit area without protection and $Area_{TS}$ is area of circuit hardened by this correction method. We evaluate $Area_{INC}$ of ISCAS'89 benchmarks in the case of pd=T/5.

$$Area_{INC} = \frac{Area_{TS} - Area_{Regular}}{Area_{Regular}} \quad (5)$$

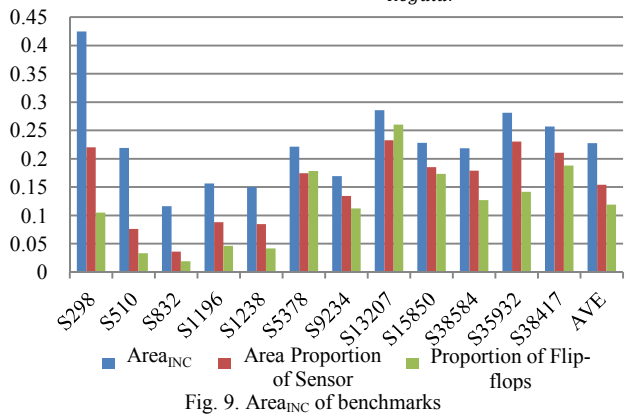

Fig. 9. $Area_{INC}$ of benchmarks

Fig. 9 describes the results of area overhead. The right bar is the proportion of flip-flops in all logic gates. The $Area_{INC}$ depends heavily on the number of flip-flops and area of sensors. In twelve benchmarks, the max area overhead is 42.47%. The average area overhead is 22.73%. With the lower area sensor, the $Area_{INC}$ would be much less.

V. CONCLUSIONS

This paper has proposed a dynamic self-adaptive correction method for error resilient application. This method employs a redundant clock to re-sample data path when aging-induced error appears. It regulates the clock phase after each error correction to keep consistency with timing constraint. This method could effectively mask aging-induced timing error and protect circuits from failure without influence on the circuit working frequency. Experiment results show that this method could improve MTTF of circuits up to 1.16 times with the 22.73% area overhead on average.

VI. ACKNOWLEDGMENTS

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