# Reliability Analysis for Integrated Circuit Amplifiers used in Neural Measurement Systems


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***Abstract*—NBTI and HCI are not only present in digital circuits but also in analog circuitry. Integrated circuit amplifiers as used in neural measurement systems (NMS) need to be resistive against degradation since these systems cannot be replaced easily. A topology driven design methodology to increase the reliability of amplifiers used for intracortical neural recording has been proposed in this work. This approach leads to a decrease in degradation for some system performances by a factor of three. It has been shown that the degradation of a circuit is highly dependent on the selected current mirror and biasing circuit.**



***Index Terms*—Analog circuits, negative bias temperature instability (NBTI), neural measurement system (NMS), circuit reliability.**


## I. Introduction

Intracortical recording has become a popular research field in the last two decades [1]. As general system aspects have been investigated, the design and study of suitable integrated circuit amplifiers has been found to be quite challenging [1]. Amplifiers used in neural measurement systems need to be low noise and low power. Full or partial system designs are already under investigation, [1], [2], [3]. Yet, reliability issues have not been considered for this type of amplifiers. Since the system is located inside the human body a replacement of the system should be avoided to minimize invasive actions to the patient. In order to achieve a long life time, not only the power consumption but also the drift in system characteristics has to be studied.

The need for reliable analog amplifiers in general has been addressed in several studies [4], [5]. Due to negative bias temperature instability and channel hot carrier influences PMOS and NMOS transistor types degrade over time, specifically the threshold voltage will alter. This leads to a drift in system performance characteristics such as gain, phase margin or common mode rejection ratio. There have also been studies on how to reduce the effects of degradation by optimizing given circuits [6]. The Worst-Case distance is used as a measure for reliable circuits. Intensive work has been done in optimizing this distance, revealing circuits with long life times and good degradation behaviors. However, this design methodology addresses reliability as an optimization factor. This leads to a design flow where reliability effects and reliability aware design steps are pushed towards the end. As in all optimizations, some system characteristics might not be achievable anymore, if such issues are taken care of at the very end. An analog designer should already be aware of degradation during the early design phase to achieve the best possible characteristics.

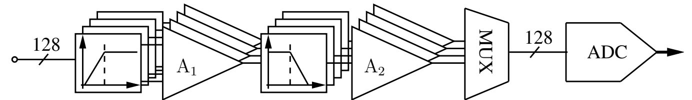


Fig. 1. Basic diagram for a neural measurement system with 128 inputs.

Early work has been done on using dedicated structures or measures to decrease degradation in amplifiers. However, neural amplifiers underly certain design restrictions such that not all HCI and NBTI counteractions are applicable. In [7] a method to overcome degradation in power down modes is introduced. By adding switch transistors to the gates of the input differential pair an improved degradation behavior was achieved. However, this approach is not suitable for amplifiers in neural recording system, since those transistors will decrease the input impedance and increase the input referred noise of the amplifier. Another way to reduce degradation is to use an NMOS differential input pair. NMOS transistors do not suffer from NBTI, but due to the worse noise behavior compared to the PMOS type transistors, an NMOS differential input pair is not an option for neural amplifiers.

## II. Neural Measurement Systems

Typically there are two different types of neural signals which are of interest and need to be detected: neural spikes and local field potentials (LFP). Neural spikes are signals from a single dedicated neuron. The amplitude of a spike varies from $50$ to $500\,\mu\text{V}$ and has a frequency range of approximately $100\,\text{Hz}$ to $10\,\text{kHz}$. LFPs are recorded signals of a large number of contributing neurons which represent the activity of a specific observed area. Their amplitude reaches up to $5\,\text{mV}$ and has a bandwidth of $1\,\text{Hz}$ to $250\,\text{Hz}$. Both signals are imposed by a varying near DC signal. It is therefore important to have a high pass filter with a cut off frequency well below $1\,\text{Hz}$.

A neural measurement system (NMS) is able to record these signals and to convert them into a bit stream. The intracortical measurement will be done by a multi-electrode array. A basic topology of an NMS with 128 input signals for an electrode


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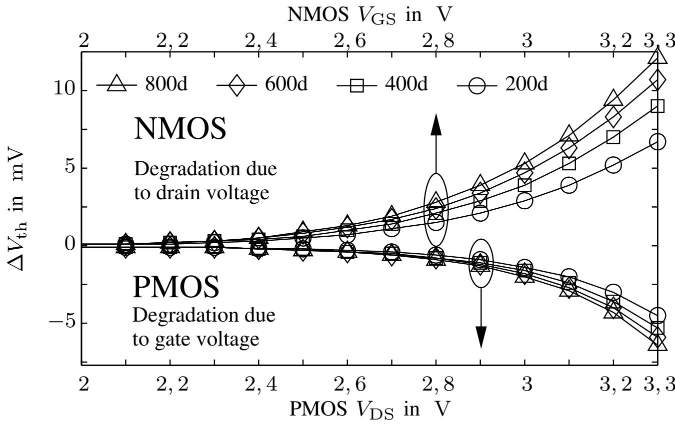


Fig. 2. Degradation of threshold voltage for an NMOS and a PMOS type transistor for a simulated stress time from 200 to 800 days.

array of the same size is shown in Fig. 1. The high and low pass filters are designed using a low noise amplifier with gain $\mathrm{A}_1$ and an output stage with gain $\mathrm{A}_2$. For each electrode there has to exist a dedicated filter path, each containing a low noise amplifier and an output stage. As every analog circuit, also an NMS suffers from degradation. The low noise amplifier is the direct interconnect between the excited neural signal and the further filter path which leads to the A/D converter. To assure an unbiased amplification that does not change over life time, it is necessary to understand the impact of degradation.

## III. NBTI and HCI Circuit Degradation

NBTI and HCI alter the device's threshold voltage over time. The negative bias temperature instability occurs in PMOS devices [4], [8] whereas the hot carrier injection occurs in NMOS devices [9]. If a negative bias voltage is applied at a PMOS, interface traps are generated at the gate/channel interface. This will lead to an increase in the threshold voltage $V_{\mathrm{th,p}}$. HCI generates interface traps near the drain side of N-channels and leads to a change in the threshold voltage $V_{\mathrm{th,n}}$. Both mechanisms will not only degrade the specific transistor behavior. As it will be shown for a given amplifier the degradation of a single transistor can have a huge influence on performances like CMRR, PSRR or the phase margin.

Both mechanisms can be described by the general *reaction diffusion model* [10]. In the *reaction* phase, due to the high electric field at the channel-gate interface some of the Si-H or Si-O bonds are broken. This will store positive charged ions ($H^+$, $O^{2+}$) in the $SiO_2$-gate introducing an interface charge and therefore an increase in $V_{\mathrm{th}}$. For NBTI this is caused by positive holes, for HCI hot electrons are causing the change in threshold voltage. During *diffusion* the generated interface traps start to diffuse deeper into the gate [11].

Design analysis is performed using an industrial $150\,\mathrm{nm}$ process. The fresh netlist will undergo degradation excited by a transient simulation. The Cadence RelXpert reliability simulator calculates the degradation for each transistor based on the transient excitation stress by using an proprietary AgeMOS model.

TABLE I
Dimensions for all NMOS and PMOS transistors.

| Device | W | L | Units | Device | W | L | Units |
|---|---|---|---|---|---|---|---|
| **Default Values** | | | | **Folded Cascode OTA** | | | |
| NMOS | 5 | 1 | µm | MC | 12.5 | 5 | µm |
| PMOS | 12.5 | 1 | µm | MF | 5 | 5 | µm |
| $I_{\mathrm{bias}}$ | 12 | | µA | M9, M10 | 50 | 1 | µm |
| **Mos Only Reference** | | | | **Beta Matching Reference** | | | |
| $\mathrm{M_{b,n}}$ | 3 | 49 | µm | S1 | 10 | 60 | µm |
| $\mathrm{M_{b,p}}$ | 5 | 23 | µm | S3 | 5 | 0.5 | µm |
| | | | | R | 12k | | Ω |
| **Cascode as Source** | | | | **Cascode as Sink** | | | |
| M3 | 5 | 4 | µm | M3 | 12.5 | 4 | µm |

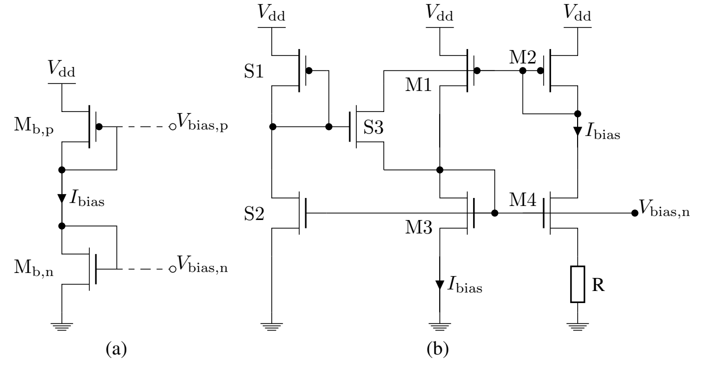


Fig. 3. Two types of biasing circuits. (a) Mos Only Reference (MOR). (b) Beta Matching Reference (BMR) with start-up circuit S1 – S3.

The degradation for the threshold voltage for an NMOS and PMOS type transistor is depicted in Fig. 2. For this analysis the NMOS has a width of $W = 5$ µm and the PMOS a width of $W = 12.5$ µm. Both types share a length of $L = 1$ µm. In order to excite a degradation, a variant drain-source (NMOS) and a variant gate-source voltage (PMOS) are applied while keeping the other voltages constant ($V_{\mathrm{DS}} = 0.5\,\mathrm{V}$ and $V_{\mathrm{GS}} = 1\,\mathrm{V}$ for NMOS and PMOS respectively). Note that NBTI manifests itself as a change in PMOS $V_{\mathrm{th,p}}$ and is dependent on $V_{\mathrm{GS}}$. HCI degradation increases the value for NMOS $V_{\mathrm{th,n}}$ and is dependent on $V_{\mathrm{DS}}$.

## IV. Reliable Current Mirror Topologies

In order to investigate the effects of NBTI and HCI on complex circuits, a deeper look has to be taken at simple structures first. Current Mirrors are one of the most used circuits in analog circuit design and are very important for various system performances. A current mirror consists at minimum of two parts: a circuit for biasing and the actual mirroring circuit. For biasing there exist numerous circuits, each with specific advantages and disadvantages. Two Biasing circuits have been chosen for this analysis. Figure 3(a) shows a MOS only reference (MOR) bias circuit. The derived voltages $V_{\mathrm{bias,n}}$ and $V_{\mathrm{bias,p}}$ will be used to bias an NMOS or PMOS to drive the current $I_{\mathrm{bias}}$ or a chosen multiple of it. This circuit must be sized for either $V_{\mathrm{bias,n}}$ or $V_{\mathrm{bias,p}}$. For a given $I_{\mathrm{bias}}$ the Beta Matching Reference (BMR) in Figure 3(b) will generate

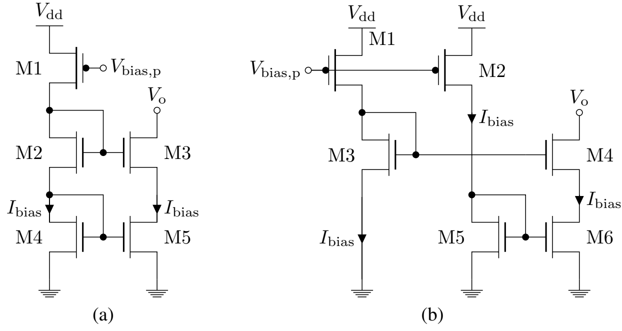


Fig. 4. Different mirroring circuits. (a) Cascode structure as sink. (b) Wide swing structure as sink.

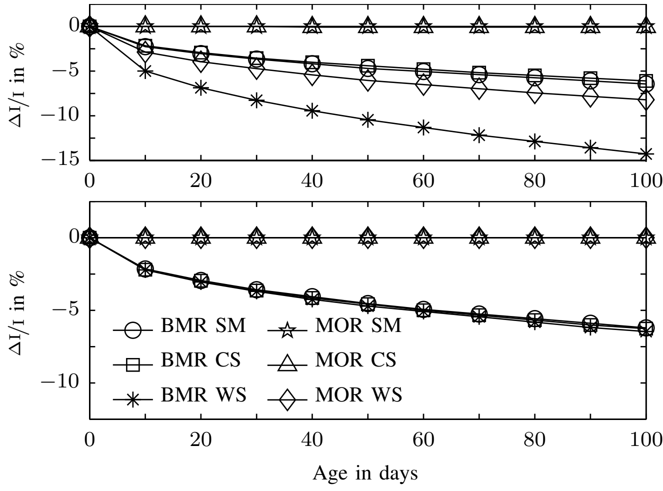


Fig. 5. Deviation of sink currents (top) and source currents (bottom) over time in steps of 100 days. SM: Single MOS transistor; CS: Cascode structure; WS: Wide Swing structure.

the exact same reference voltages as the MOR, but has a higher suppression of changes in $V_{\mathrm{dd}}$.

The mirroring part of a current mirrors is biased by either a MOR or BMR and can function as a sink or a source. For a single rail (single supply voltage) configuration a current sink drives a current from a given node to ground and is usually constructed by NMOS transistors. A source drives a current from a given node to $V_{\mathrm{dd}}$ and is usually made of PMOS transistors. Three different mirroring structures have been investigated: single transistors, cascode mirrors and wide swing mirrors.

A cascode mirror structure in sink configuration is shown in Fig. 4(a), the corresponding wide swing current sink is shown in Fig. 4(b). The wide swing structure has approximately the same output resistance as the cascode structure but a lower minimum output voltage to keep both transistors M4 and M6 in saturation. All structures have been designed as sinks and sources. All NMOS and PMOS devices share the same dimensions stated in Table I. The circuits are designed to drive a current $I_{\mathrm{bias}}$ of 12 µA at a supply voltage of $V_{\mathrm{dd}} = 3.3$ V. For the MOR, the dimensions for $\mathrm{M}_{\mathrm{bias,n}}$ and $\mathrm{M}_{\mathrm{bias,p}}$ are given for generating $V_{\mathrm{bias,p}}$ and $V_{\mathrm{bias,n}}$ respectively.

By combining two different bias circuits and six different mirroring circuits (sinks and sources), a total of 12 circuits can be analyzed to their degradation over time. Figure 5 shows the deviation of the output current for a degradation of 100 days full time operation. The node voltage $V_{\mathrm{o}}$ was set to $V_{\mathrm{o}} = 1$ V for sinks and $V_{\mathrm{o}} = 2.3$ V ($V_{\mathrm{dd}} - 1$ V) for sources. The deviation shown in Fig. 5 ranges from 0 to approximately 15 %. All current sinks biased by the BMR show deviation. The same structures biased by the MOR tend to be more stable. The MOR biased single MOS transistor and cascode structure do not show any deviation. The deviation of the source currents reaches approximately only 50 % of the sink's deviation. This can be explained by the fact that sinks suffer mostly from HCI which is dependent on the drain source voltage. As seen in Fig. 2, comparing the influence of $V_{\mathrm{DS}}$ and $V_{\mathrm{GS}}$ at the same value, $V_{\mathrm{th,n}}$ degradation is worse than the degradation of $V_{\mathrm{th,p}}$ by a factor of 2, which corresponds to the results from Fig. 5. As for the current sources the applied gate voltages are lower than the drain voltages for the sinks, the effect of NBTI is less than HCI.

The different degradation behavior of the current mirrors and biasing circuits can be used to methodically design reliable amplifier structures. By interchanging current mirror topologies the degradation of whole circuits can be drastically reduced. Although neural amplifiers obey specific design rules, e.g. using PMOS input transistors for an improved noise characteristic, it can be shown that the proposed method is suitable for that class of amplifiers.

TABLE II
FRESH SYSTEM CHARACTERISTICS.

| **Specification** | **Unit** | **CS BMR** | **CS MOR** | **SI BMR** | **SI MOR** |
|---|---|---|---|---|---|
| Phase Margin | ° | 88.6 | 88.7 | 88.6 | 88.6 |
| Slew Rate Rise | V/ µs | 1.68 | 1.72 | 1.68 | 1.72 |
| Slew Rate Fall | V/ µs | 2.32 | 2.38 | 2.46 | 2.53 |
| DC Gain | dB | 65.4 | 65.5 | 65.3 | 65.4 |
| GBW | MHz | 3.77 | 3.84 | 3.88 | 3.94 |
| PSRR | dB | 83.9 | 70.3 | 84.3 | 73.1 |
| CMRR | dB | 85.5 | 79.3 | 89.2 | 81.2 |

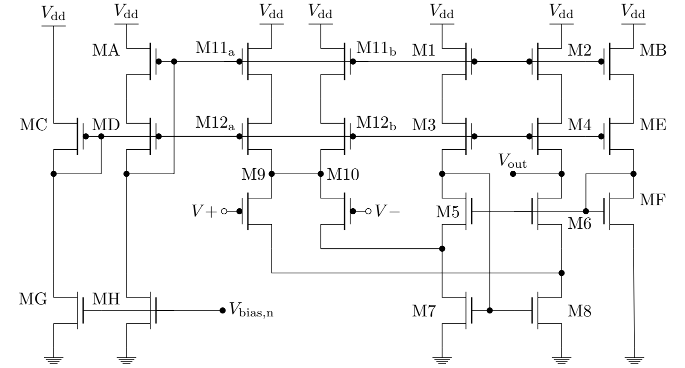


Fig. 6. Schematic of Folded Cascode OTA.

## V. Degradation of a Folded OTA Structure

Figure 6 shows the schematic of a folded cascode amplifier used for neural measurement systems. If not stated differently,

TABLE III
DEGRADED SYSTEM CHARACTERISTICS

| Specifications | 200d | 400d | 600d | 800d | 1000d |
|---|---|---|---|---|---|
| **Wide Swing biased by BMR** | | | | | |
| PM | 0.81 | 1.25 | 1.47 | 1.61 | 1.86 |
| Slew Rate Rise | -19.55 | -26.74 | -31.97 | -36.19 | -39.81 |
| Slew Rate Fall | -58.75 | -75.02 | -84.48 | -90.89 | -95.38 |
| DC Gain | 0.38 | -2.03 | -5.37 | -9.93 | -16.81 |
| GBW | -41.14 | -58.75 | -71.63 | -81.76 | -90.18 |
| PSRR | -46.32 | -52.22 | -57.13 | -62.26 | -68.78 |
| CMRR | 5.83 | 9.90 | 12.69 | 14.85 | 15.13 |
| **Wide Swing biased by MOR** | | | | | |
| PM | 0.72 | 1.14 | 1.31 | 1.40 | 1.57 |
| Slew Rate Rise | -11.38 | -15.56 | -18.52 | -21.02 | -23.05 |
| Slew Rate Fall | -52.10 | -67.49 | -76.90 | -83.56 | -88.57 |
| DC Gain | 1.18 | -0.32 | -2.32 | -4.78 | -7.85 |
| GBW | -33.24 | -50.18 | -60.90 | -69.92 | -78.18 |
| PSRR | -51.05 | -57.74 | -62.78 | -67.36 | -72.01 |
| CMRR | 2.81 | 5.05 | 6.83 | 8.27 | 7.68 |
| **Single PMOS biased by BMR** | | | | | |
| PM | 0.89 | 1.24 | 1.41 | 1.61 | 1.84 |
| Slew Rate Rise | -19.55 | -26.74 | -31.97 | -36.19 | -39.81 |
| Slew Rate Fall | -55.55 | -70.57 | -79.67 | -86.00 | -90.55 |
| DC Gain | 0.64 | -1.52 | -4.42 | -8.19 | -13.43 |
| GBW | -40.62 | -57.50 | -69.99 | -79.57 | -87.14 |
| PSRR | -50.07 | -55.49 | -59.92 | -64.35 | -69.51 |
| CMRR | 3.83 | 6.71 | 8.91 | 10.58 | 10.32 |
| **Single PMOS biased by MOR** | | | | | |
| PM | 0.77 | 1.14 | 1.30 | 1.40 | 1.57 |
| Slew Rate Rise | -11.27 | -15.46 | -18.48 | -20.98 | -23.07 |
| Slew Rate Fall | -48.97 | -62.94 | -71.71 | -78.04 | -82.95 |
| DC Gain | 1.41 | 0.09 | -1.65 | -3.76 | -6.36 |
| GBW | -33.33 | -49.96 | -59.05 | -68.39 | -75.58 |
| PSRR | -53.86 | -59.86 | -64.36 | -68.35 | -72.35 |
| CMRR | 2.06 | 3.77 | 5.17 | 6.24 | 5.15 |

the dimensions of the transistors are given in Tab. I. The OTA is built by $\mathrm{M1}$ to $\mathrm{M12}$. $\mathrm{MA}$ to $\mathrm{MH}$ generate bias voltages for the OTA. The PMOS differential input pair is driven by the current source constructed by $\mathrm{M11_a}$, $\mathrm{M11_b}$, $\mathrm{M12_a}$ and $\mathrm{M12_b}$. $V_{\mathrm{bias,n}}$ is generated by a MOS only or a beta matching reference circuit from Figure 3.

The transistors $\mathrm{MA}$, $\mathrm{MC}$, $\mathrm{MD}$, $\mathrm{MG}$ and $\mathrm{MH}$ will serve in combination with the 4 cascode structures $\mathrm{M11\text{-}M12}$, $\mathrm{M1\text{-}M3}$, $\mathrm{M2\text{-}M4}$ and $\mathrm{MB\text{-}ME}$ as an improved wide swing current mirror (note that compared to Fig. 4(b) $\mathrm{MD}$ has been included for a better bias voltage matching). By removing $\mathrm{M12_a}$ and $\mathrm{M12_b}$ the PMOS differential input pair is driven by a single MOS current source instead of a wide swing current source. Analysis of the amplifier characteristics has been done with two different current mirrors sourcing the differential input pair and also two biasing circuits (BMR, MOR) generating $V_{\mathrm{bias,n}}$. Fresh characteristics are shown in Table II. The circuit is degraded for $1000$ days in a step size of $200$ days. Table III shows the degraded system characteristics. The results of the analysis show that the characteristics degrade dependent on the used bias circuit and current source for the differential input pair. The degradation of the DC Gain after $1000$ days has its lowest value of $-6.36\ \%$ for the single PMOS current source and MOR biasing. The highest degradation of $-16.81\ \%$ can be found for the cascode current source and BMR biasing. In case of the CMRR and Slew Rate the degradation can be reduced by almost a factor of two to three comparing the single PMOS transistor biased by a MOR and the wide swing current mirror biased by a BMR. However, for the given example the PSRR degradation increases, showing that a reduction in degradation for all system characteristics cannot be achieved at the same time.

## VI. CONCLUSION

Degradation aware design has already become a daily work pattern for analog designers. There exist different approaches on how to increase the reliability. In contrast to leaving this aspect to the courtesy of optimizers, the described method is driven by the designer itself. We think that our approach of a topology driven design flow will serve as a very good starting point for reliable designs. The degradation of a neural folded cascode OTA has been greatly reduced by choosing appropriate current mirrors and biasing circuits.

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