

technical programme topic chairs

D1 System Specifications, Models, and Methodologies

Christian Haubelt
University of Rostock, DE

Dominique Borrione
TIMA Labs, FR

D2 System Design, Synthesis and Optimization

Jan Madsen
Technical University of Denmark, DK

Luciano Lavagno
Politecnico di Torino, IT

D3 Simulation and Validation

Franco Fummi
Universita' di Verona, IT

Mark Zwolinski
University of Southampton, UK

D4 Design of Low Power Systems

Tudor Murgan
Intel, DE

Domenik Helms
OFFIS, DE

D5 Power Estimation and Optimization

Massimo Poncino
Politecnico di Torino, IT

Jian-Jia Chen
KIT, DE

D6 Emerging Technologies, Systems and Applications

Sanjukta Bhanja
University of South Florida, US

Siddharth Garg
University of Waterloo, CA

D7 Formal Methods and Verification

Gianpiero Cabodi
Politecnico di Torino, IT

Jason Baumgartner
IBM Corporation, US

D8 Networks-on-Chip

Federico Angiolini
iNoCs, CH

Fabien Clermidy
CEA-LETI, FR

D9 Architectural and Micro-Architectural Design

Laura Pozzi
University of Lugano, CH

Tulika Mitra
National University of Singapore, SG

D10 Architectural and High-Level Synthesis

Philippe Coussy
Universite de Bretagne Sud / Lab-STICC, FR

Nikil Dutt
University of California, Irvine, US

D11 Reconfigurable Computing

Fadi Kurdahi
University of California at Irvine, US

Marco Platzner
University of Paderborn, DE

D12 Logic Synthesis and Timing Analysis

Jordi Cortadella
Universitat Politecnica de Catalunya, ES

José Monteiro
INESC-ID / IST, TU Lisbon, PT

D13 Physical Design and Verification

Ralph Otten
TU Eindhoven, NL

Azadeh Davoodi
University of Wisconsin - Madison, US

D14 Analog and Mixed-Signal Systems and Circuits

Catherine Dehollain
EPFL, CH

Günhan Dündar
Boğaziçi University, TR

D15 Modeling and Design for Signal and Power Integrity

Stefano Grivet-Talocia
Politecnico di Torino, IT

Jounggho Kim
KAIST, KR

A1 Green Computing Systems

Tajana Simunic Rosing
UCSD, US

AYSE COSKUN
Boston University, US

A2 Communication, Consumer and Multimedia Systems

Frank Kienle
Technical University of Kaiserslautern, DE

Theocharis Theocharides
University of Cyprus, CY

A3 Transportation, Management and Energy Generation Systems

Davide Brunelli
University of Trento, IT

Bart Vermeulen
NXP Semiconductors, NL

A4 Medical and Healthcare Systems

Srinivasan Murali
IMEC, BE

Martino Ruggiero
University of Bologna, IT

A5 Secure Systems

Patrick Schaumont
Virginia Tech, US

Guido Bertoni
STMicroelectronics, IT

A6 Reliable and Reconfigurable Systems

Jose Ayala
Complutense University of Madrid, ES

Marco D. Santambrogio
Politecnico di Milano, IT

A7 Industrial Experiences Brief Papers

Ahmed Jerraya
CEA Leti, FR

Roberto Zafalon
STMicroelectronics, IT

T1 Test for Defects, Variability, and Reliability

Bram Kruseman
NXP Semiconductors, NL

Jaume Segura
Universitat de les Illes Balears, ES

T2 Test Generation, Simulation, and Diagnosis

Grzegorz Mrugalski
Mentor Graphics Poland, PL

Bernd Becker
University of Freiburg, DE

T3 Test for Mixed-Signal, Analog, RF, MEMS

Abhijit Chatterjee
Georgia Tech, US

Haralampos Stratigopoulos
TIMA Laboratory, FR

T4 Test Access, Design-for-Test, Test Compression, System Test

Sybille Hellebrand
University of Paderborn, DE

Rohit Kapur
Synopsys, US

T5 On-Line Testing and Fault Tolerance

Cecilia Metra
University of Bologna, IT

Lorena Anghel
TIMA, FR

E1 Real-time, Networked, and Dependable Systems

Giuseppe Lipari
ENS-Cachan, FR

Stefan M. Petters
CISTER-ISEP, IPP, PT

E2 Compilers and Software Synthesis for Embedded Systems

Bjoern Franke
University of Edinburgh, UK

Heiko Falk
Ulm University, DE

E3 Model-Based Design and Verification for Embedded Systems

Wang Yi
Uppsala University, SE

Saddek Bensalem
Université Joseph Fourier, FR

E4 Embedded Software Architectures

Gabriela Nicolescu
Ecole Polytechnique de Montreal, CA

Oliver Bringmann
FZI / University of Tuebingen, DE

E5 Cyber-Physical Systems

Anuradha Annaswamy
MIT, US

Anton Cervin
Lund University, SE