Systematic Design of Nanomagnet Logic Circuits

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***Abstract*—Nanomagnet Logic (NML) is an emerging device architecture that performs logic operations through fringing field interactions between nano-scale magnets. The design space for NML circuits is large and so far there exists no systematic approach for determining the parameter values (e.g., device-to-device spacings, clocking field strength etc.) to generate a predictable design solution. This paper presents a formal methodology for designing NML circuits that marshals the design parameters to generate a layout that is guaranteed to evolve correctly in time at $0K$. The approach is further augmented to identify functional design targets when considering thermal noise associated with higher temperatures. The approach is applied to identify layouts for a 2-input AND gate, a "corner turn," and a 3-input majority gate. Layouts are verified through simulations both at $0K$ and room temperature ($300K$).**

I. Introduction

It is well known that CMOS scaling trends are now accompanied by less desirable byproducts such as increased energy dissipation. Devices where state is represented without the use of electric charge could alleviate undesirable side effects of CMOS scaling – especially when considering low power application spaces. Nanomagnet Logic (NML) is one such technology. Binary information is stored and processed with lithographically-defined magnetic islands. Boolean logic operations and signal propagation are accomplished via fringing field interactions between magnets [1], [2]. [3] suggests that NML could best CMOS hardware equivalents at iso-performance even after accounting for clock overhead.

Still, a systematic method for designing NML circuits – for experimental *and* simulation targets – does not exist, and nearly all design efforts have been performed in a "trial and error" fashion [2], [4]. While the structure of a given NML ensemble is often obvious – e.g., for fanout or for a majority gate – the design parameter space is large. Device-to-device spacing, magnet size, aspect ratio, material, crystal structure, thickness, and shape can all impact whether or not a magnet ensemble evolves to a *logically correct* ground state. Finding a functionally correct layout is non-trivial. Any magnet in an ensemble could influence any other magnet through unwanted fringing field interactions. Thermal noise can also impact switching order and produce undesirable states.

Here we present a systematic design method for NML circuits that marshals all of the aforementioned design parameters to generate a layout that will function correctly during *initial* physical-level simulations. Our approach identifies design parameters that lead to safe operating windows. The end result is a layout that can be generated via an automated process where devices evolve in a predictable, and logically correct manner.

The main contributions of this paper are as follows: **(1)** We have introduced an analysis technique to determine the necessary conditions for a given magnet to remain in or transition to a desired magnetization state. **(2)** Using the aforementioned analysis, we have developed a methodology for generating NML layouts that are guaranteed to function correctly[1]. By supplying a target structure and desired ground state, our methodology can be employed to determine device sizes, spacings, etc. in an automated fashion. **(3)** We have enhanced the design methodology to augment initial layouts (targeted for $0K$ simulations) such that logically correct ground states could be achieved when considering stochastic effects associated with higher temperatures.

Our methodology has been used to identify layouts for 2-input AND gates, 3-input majority gates, and "corner turns" comprised of anti-ferromagnetic lines that transition to ferromagnetic lines. The methodology and representative results are presented in the rest of the paper.

II. Background

Here, we discuss the basic principles of NML, clock functionality, and the simulation setup used throughout this work.

A. Circuit Constructs

Magnetization states of single-domain magnets can represent, move and process binary information. A wire (Fig. 1a) can be formed from a line of magnets that are anti-ferromagnetically (AF) coupled with each other. Ferromagnetic interconnect is also possible [5]. A functionally complete logic set can be realized with combinations of majority voting gates. By setting one input to a logic 0 or 1, the gate can execute an AND/OR (or NAND/NOR) function [1]. This "parts library" has been expanded to include programmable majority gates, fanout, and non-majority AND/OR logic [6]. All have been experimentally demonstrated at room temperature.

B. Clock Functionality

Externally supplied switching energy is needed to re-evaluate a magnet ensemble (e.g., Fig. 1a) with new inputs (Fig. 1b, c). For "on-chip" clocking, [7] proposed using hard axis directed magnetic fields from current driven wires. These structures have been (i) fabricated [8], (ii) used to switch the state of individual magnetic islands [8], and (iii) used to re-evaluate line and gate structures with new inputs [9].

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[1]We do not claim to identify an optimal layout; we identify a working target, without trial and error simulations, that can be optimized further.

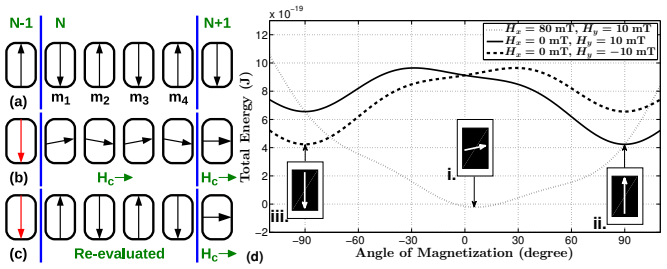


Fig. 1. (a) AF-line moves information; (b) an AF-line has a new input, and an external clocking field is used to facilitate re-evaluation of the line; (c) as the field is removed, devices relax along their easy axes; (d) Energy landscape of a representative magnet when subjected to different field combinations.

Ensembles of magnets could be grouped in clocking zones. Fig. 1b illustrates the effects of the clocking field: magnets of clocking zone N and N+1 are put into a metastable state (i.e., along the hard/short/x-axis) against the preferred shape anisotropy. As magnets always tend to be magnetized along a direction such that the *total energy* is minimized, if a driving neighbor provides a y-directed field, the driven magnet's magnetization rotates toward a preferred easy (long/y) axis (Fig. 1d-i). When the clock is removed, magnet m_1 will relax to a new, low energy ground state (Fig. 1d-ii, iii). Succeeding magnets m_2, m_3, and m_4 should then relax in order.

C. Simulation Setup

Micro-magnetic simulation is a valuable tool for predicting the behavior of an NML ensemble. In this work, we use the Objected Oriented Micro-Magnetic Framework (OOMMF) [10] developed by NIST as the simulation tool. All simulations assume magnets made from Cobalt (Co) with a magnetocrystalline biaxial anisotropy constant $K_1 = 40\ KJ/m^3$, which further promotes hard axis stability during switching [4]. Per [4], we use a saturation magnetization of $10^6\ A/m$ and an exchange stiffness constant of $1.3 \times 10^{-11}\ J/m$. We assume a damping coefficient of 0.05. A rounded rectangular shape with a $39 \times 63 \times 5\ nm^3$ footprint (a multiple of the $3 \times 3 \times 5\ nm^3$ simulation mesh) is used for magnets in horizontal and vertical wires. Helper magnets with easy axes parallel to the direction of the applied field can provide static, hard-axis biasing fields over a target magnet when needed. Our design methodology is also employed to size and place these helper structures.

III. Overview of Phase Diagram Based Design

In this section we introduce a fundamental concept of our design methodology – the *phase diagram*. We explain how a phase diagram can be used to determine the required external fields over a given magnet to ensure that it (i) switches to a logically correct, easy axis magnetization state at an appropriate time, and (ii) otherwise remains in a metastable state. We end the section by presenting the overall approach.

A. Phase Diagrams

In an ensemble, the external magnetic field that a magnet experiences varies over the course of a computation as neighboring magnets switch and/or the magnitude of the clock field changes. Thus, the energy profile of a magnet also evolves

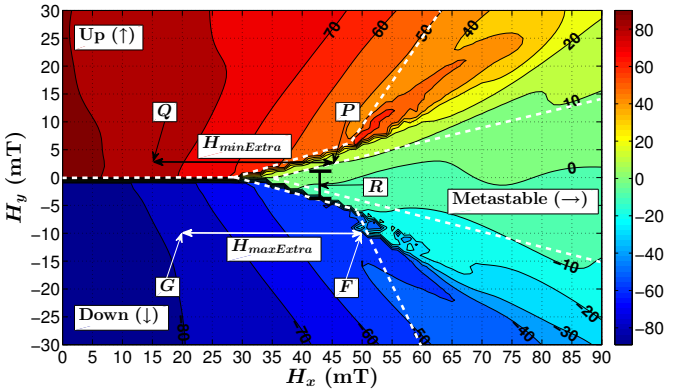


Fig. 2. Phase diagram of a $39 \times 63 \times 5\ nm^3$ Co magnet with biaxial anisotropy constant $K_1 = 40\ kJ/m^3$ depicting the angle of magnetization when subjected to different field combinations.

over time, and an energy minimum can shift to different positions (Fig. 1d) causing the magnetization vector to settle at different angles. To correctly predict the magnetization state of a magnet over time, it is important to capture how it reacts under the influence of *any* external field. We introduce *phase diagrams* (see a representative example in Fig. 2) to achieve this goal. Each point in a phase diagram represents the angle of magnetization at which a given magnet settles when subjected to a pair of x-directed (H_x) and y-directed (H_y) fields. In Fig. 2, one can clearly distinguish three mutually exclusive regions (defined by overlaid dashed lines) on the phase diagram corresponding to three magnetic states: 'Up' (↑), 'Down' (↓) and 'Metastable' (→). We assume a magnet is in a ↑ or ↓ state if its angle of magnetization is greater than $50°$ or less than $-50°$, respectively. If the angle of magnetization is between $-10°$ and $10°$, we consider the magnet to be in a metastable state. (The two remaining areas do not precisely represent any stable magnetization state, and hence we choose to avoid those regions.)

For a magnet with given material properties and dimensions, a single corresponding phase diagram can be (i) generated via any micro-magnetic simulator, and (ii) continuously re-used when designing a circuit (even if device-to-device spacing changes). We used OOMMF to generate a phase diagram by subjecting a single magnet to varying H_x and H_y fields in the range that a device may experience from its neighbor's fringing fields and/or the clock. When generating a phase diagram, the device is initially hard axis biased – an intermediate state associated with clocking (see Fig. 1b). It is then subjected to different field contributions and allowed to relax for a sufficient period of time such that the magnetization vector reaches a steady state. (Here, 1.5 ns was sufficient.) Final angles of magnetiation are then plotted for each H_x and H_y pair.

B. Conditions for Hard axis Stability

For a magnet ensemble to evolve to a logically correct ground state, a given device must be able to: (i) remain in a metastable state such that it does not switch prematurely, and (ii) deterministically switch to a logically correct, easy axis magnetization state based on fringing fields from an appropriate neighbor. We first define the criteria for (i), and

discuss those for (ii) in the next subsection.

Let the input space $I = \{I_0, I_1, ..., I_{2^n-1}\}$ represent all 2^n possible input combinations for an n-input gate or circuit structure. For a given magnet M and given input I_j, let t_{sw}^M be the time when M should begin switching to a logically correct state such that correct ensemble switching order is preserved. Also, let $H_x(I_j, t)$ and $H_y(I_j, t)$ be the x- and y-components of the total magnetic field experienced by M for input I_j at an arbitrary time $t < t_{sw}^M$.

Given the values of $H_x(I_j, t)$ and $H_y(I_j, t)$, we must determine whether or not a magnet will remain metastable. We employ the phase diagram to find the minimum value of H_x that is required to keep the magnet metastable. For example, per point Q in Fig. 2, if $H_x(I_j, t) = 15\ mT$ and $H_y(I_j, t) = 2.5\ mT$ then the x-directed field should be at least $45\ mT$ (per point P) to ensure that the magnet remains in the metastable region of the phase diagram. We refer to this minimum required x-directed field as $H_{min}(I_j, t)$. If the existing field $H_x(I_j, t)$ does not put the magnet in a metastable state (point Q), some additional x-directed field (from the clock and/or a helper cell) must be provided. This minimum required additional x-directed field can be expressed as:

$$H_{minExtra}(I_j, t) = \begin{cases} 0 & \text{if } H_x(I_j, t) \geq H_{min}(I_j, t) \\ H_{min}(I_j, t) - H_x(I_j, t) & \text{otherwise} \end{cases} \quad (1)$$

Definition 1. *$H_{minExtra}$: The minimum required additional x-directed field to keep a given magnet metastable for all input combinations and for any $t < t_{sw}^M$. It can be expressed as:*

$$H_{minExtra} = \max(\{H_{minExtra}(I_j, t) | I_j \in I, t < t_{sw}^M\}) \quad (2)$$

Thus, the necessary and sufficient condition to keep a magnet in a metastable state such that it does not switch prematurely (implying that a local bias H_x is sufficient) is:

$$H_{minExtra} = 0 \quad (3)$$

C. Conditions for Correct Switching

Here, we introduce criteria for a magnet to successfully switch to a logically correct, easy axis magnetization state when set by an appropriate neighbor (i.e., at time t_{sw}^M). Once a magnet has switched in a properly designed NML circuit, it should remain in a logic 1/0 state until re-evaluated with another input.

From the phase diagram we can determine the maximum tolerable value of H_x such that a magnet remains in a region corresponding to a $\uparrow$ or $\downarrow$ state. For example, per point G in Fig. 2, if $H_x(I_j, t_{sw}^M) = 20\ mT$ and $H_y(I_j, t_{sw}^M) = -10\ mT$, H_x must not exceed $50\ mT$ (indicated by point F). We denote this upper limit of H_x as $H_{max}(I_j, t_{sw}^M)$. For successful switching, the maximum tolerable additional x-directed field for input I_j can be expressed as:

$$H_{maxExtra}(I_j) = \begin{cases} 0 & \text{if } H_x(I_j, t_{sw}^M) \geq H_{max}(I_j, t_{sw}^M) \\ H_{max}(I_j, t_{sw}^M) - H_x(I_j, t_{sw}^M) & \text{otherwise} \end{cases}$$

Definition 2. *$H_{maxExtra}$: The maximum tolerable additional x-directed field so that a magnet can successfully switch for all input combinations. It can be expressed as:*

$$H_{maxExtra} = \min(\{H_{maxExtra}(I_j) | I_j \in\ I\})$$

Thus, the necessary condition for a magnet to switch to a logically correct easy axis state is:

$$H_{maxExtra} > 0 \quad (4)$$

This implies that for all input combinations, $H_x < H_{max}$. If for any input, $H_x \geq H_{max}$ – i.e., $H_{maxExtra} = 0$, a magnet will not be able to transition to the corresponding easy axis. The above analysis results in the following design rule[2]:

Rule 1. *If for any magnet $H_{maxExtra} = 0$, a design is not feasible.*

We use the conditions for hard axis stability (Eqn. 3), and for correct switching (Eqn. 4) to categorize the magnets in an ensemble into two groups per the following definitions:

Definition 3. ***Non-critical magnet**: A magnet is 'non-critical' if, given the existing H_x (from the ensemble and/or clock field), (i) it is capable of remaining in a metastable state such that it does not switch prematurely (i.e., $H_{minExtra} = 0$), and (ii) it can switch to a logically correct easy axis when needed (i.e., $H_{maxExtra} > 0$). That is, a magnet is 'non-critical' if:*

$$(H_{minExtra} = 0) \wedge (H_{maxExtra} > 0) \quad (5)$$

Definition 4. ***Critical magnet**: A magnet is 'critical' if, given the existing H_x (from the ensemble and/or clock field), (i) it requires some additional H_x (i.e., from the clock and/or a static helper) to remain in a metastable state (i.e., $H_{minExtra} > 0$), and (ii) it can switch to a logically correct state (i.e., $H_{maxExtra} > 0$). That is, a magnet is 'critical' if:*

$$(H_{minExtra} > 0) \wedge (H_{maxExtra} > 0) \quad (6)$$

Each magnet in an ensemble should remain metastable until set by an appropriate neighbor. Thus, all magnets must satisfy the condition for *non-criticality* (Eqn. 5).

D. Overall Approach

The central idea of our design methodology is to make each *critical* magnet *non-critical* by setting appropriate values for device-to-device spacing, and by providing x-directed fields from helper cells and/or the clock.

A complete design flow is captured by Fig. 3. The design process takes as input an initial, conceptual circuit layout (e.g., Fig. 4a), and the desired time evolution of the magnets (e.g., Fig. 4b-4j). It first finds permissible pairs of horizontal and vertical spacings (d_x and d_y, respectively) between devices that allow the interior magnets (IM) in all horizontal lines to become *non-critical* (steps 1a, 1b in Fig. 3). The process then iteratively tests the permissible d_x, d_y pairs (step 2) to verify if the rest of the magnets could be made *non-critical* via: (i) a *switchability test* which checks if too much hard axis stability would inhibit switching (steps 3a, 3b), and by (ii) determining the clock field and/or helper cell design and placement to preserve metastability prior to switching (steps 4, 5). Once a suitable d_x, d_y pair is found, the methodology modifies the initial layout by accommodating the newly identified helper cells (step 6). The modified layout is again tested to verify

[2]We use "design rules" to signify conditions that a design must not violate.

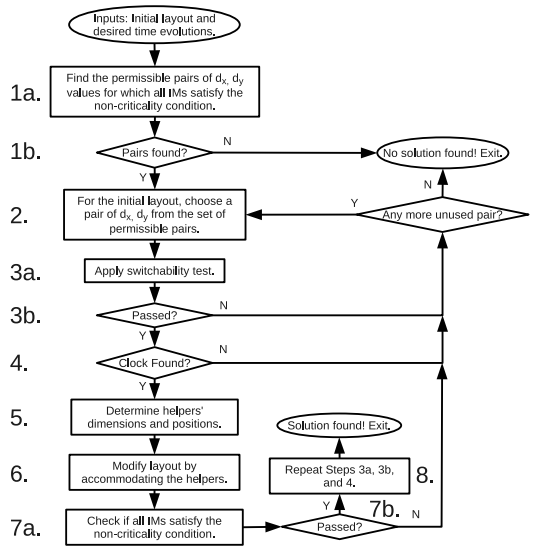
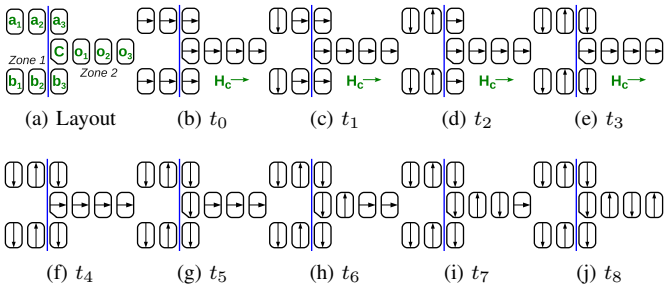


Fig. 3. Design methodology flowchart.



(a) Layout (b) t_0 (c) t_1 (d) t_2 (e) t_3

(f) t_4 (g) t_5 (h) t_6 (i) t_7 (j) t_8

Fig. 4. (a) Initial layout for an AND gate. The slanted magnet edge induces an energy barrier shift that facilitates a 2-input AND [11]. The initial layout also includes the clock boundaries. For example, the AND layout is divided into two separate clocking zones (as shown by the overlaid line) to avoid a potential race condition at magnet C. The initial layout functionally resembles stick diagrams for a CMOS layout; (b)-(j) the desired switching order of the magnets during logic evaluation for input $ab = \downarrow\downarrow$. At t_1 the inputs (magnets a_1 and b_1) are set. A clock field acts on zone 2 (see Section II-B) until time-step t_3 and is removed at the beginning of t_4. The appropriate switching time, t_{sw}^M for a given magnet M is assigned to one of the time-steps t_0 to t_8 during which the magnet is expected to start relaxing. For example, $t_{sw}^C = t_4$ and $t_{sw}^{a_3} = t_{sw}^{b_3} = t_2$.

that: (a) all its IMs are non-critical (steps 7a, 7b), and (b) the rest of the magnets are non-critial (step 8). The design process completes after determining device-to-device spacings, helper cells' size and positions, and a common clock field magnitude.

IV. Detailed Design Approach

We now describe the key steps of our design methodology. The design of an AND gate is used as a running example.

A. Making Interior Magnets Non-critical

Here, we discuss how to achieve *non-criticality* for the interior magnets (IM) in any horizontal, anti-ferromagnetically ordered line (steps 1a, 1b in Fig. 3). (Note that interior magnets in vertical lines can be made *non-critical* by using helpers and/or clock field which will be discussed in Section IV-C.) One can make a *critical* magnet *non-critical* by: (i) setting appropriate values for device-to-device spacings, and/or (ii) providing appropriate x-directed fields from helper cells and/or

Procedure 1 Find Permissible Pairs of (d_x, d_y)

1: **for** each pair $(d_x, d_y) \in D_x \times D_y$ **do**
2: Calculate $H_{minExtra}$ and $H_{maxExtra}$ for each IM using the *phase diagram*.
3: **if** all the IMs satisfy *non-criticality* condition **then**
4: Include (d_x, d_y) within the set of permissible pairs.

Procedure 2 Switchability Test for a permissible (d_x, d_y)

1: **for** each magnet M among the magnets that are not IM **do**
2: Calculate $H_{minExtra}$ and $H_{maxExtra}$ for M using the *phase diagram*.
3: **if** $(H_{minExtra} = 0) \wedge (H_{maxExtra} > 0)$ **then** M is *non-critical*, Continue.
4: **else if** $H_{maxExtra} = 0$ **then return** False.
5: **else if** $(H_{minExtra} > H_{maxExtra}) \wedge M$ is $TypeA$ **then return** False.
6: **return** True.

the clock field if necessary. However, helper cells cannot be used to preserve metastability for IMs (e.g., a_2, b_2, o_1, o_2 in Fig. 4a) in an anti-ferromagnetically ordered line. Additionally, any applied clocking field on the said device might be removed well before it should switch. Therefore, assuming that material and crystalline structure do not change, the only way to make IMs *non-critical* is to augment device-to-device spacing.

Procedure 1 illustrates how to find permissible d_x and d_y pairs such that each IM satisfies the *non-criticality* condition. Here, D_x and D_y are the set of values of d_x and d_y to be tested. The cartesian product $D_x \times D_y$ contains all possible pairs of d_x and d_y. For a given (d_x, d_y), we use the phase diagram to calculate $H_{minExtra}$ for all IMs (line 2 of Procedure 1) by utilizing Eqn. 1, and Eqn. 2. For a given magnet M, Eqn. 1 needs: (i) the minimum required x-directed field to keep M in a metastable state which is readily found from the phase diagram, and (ii) the existing x-directed field over M exerted by the rest of the magnets in the ensemble. Note that this can be obtained with a micro-magnetic simulator. With Eqn. 2, we consider all the time-steps that precede t_{sw}^M. Similarly, we calculate the values of $H_{maxExtra}$ for all IMs. For the given (d_x, d_y), if all the IMs satisty the *non-criticality* condition (Eqn. 5) the pair is included in the set of permissible pairs.

For the running example of the AND gate design in Fig. 4a, D_x and D_y range from 6 nm to 15 nm and 15 nm to 36 nm respectively. (Only intervals of 3 nm – the smallest multiple of our simulation mesh – are considered.) Thus, we find the set of permissible pairs to include all (d_x, d_y) with d_x: 6 to 9 nm and d_y: 15 to 36 nm. Note that, a designer can further filter the permissible set with fabrication constraints.

B. Switchability Test

Now, we introduce the *switchability test* (Procedure 2) to determine – for a given (d_x, d_y) – whether magnets that are not IM can switch to a logically correct, easy axis state (steps 3a, 3b in Fig. 3). Any permissible (d_x, d_y) pair already guarantees the *non-criticality* of IMs. The design process iteratively invokes this test to find a permissible (d_x, d_y) pair that allows the non-IMs to satisfy the second requirement for *non-criticality* – being able to switch to an easy axis.

For a given (d_x, d_y), for each of the non-IMs, we again calculate the values of $H_{minExtra}$ and $H_{maxExtra}$. If a magnet is found to be *non-critical* (line 3, Proc. 2), the test simply continues to the next non-IM. However, if $H_{maxExtra}$ is equal to zero for a magnet (line 4, Proc. 2), i.e., if it cannot switch, the design becomes infeasible according to Rule 1 (see

Sec. III-C). If a magnet is not *non-critical*, and does not fail to switch according to Rule 1, it is *critical*.

We now consider *critical* magnets in more detail. We define a *critical* magnet M as $TypeA$, if time-step t_{sw}^M, when M begins to switch, is not the same as time-step, t_c, when the clock field is removed, i.e., $t_{sw}^M \neq t_c$. In contrast, if $t_{sw}^M = t_c$, i.e., switching begins as a direct consequence of clock field removal, a magnet is $TypeB$. In the AND gate initial layout (Fig. 4a), if initially *critical*, magnet C would be a $TypeB$ magnet, and magnets a_3, b_3 and o_3 would be $TypeA$.

For a $TypeA$ *critical* magnet, $H_{minExtra}$ must be less than $H_{maxExtra}$ to enable successful switching. As an example, assume a given magnet M is $TypeA$ *critical*, for which $H_{minExtra}$ is 20 mT and $H_{maxExtra}$ is 15 mT. We need to provide at least 20 mT additional x-directed field on this magnet to keep it in a metastable state before t_{sw}^M. But at t_{sw}^M, the upper bound for tolerable additional x-directed field is 15 mT. As such, the magnet will never be able to switch. For $TypeB$ *critical* magnets, if $H_{minExtra} > H_{maxExtra}$, the applied additional x-directed field will be reduced at t_{sw}^M as the clock field is removed, thus the same problem does not occur. The following design rule results:

Rule 2. *A design is not feasible if for any $TypeA$ critical magnet, $H_{minExtra} > H_{maxExtra}$.*

For our running example, we iteratively tested permissible (d_x, d_y) pairs for *switchability* and found that acceptable pairs included $(9\ nm, 21\ nm)$ and $(6\ nm, 21\ nm)$.

C. Determination of Clock Field and Layout Results

We now discuss steps 4, 5 (Fig. 3) of our design methodology. Since a (d_x, d_y) pair that passes the switchability test results in a layout where all magnets are either *non-critical* or *critical*, the focus now is to make all *critical* magnets *non-critical* (i.e., ensure that *critical* magnets remain metastable and do not switch prematurely). We achieve this by leveraging the clock field and/or helper cells to provide additional x-directed fields on the *critical* magnets.

Here we focus on finding the clock field (Proc. 3) due to page limit. The clock field only effects magnets that reside next to the clock boundary and switch at or before t_c (e.g., a_3, b_3, C). For each such magnet, we determine the minimum required (C_{min}^M) and the maximum tolerable (C_{min}^M) clock fields (line 2-5). For magnets that switch before t_c (e.g., a_3, b_3), $C_{min}^M = 0$ (required additional field coming from helper), and $C_{max}^M = H_{maxExtra}$ (when no helper is used). A magnet switching at t_c experiences the clock field only before switching. Thus, it can tolerate an infinite clock field (line 3). At t_c, this magnet experiences field contribution only from a helper, and this field can at most be $H_{maxExtra}$ (otherwise, the magnet will not switch). Therefore, before switching, the magnet must see a clock field of at least $H_{minExtra} - H_{maxExtra}$ (line 4) such that the total field for metastability becomes $H_{minExtra}$. Note that, if $H_{minExtra} \leq H_{maxExtra}$, the helper alone (contributing $H_{maxExtra}$) can satisfy metastability, hence $C_{min}^M = 0$ (line 5). A range for the clock field is determined in line 6-7. A value within this range is chosen as a clock field (line 8). If the clock field is not enough for metastability, additional field is provided via a helper cell.

Procedure 3 Find Clock field

1: **for** each critcical magnet M next to the clock boundary with $t_{sw}^M \leq t_c$ **do**
2: **if** $t_{sw}^M < t_c$ **then** $C_{max}^M = H_{maxExtra},\ C_{min}^M = 0$
3: **else if** $t_{sw}^M = t_c$ **then** $C_{max}^M = \infty$
4: **if** $H_{minExtra} > H_{maxExtra}$ **then** $C_{min}^M = H_{minExtra} - H_{maxExtra}$
5: **else** $C_{min}^M = 0$
6: C_{max} = minimum of the C_{max}^M values.
7: C_{min} = maximum of the C_{min}^M values.
8: **if** $C_{max} \geq C_{min}$ **then** choose any value between C_{min} and C_{max} as clock.
9: **else** clock not found, **return** False.

Magnets:	a_3, b_3	C	o_3
$H_{minExtra}$ (mT)	35	41	20
$H_{maxExtra}$ (mT)	37	12	35
C_{max}^M (mT)	37	∞	-
C_{min}^M (mT)	0	29	-

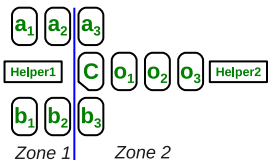


Fig. 5. Values for the critical magnets, and the final AND layout with $d_x = 9\ nm$ and $d_y = 21\ nm$. Both the helpers are $87 \times 39 \times 5\ nm^3$ in dimension. $Helper1$ is 18 nm left from C and $Helper2$ is 6 nm right from o_3.

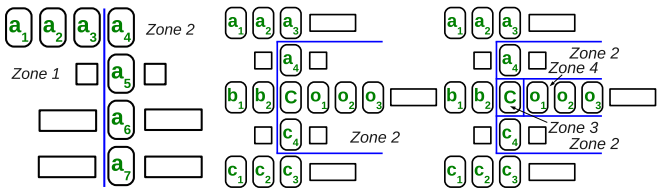
For the AND gate with $(d_x, d_y) = (9\ nm, 21\ nm)$, the corresponding values for the *critical* magnets a_3, b_3, o_3 and C are shown in Fig. 5. The clock range is found to be 29 to 37 mT. From this range we fix the clock field as 35 mT. With this clock field, no helper is required for a_3 and b_3. For magnet C, at least 6 mT must be provided via a helper cell, and this helper contribution cannot exceed 12 mT. Using OOMMF, we found that a $87 \times 39 \times 5\ nm^3$ helper placed 18 nm away from C satisfies the above requirement. The helper cell for magnet o_3 must provide a field between 20 mT and 35 mT. A $87 \times 39 \times 5\ nm^3$ helper cell placed 6 nm away from o_3 provides a 23 mT field. (This helper cell mimics an adjacent clock group, and would be omitted in a larger design.)

We modify the initial layout by accommodating the helper cells (step 6 in Fig. 3). These helper cells will exert magnetic fields on all devices in the circuit, and thus can alter their characteristics. Therefore, for the modified layout, further testing as shown in Fig. 3 is then conducted, and the clock field is again determined following the aforementioned procedure. With our running example, the finalized clock field is 30 mT. To verify the final layout (Fig. 5), we simulated it in OOMMF at $0K$. The time evolution of the design was correct for all inputs.

We have also applied our methodology to design a corner turn and a 3-input majority gate. In a corner turn, a signal transitions from an anti-ferromagnetic line to a ferromagnetic line, and thus it functions as interconnect. The final layouts for both corner turn (Fig. 6a) and majority gate (Fig. 6b), evolve correctly in time for all input combinations when simulated at $0K$.

V. Thermal Noise Consideration

Thermal noise can have a significant impact on the behavior of NML circuits and could lead to unwanted magnetization states. For example, during simulation of the initial corner turn design (Fig. 6a) at $300K$, magnet a_3 switches prematurely to a wrong easy axis state for input $a = \uparrow$. This problem is due to the fact that thermal excitation essentially introduces a random magnetic field. Specifically, thermal noise in a micro-magnetic model can be expressed as an equivalent stochastic magnetic



(a) (b) (c)

Fig. 6. (a) Final layout for a corner turn with $d_x = 9\ nm$ and $d_y = 24\ nm$. All helpers are $9\ nm$ away from the magnets. The helpers of a_5 are $39 \times 39 \times 5\ nm^3$, and those for a_6 and a_7 are $87 \times 45 \times 5\ nm^3$ in dimension. When zone 2 is clocked by a $23\ mT$ field, input propagates correctly up to a_4. After the clock is removed, a_5, a_6 and a_7 switch in order. (b) Final layout for a majority gate (at $0K$) with $d_x = 9\ nm$, $d_y = 15\ nm$ and a clock field of $50\ mT$. Three $87 \times 39 \times 5\ nm^3$ helpers are placed $9\ nm$ right from a_3, o_3, c_3 and two $39 \times 39 \times 5\ nm^3$ helpers are placed $9\ nm$ away from a_4 and c_4 on both sides. Inputs propagate correctly up to a_3, b_2, and c_3. After the clock is removed: i) a_4 and c_4 switch first, ii) then the compute magnet C switches, and iii) lastly o_1, o_2, o_3 switch in order. (c) Final Layout for a majority gate (at $300K$) such that: i) distances between a_1 and a_2, c_1 and c_2 are $6\ nm$. ii) Clocking fields for zone 2, 3, and 4 are 40, 50, and 30 mT, respectively. Clock field is first removed from zone 2, then from zone 3 and lastly from zone 4. iii) distances between C and a_4, C and c_4 are $21\ nm$ and distance between C and o_1 is $6\ nm$.

field [12], [13] where $g(t)$ is a Gaussian random distribution with unit variance and zero mean, V is the volume of the nanomagnet, and Δt is the discretization in time:

$$H_{thermal} = \frac{1}{\sqrt{V\Delta t}}\sqrt{\frac{2kT\alpha}{\mu_0\gamma M_S}}g(t) \tag{7}$$

By setting Δt to the relaxation period of zone 1 (here, it is $1\ ns$), we get a representative value for thermal noise on magnet a_3. At $300K$, for 1 million Gaussian-distributed random numbers, $H_{thermal}$ varies from $-2.4\ mT$ to $+2.4\ mT$.

For the corner turn layout, before switching, a_3 operates within the metastable region in the phase diagram (point R in Fig. 2), but resides so close to the border that thermal noise may easily shift the operating point, R out of the metastable region. For example, with a y-directed $H_{thermal}$ of $-2.4\ mT$, R would shift to the bottom end of the overlaid vertical line shown in Fig. 2. Thus, premature switching is possible. To combat this problem, we move point R further to the right into the metastable region by increasing the x-directed field on a_3 such that the point can have more margin for thermal shift and reside within the metastable region. This is accomplished by changing the distances between a_3 and a_2, a_3 and a_4 to $6\ nm$ (from $9\ nm$ in the $0K$ design). 100 simulations (at $300K$) of this layout evolved correctly for all input combinations.

Other designs also need to be adjusted to accommodate thermal noise. For AND gate (Fig. 5) simulation at $300K$, for input $ab = \uparrow\downarrow$, magnet C does not switch to a $\downarrow$ state within $1\ ns$, and remain metastable. When a longer relaxation period was allowed, C sometimes required $4\ ns$ to switch. This would obviously have a negative impact on clock period. In this case, the operating point resides in the $\downarrow$ region of the phase diagram close to the border, and thermal noise shifts it into the metastable region. To solve this, the operating point is moved further left by decreasing the H_x field. This is done by changing the distance between C and $Helper1$ to $30\ nm$ and clock field to $34\ mT$. 100 simulations at $300K$ evolved correctly for all input combinations where C switched within $1\ ns$.

Thermal simulations of the initial majority gate design (Fig. 6b) at $300K$ illustrated three problems: (i) a_2 and c_2 switch prematurely, (ii) the state of C is dominated by b_2 if a_4 and c_4 were slow while switching to their corresponding easy axis states, and (iii) o_1 switches prematurely. The layout for $300K$ (Fig. 6c) solves case (i) by increasing the x-directed field on the magnets (bringing the neighbors of a_2 and c_2 closer) such that they have more margins in the metastable region to withstand thermal noise. For case (ii) the race condition on C is eliminated by separating it into a different clocking zone such that it can respond only after all of its adjacent previous neighbors are set. The more complex clocking zones can be supported by voltage controlled clock scheme [14]. To solve case (iii) of o_1, both clocking zone separation and x-directed field increment were required. For this layout, 100 thermal simulations for all input combinations were all correct.

VI. Conclusion

We show that it is possible to generate predictable design solutions for NML circuits in a systematic manner. The proposed methodology can be implemented as a CAD tool to facilitate faster layout identification. Our approach is applied to find functional layouts for a 2-input AND gate, corner turn, and majority gate – which eventually could be used to construct any boolean circuit. Formal design of larger circuits by using the constructs investigated in this paper as building blocks will be considered in future works. While current driven clocking is the context for this work, how our methodology could be applied given other clocking methods will also be considered.

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