System-Level Modeling and Microprocessor Reliability Analysis for Backend Wearout Mechanisms

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***Abstract*—Backend wearout mechanisms are major reliability concerns for modern microprocessors. In this paper, a framework which contains modules for backend time-dependent dielectric breakdown (BTDDB), electromigration (EM), and stress-induced voiding (SIV) is proposed to analyze circuit layout geometries and interconnects to accurately estimate state-of-art microprocessor lifetime due to each mechanism. Our methodology incorporates the detailed electrical stress, temperature, linewidth and cross-sectional areas of each interconnect within the microprocessor system. We analyze several layouts using our methodology and highlight the lifetime-limiting wearout mechanisms, along with the reliability-critical microprocessor functional units, using standard benchmarks.**

Keywords—Wearout Mechanisms; Microprocessor; Reliability; EM; SIV; SM; TDDB; Aging

I. Introduction

Although constant technology scaling has resulted in considerable benefits, including smaller device dimensions, higher operating temperatures and electric fields have also contributed to faster device aging due to wearout. Not only does this result in the shortening of processor lifetimes, it leads to faster wearout resultant performance degradation with operating time.

Each technology generation reduces the interconnect dimensions without always reducing the supply voltage in proportion. This results in higher electric fields within the backend dielectric and within the metal lines, increasing wearout in the backend geometries. At the same time, as the dielectric constant (*k*) decreases to reduce parasitics, as prescribed by the *International Technology Roadmap for Semiconductors* (ITRS), the porosity of materials must increase, at the possible cost of increasing the vulnerability of materials to breakdown. The faster operating frequencies of processors result in decreased interconnect reliability as well, due to increases in both electrical current and operating temperature. These factors combine to increase the risk of failure of chips due to backend breakdown in the newer technology nodes.

The physics describing IC failure mechanisms in the backend has matured as a result of years of refinement to existing theories. However, the extension of these models to large and complex microprocessor systems has not proven to be straightforward and is complex. Microprocessor system reliability analysis requires techniques to extend the results gathered from small test structures to large complex microprocessors. Such an endeavor requires methods to manage the deluge of data that comes with analyzing large layouts.

The purpose of this paper is to present a methodology to assess microprocessor lifetimes due to each wearout mechanism by developing the link between the device level wearout models and the architecture level. We have focused on backend wearout mechanisms, namely BTDDB, EM, and SIV, and have demonstrated the feasibility of our methodology by presenting results from a simulator based on the proposed methodology.

Since the wearout mechanisms under study are activity and temperate dependent, the proposed framework determines the detailed thermal profile of the system under study, as well as the electrical stress of each net in the system. Hence, we compute the detailed activity and operating temperature of each functional unit in the system. The lifetime-limiting wearout mechanisms, along with the reliability-critical microprocessor functional units, are highlighted using standard benchmarks. This enables a designer to make any updates in the design to enhance reliability prior to committing a design to manufacture.

The rest of the paper is organized as follows. Section 2 gives a brief overview of the related work and recent trends. Section 3 presents our bottom-up hierarchical wearout prediction framework and summarizes our methodology to estimate microprocessor lifetime due to each wearout mechanism. Our methodology incorporates the microprocessor geometries, temperature profile, and stress conditions. Section 4 gives the overview of our system-level aging assessment framework. The methodology to determine model parameters through FPGA emulation is also described. In Section 5, we study the lifetimes for the microprocessor system from our simulator and present a comparison based on our results. Section 6 concludes the paper.

II. Related Work

The first step in insuring reliable system operation is to bridge the gap between the established device level wearout models and system behavior at the architecture level. The current mean-time-to-failure (MTTF) based high level reliability models, such as [1],[2], only provide us with crude, single point, reliability estimates based on the assumption that the system is a series combination of the components.

These methods assume an exponential failure rate distribution and that we can compute a MTTF for each mechanism and each block. However, each block is composed of a large number of elements, all failing at different rates, based on their temperature, electrical stress, and geometry. Moreover, component failure rates are typically modeled with Weibull or Lognormal distributions, rather than exponential distributions. Hence, the methodology to determine the MTTF for each block, as required in [1],[2], is not clear. Instead, we work with process-level models directly, and propagate these models to system-level models.

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This is not the first attempt to develop a system-level reliability simulator incorporating multiple mechanisms, without the use of the standard exponential distribution to characterize components and blocks. In [3], a system-level reliability simulator has been developed that includes EM, SIV, gate-oxide breakdown (GOBD), and thermal cycling based on process-level models. However, the implementation is limited to 50,000 or fewer devices. We get around this problem through the use of an FPGA-based emulator to generate activity and temperature profiles.

III. Bottom-Up Hierarchical Wearout Prediction

Wearout mechanisms can be divided into two broad categories, the voltage (or E-field) dependent wearout mechanisms, such as negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), GOBD, and BTDDB etc., and the current stress-dependent wearout mechanisms, such as EM. Due to the lack of higher level models for the progressive effect of these mechanisms, it is necessary to first model their effects at the device level and then abstract the models to the micro-architecture level. For this work we have focused on backend wearout mechanisms, namely BTDDB, EM and SIV.

It is common to describe backend wearout mechanisms with a Weibull distribution

$$P(TF) = 1 - \exp\left(-\left(TF/\eta\right)^{\beta}\right), \quad (1)$$

having two parameters: the characteristic lifetime, η, and shape parameter, β. The characteristic lifetime is the time-to-failure at the 63% probability point, when 63% of the population have failed, and the shape parameter describes the dispersion of the failure rate population. The physics of each wearout mechanisms is linked to the Weibull parameters in the sections below.

A. Backend Time-Dependent Dielectric Breakdown (BTDDB)

In order to calculate the vulnerability of a layout due to BTDDB, the BTDDB simulator operates by determining the vulnerable length of the microprocessor layout for each linespace. The vulnerable length, L_i, is defined as the length of a block of dielectric between two copper lines separated by linespace S_i, illustrated in Fig. 1. A given layout is analysed by determining the pairs (S_i, L_i) for each layer for all linespaces. The details of our methodology can be found in [4]-[6].

The characteristic lifetime of a dielectric segment of the microprocessor, with vulnerable length, L_i, associated with linespace, S_i, is

$$\eta = A L_i^{-1/\beta_i} \exp\left(-\gamma E^m - E_a/kT\right), \quad (2)$$

where A is a constant that depends on the material properties of the dielectric, γ is the field acceleration factor, m is one for the E model [7],[8] and $1/2$ for the $\sqrt{E}$ model [9],[10]. The electric field is a function of voltage, V, and the linespace, S, between the two lines surrounding a dielectric segment, i.e., $E=V/S$. The electric field, temperature (T), and geometry (L_i) determine the characteristic lifetime, η. The temperature dependence is modeled with the Arrhenius relationship [11],

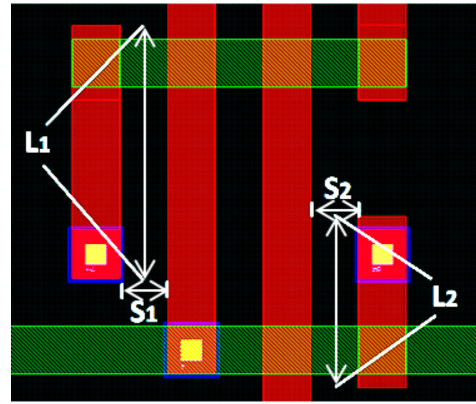

Fig. 1. The vulnerable length associated with a linespace is shown. The rectangles are copper wires, surrounded by the backend dielectric.

[12], where k is the Boltzmann constant, q is the electronic charge, and the activation energy, $E_a \propto q\left(\phi_B - \sqrt{qE/\pi\varepsilon}\right)$, is field dependent. The data used in our study comes from experimental data obtained from [4]-[6].

It should be noted that process data comes from test structures that are stressed with DC stress, while the microprocessor dielectrics undergo AC stress. For segments of the microprocessor, it is sufficient to determine the time that each dielectric segment is under stress. To translate the DC stress of the test structure to the AC stress of the circuit, we compute the probability that each adjacent net has opposite voltages, α. Let's suppose that there are n different probabilities of segments being under stress, α_n, for linespace, S_i. Then the corresponding characteristic lifetime for linespace, S_i, under use conditions is

$$\eta_{S_i} = \eta_{dc} \sum_m \left(\alpha_n^{\beta}\right)^{-1/\beta}. \quad (3)$$

We collect the electrical state profiles of each net within the microprocessor while running standard benchmarks [13] using FPGA emulation described in Section 4. First, we find the probability that each net is at logic "1". We then compute the stress probability of a dielectric segment as the probability that the two adjacent nets are at different logic states. If the adjacent state probabilities are p_1 and p_2, then

$$\alpha = p_1(1-p_2) + p_2(1-p_1). \quad (4)$$

The microprocessor system under study includes 310k nets which form around 31 million dielectric segments to be analyzed in the layout.

B. Electromigration (EM)

EM refers to the dislocation of metal atoms caused by momentum imparted by electrical current in interconnects and vias. Once a void is formed, it grows and causes an increase in resistance. The resistance is allowed to increase until a maximum tolerable value is reached, which is used as the failure criterion. The characteristic lifetime, η, of an interconnect line under EM is of the general form [14]-[17]

$$\eta = \frac{L_{via}}{v_d} = \frac{h}{\delta_s} \frac{kTL_{via}}{eZ*\rho j D_s}, \quad (5)$$

where v_d is the velocity of the void and L_{via} is the via size. v_d is a function of the effective charge, Z*, the current density, j, the resistivity of the conducting metal, ρ, and the electron charge, e. For Cu, since the surface diffusivity, D_s, is much

larger than the interface diffusivity, the effective diffusivity is given by the surface diffusivity times the surface thickness, δ_s, and divided by the thickness of the line, *h*. An EM failure occurs when the void spans the via size, L_{via}. The data on EM used in this study comes from Choi's experimental data [14].

In order to calculate the vulnerability of a layout to EM, the EM simulator operates by determining the characteristic lifetime of each interconnect segment within the microprocessor layout. To better model the reliability of the microprocessor under EM and determine the accurate current density of each interconnect, we collect the switching activity profiles of each interconnect while running standard benchmarks [13] using FPGA emulation and take into account the temperature, RC parasitics, and cross-sectional area of each interconnect segment.

C. Stress-Induced Voiding (SIV)

SIV damage is caused by the directionally biased motion of atoms in interconnects due to mechanical stress caused by thermal mismatch between metal and dielectric materials. Based on the SIV dependence on both temperature and geometric linewidth, the characteristic lifetime, η, of an interconnect line under SIV is given by [18],[19]

$$\eta = AW^{-M}(T_0 - T)^{-N}\exp(E_a / kT) \tag{6}$$

where *W* is the linewidth, *M* is the geometry stress component, T_0 is the stress-free temperature, *N* is the thermal stress component, and *A* is a constant. The data used in our study of SIV comes from Yao's experimental data [18].

Similar to the EM simulator, the SIV simulator operates by determining the characteristic lifetime of each interconnect within the microprocessor layout.

D. Microprocessor Lifetime Models

The characteristic lifetime of the microprocessor, $\eta_{processor}$, is the solution of [4]-[6]:

$$1 = \sum_{i=1}^{n} (\eta_{processor} / \eta_i)^{\beta_i} \tag{7}$$

Similarly [5],

$$\beta_{processor} = \sum_{i=1}^{n} \beta_i (\eta_{processor} / \eta_i)^{\beta_i} \tag{8}$$

For BTDDB, the components in (7) and (8) could be different layers of a microprocessor, different geometries within a layer, or different geometries within a layer at different temperatures. Hence, the simulator (a) determines the characteristic lifetimes and shape parameters for all of the underlying geometries or components of each layer, accounting for temperature and use conditions with equation (2) for BTDDB, equation (5) for EM, and equation (6) for SIV, and (b) applies (7) and (8) to solve for $\eta_{processor}$ and $\beta_{processor}$. Equations (7) and (8) provide a method to combine millions of component-level Weibull distributions into a single system-level Weibull distribution.

IV. Aging Assessment Framework

A. Layout Feature Extraction

The layout is broken down into dielectric segments for BTDDB and interconnect segments for EM and SIV.

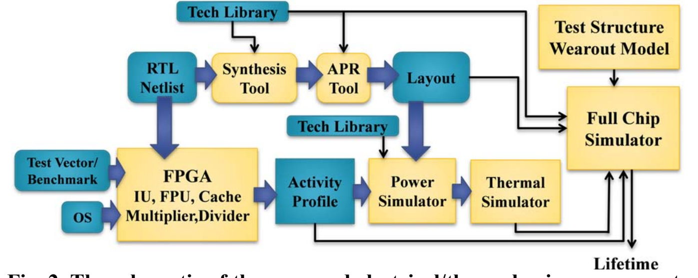

Fig. 2. The schematic of the proposed electrical/thermal aging assessment framework is shown. Yellow blocks indicate tools, while blue blocks indicate data.

BTDDB requires the determination of the vulnerable length of the dielectric segments as a function of linespace. We have developed a layout extraction tool using the standard object oriented programming language C++. A detailed description of the algorithm is given in [20].

After extraction of the dielectric segments' length and linespace, each dielectric segment is linked to its thermal and stress profile in order to compute its characteristic lifetime with (2). Temperature is a function of the location of the segment in the layout, and stress is a function of the state probabilities of the adjacent nets.

EM and SIV also depend on temperature. For these two wearout mechanisms, the location of each interconnect segment is determined to provide a link to its thermal profile. The switching activity of the net is converted to a current density, which is combined with the thermal data to find the interconnect segment's characteristic lifetime for EM with (5). The width of the net is combined with the thermal data to find the interconnect segment's characteristic lifetime for SIV with (6).

B. Electrical/Thermal Profile Acquisition

A framework for the acquisition of spatial and temporal thermal/electrical stress of a system was constructed.

Running RTL or SPICE simulations of a complete microprocessor to extract the activity profile of each net is not feasible in most cases, since it may take a few months to finish simulating a single benchmark. On the other hand, simulating microprocessors with standard benchmarks on an FPGA takes only a few minutes. Our electrical aging assessment framework is schematically described in Fig. 2, which provides an efficient way to acquire electrical and thermal profiles for any digital system for use in system-level reliability analysis.

For analyzing the impact of different wearout mechanisms on a microprocessor system, we have used the well-known open-source LEON3 IP core processor [22] with superscalar abilities. The microprocessor logic units consist of a 32-bit general purpose integer unit (IU), a 32-bit multiplier (MUL), a 32-bit divider (DIV) and a memory management unit (MMU). Storage blocks include a window-based register file unit (RF), separate data (D-Cache) and instruction (I-Cache) caches, and cache tag storage units (Dtags and Itags). The LEON3 processor was synthesized using an IBM 90nm technology library.

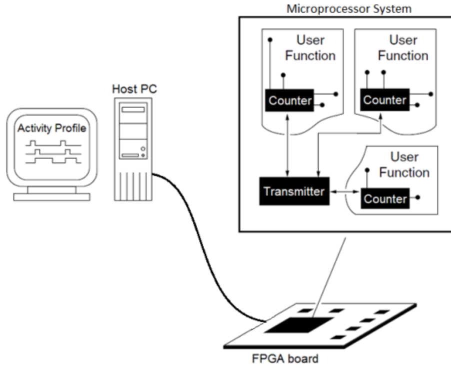

Fig. 3. The system used to collect activity profile of microprocessor contains an FPGA board that implements the microprocessor system and exports data on the activity profile to a PC.

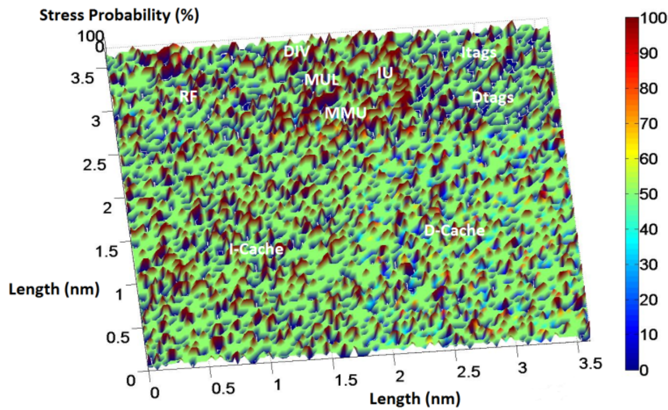

Fig. 4. The distribution of the dielectric stress probability for the microprocessor is shown while running a standard benchmark.

For activity tracking, the hardware RTL/netlist of the design under study was synthesized for an FPGA, and counters were placed at the I/O ports, which track both the state probabilities and the toggle rates of the ports during application runtime, as illustrated in Fig. 3. A standard set of benchmarks [13] were used as the applications for the analysis. The output of the FPGA emulation is I/O activities and state probabilities.

The I/O activities and the gate-level netlist were then used for activity propagation to each net in the design, depending on its logic behaviour, for a complete stress/transition probability profile of the internal nodes of the microprocessor under study. This component is done in software on a block-by-block basis. Thus, we have the probability of a transition occurring at any node and the probability at each state, i.e., the probability at logic "1". Fig. 4 and Fig. 5 show the distributions of the dielectric stress probability and the transition rate, respectively, when the microprocessor is running a standard benchmark.

Besides activity variation, the temperature variation throughout the microprocessor is taken into account when modeling different wearout mechanisms. The netlist was also used for layout generation, as shown in Fig. 2. The RC information from the layout, together with the net activities, were used for the extraction of the power profile and the

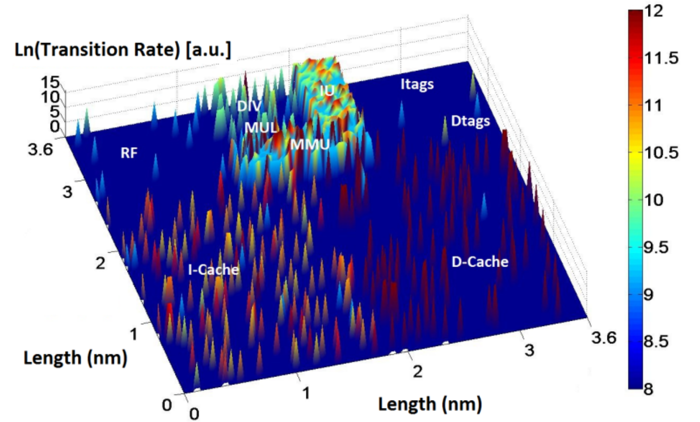

Fig. 5. The distribution of the transition rate for the microprocessor is shown while running a standard benchmark.

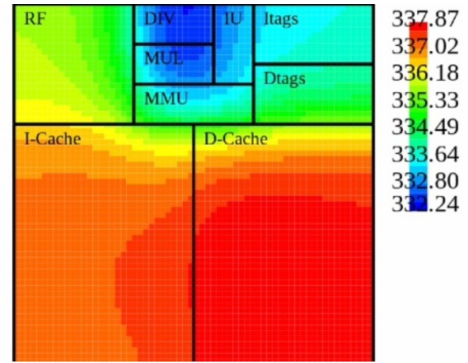

Fig. 6. The average temperature distribution for the microprocessor is shown while running a standard benchmark.

consequent thermal profile, through the power simulator [22] and the thermal simulator [23], respectively, for every single unit of the microprocessor system. Fig. 6 shows the average temperature distribution when the microprocessor system is running a standard benchmark.

Then, using the layout, the thermal profile and the calculated probability of current flow and voltage stress, we can use device level models (equations (2), (5), and (6)) to characterize any wearout mechanism in every feature in the layout and unit of the microprocessor under study to determine the wearout profile of the system. The component level models are combined with equations (7) and (8) to find the system wearout distribution for each backend wearout mechanism. These are the final blocks in Fig. 2 that output the lifetime.

Note that our current implementation uses an average temperature for each benchmark. As can be seen in Fig. 2, the thermal simulator is only run once. However, temperature transients in long runs can be included by implementing a feedback loop during the operation of each benchmark, as was done in [24] for smaller systems.

V. Estimated Lifetime for The Microprocessor System

A set of standard benchmarks [13] were run on the microprocessor system under study. The microprocessor includes 20 – 25k gates, and the runtime for executing

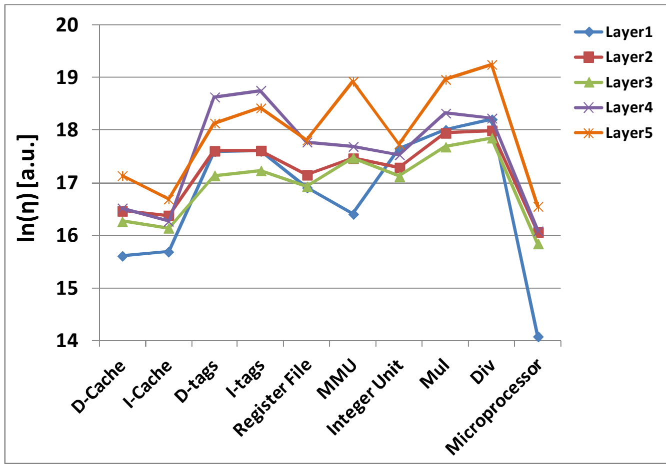

Fig. 7. Characteristic lifetimes for each layer and for each unit in the microprocessor system due to BTDDB indicate the most vulnerable blocks and layers.

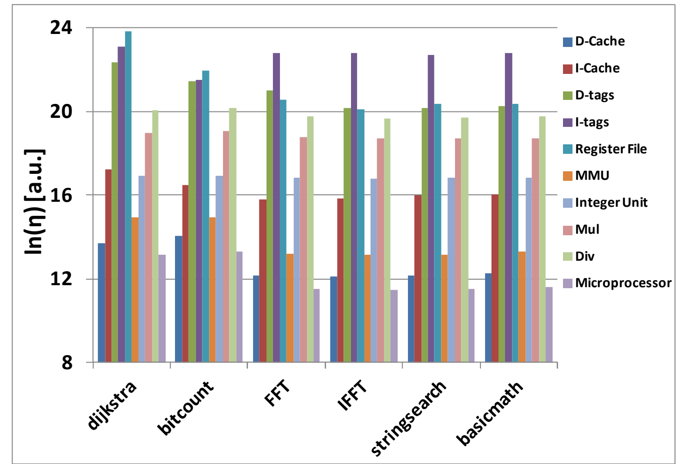

Fig. 9. Characteristic lifetime results under different benchmarks for each unit in the microprocessor system due to EM indicate the most vulnerable blocks.

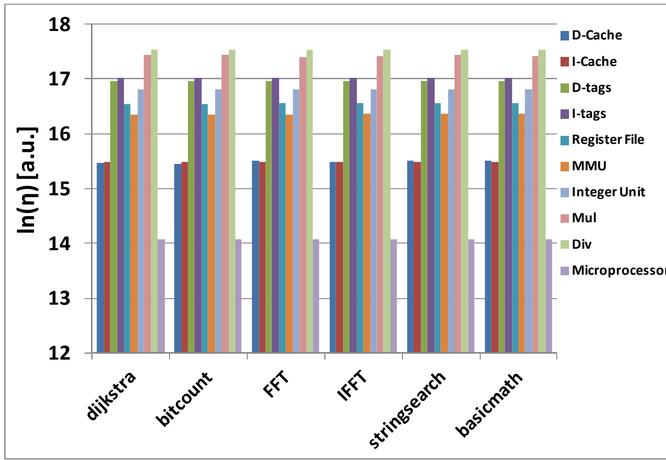

Fig. 8. Characteristic lifetime results under different benchmarks for each unit in the microprocessor system due to BTDDB indicate the most vulnerable blocks.

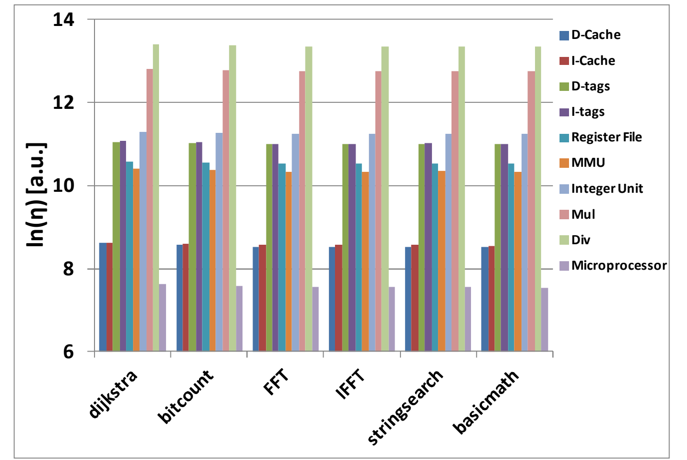

Fig. 10. Characteristic lifetime results under different benchmarks for each unit in the microprocessor system due to SIV indicate the most vulnerable blocks.

benchmarks on the system is around 15 minutes. The technology library used is IBM 90nm. The electrical stress and thermal profiles for the system were collected using the framework described in Section 4. The electrical and thermal profiles, together with the lifetime models from Section 3, were then used to estimate the lifetime of each functional unit in the microprocessor system.

The microprocessor system can be broken down into two distinct groups: the storage units and the combinational logic units. The storage units include the data cache, the instruction cache, the two cache units for tag storage, and the register file. The combinational logic units include the memory management unit, the integer unit, the multiplier, and the divider.

For BTDDB, we have estimated the lifetime of each microprocessor unit and analyzed the lifetime for every metal layer in the design technology used under different benchmarks, as shown in Figs. 7 and 8. Figs. 7 and 8 report the characteristic lifetimes, η. The characteristic lifetime is the probability point when 63% of the population has failed.

When the characteristic lifetime is combined with the shape parameter, β, we have a complete probability density distribution, given by equation (1). The lifetime of the microprocessor system under BTDDB is clearly limited by the Metal 1 layer. As we move up in the metal layer stack, the metal spacing increases, resulting in an increased time-to-failure. Our analysis shows that the data cache and the instruction cache are the lifetime-limiting units in the microprocessor. Among the combinational units, lifetime is limited by the MMU and the IU, while the MUL and the DIV blocks have relatively better lifetimes. Figs. 4, 6, 7 and 8 also clearly suggest a strong temperature dependence of functional unit lifetimes.

The microprocessor system lifetime was also investigated under EM. The results for the expected lifetimes of the microprocessor and each unit under EM are shown in Fig. 9. The lifetime limiter is expected to be the data cache under EM. A comparison of these results with the activity and thermal profiles shown in Figs. 5 and 6, respectively, indicates the strong activity and temperature dependence of functional unit

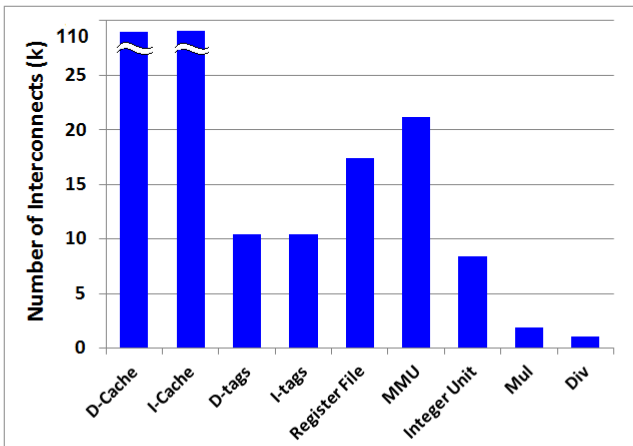

Fig. 11. The number of interconnects of each unit in the microprocessor system is shown.

lifetimes. Among the logic units, the memory management unit is expected to have the shortest lifetime under EM.

The microprocessor system lifetime under SIV was also analyzed. The results for the expected lifetimes of the microprocessor and each unit under SIV are shown in Fig. 10. The results for SIV for the microprocessor system indicate that the system lifetime is limited by the data cache lifetime. SIV is a function of metal density. The number of interconnects in each unit is shown in Fig. 11. A comparison of the results in Fig. 10 with the thermal profiles and the number of interconnects of each unit shown in Figs. 6 and 11, respectively, indicates a strong temperature and interconnect count dependence of the functional unit lifetimes. Among the logic units, the memory management unit is expected to have the shortest lifetime under SIV.

VI. Conclusion

This paper presents a simulation workflow to analyze state-of-art microprocessor reliability. Taking into account the detailed thermal and electrical stress profiles of microprocessor systems while running standard benchmarks, a methodology is proposed to accurately assess microprocessor lifetime based on backend wearout mechanisms. In addition, this paper presents a way to establish the link between the device-level wearout models and the architecture level. Combining the wearout models, the thermal profile, and the electrical stress profile, this work provides insight into lifetime-limiting wearout mechanisms, along with the reliability-critical microprocessor functional units for a system, while using standard benchmarks.

Future work will add frontend wearout mechanisms to the existing framework to provide a capability for complete system-level wearout evaluation.

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