A Low-Power and Low-Voltage BBPLL-based Sensor Interface in 130nm CMOS for Wireless Sensor Networks

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***Abstract*—A low-power and low-voltage BBPLL-based sensor interface for resistive sensors in Wireless Sensor Networks is presented. The interface is optimized towards low power, fast start-up time and fast conversion time, making it primarily useful in autonomous wireless sensor networks. The interface is time/frequency-based, making it less sensitive to lower supply voltages and other analog non-idealities, whereas conventional amplitude-based interfaces do suffer largely from these non-idealities, especially in smaller CMOS technologies. The sensor-to-digital conversion is based on the locking behavior of a digital PLL, which also includes transient behavior after start-up. Several techniques such as V_{DD} scaling, coarse and fine tuning and pulse-width modulated feedback are implemented to decrease the transient and acquisition time and the power to optimize the total energy consumption. In this way the sensor interface consumes only 61μW from a 0.8V DC power supply with a one-sample conversion time of less than 20μs worst-case. The sensor interface is designed and implemented in UMC130 CMOS technology and outputs 8 bit parallel with 7.72 ENOB. Due to its fast start-up time, fast conversion time and low power consumption, it only consumes 5.79 pJ/bit-conversion, which is a state-of-the-art energy efficiency compared to recent resistive sensor interfaces.**

I. Introduction

Wireless Sensor Networks (WSNs) are a growing application domain [1]. Sensor nodes typically consist of a sensor, a sensor interface to digitize the sensor information, a transceiver to communicate the data, and an energy supply block. In autonomous WSNs, techniques such as energy harvesting can be used to supply the sensor nodes. Typically, the harvested power is lower than the power needed by the WSN electronics, so energy is stored in a capacitor from which the electronics are powered later on [2]. Contrary to continuously sampled systems, these interfaces start up, digitize one value and are then again switched off to save energy. Therefore the energy needed to complete one operation includes the start-up time and one sensor-to-digital conversion, revealing the need for interfaces with fast start-up time, low power consumption and fast conversion time.

This paper presents a time-based sensor interface for resistive sensors that fulfills these requirements. The time-based design makes fast start-up and conversion times possible, while several techniques such as V_{DD} scaling, coarse and fine tuning and pulse-width modulated feedback are introduced to decrease the power and energy consumption. The low-power digitally-oriented time-based approach makes this interface very useful in autonomous WSNs.

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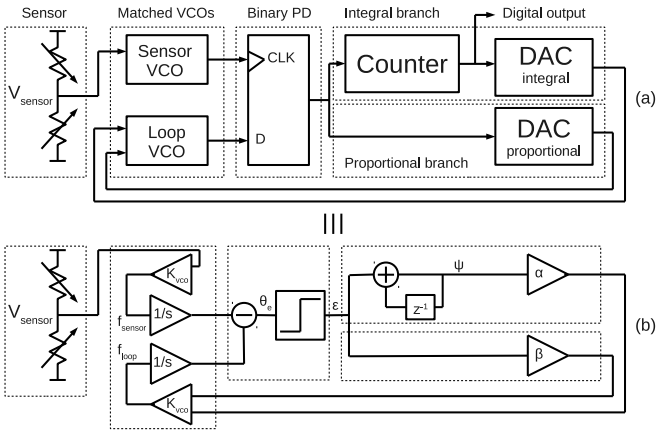

Fig. 1. Architecture of the BBPLL-based sensor interface

The paper is organized as follows. In section II, an overview of the design approach and interface architecture is given. Next, section III discusses some of the implemented building blocks. The circuit has been prototyped in UMC130 CMOS technology. Finally, in section IV, the measurement results are discussed and compared to other state-of-the-art resistive sensor interfaces. Section V concludes this paper.

II. System level overview

The basic architecture of the resistive sensor interface is given in Fig. 1, while an extended version of the system, including the lock detector and the pulse-width modulated feedback, is depicted in Fig. 2.

A. Resistive sensor readout approach

Traditional resistive bridge readout circuits involve amplification, filtering and analog-to-digital conversion. These analog building blocks tend to consume much power and are a real challenge in smaller silicon CMOS technologies due to the low supply voltage (1V and lower) and the small sensor signal swing [3]. In this design, the problem is approached from a

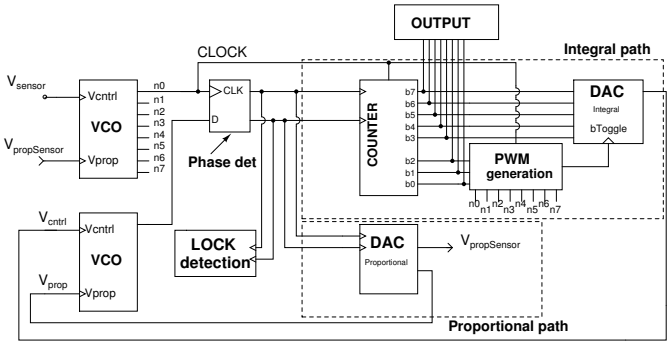

Fig. 2. Complete architecture of the BBPLL-based sensor interface including the lock detector and the pulse-width modulated feedback.

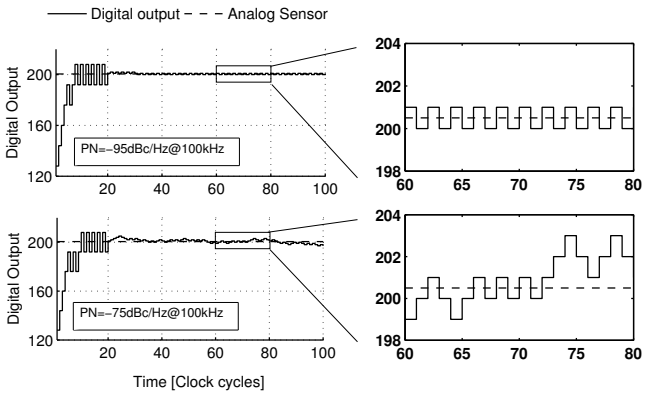

Fig. 3. Simulated transient behavior of the 8-bit digital output as a function of time. Coarse tuning is applied during the first 20 clock cycles to speed up the locking. Phase noise ($1/f^2$) is added to both VCOs: (top) -95dBc/Hz@100 kHz and (bottom) -75dBc/Hz@100 kHz.

time-based point of view. By converting the analog amplitude signal to the time/frequency domain with a Voltage-Controlled Oscillator (VCO), the quantization and other processing can be done in the digital domain. Hereby one can avoid extra analog building blocks for the preconditioning of the analog sensor signal. Recently, time-domain processing and sensing has received a lot of attention and recent publications also prove the superior energy efficiency of these time-based implementations for resistive [4] [5] [6] and capacitive [7] [8] [9] sensors.

B. BBPLL-based interface architecture

To convert the sensor frequency signal to a digital equivalent, a phase-locked loop (PLL)-based interface architecture is proposed. In essence, the analog sensor amplitude signal is first converted to the frequency domain by the VCO (i.e. FM modulation), whereafter it is demodulated directly to the digital domain by employing a digital PLL, which is based on a second-order Bang-Bang Phase-Locked Loop (BBPLL) [10] (see Fig. 1 (a)). The depicted converter involves two VCOs whose phase difference is sampled by a binary phase detector (implemented with a D-flipflop), which acts as a single-bit quantizer. Due to the loop dynamics, the frequency of the VCO in the loop is locked onto the frequency of the sensor VCO, which is controlled by the sensor signal (cfr. FM demodulation). If both VCOs are identical and are running at the same frequency (in lock), both controlling signals must be the same. If the sensor signal is an analog signal and the loop signal is a digital signal controlling the loop VCO through a digital-to-analog converter (DAC), the digital signal is equivalent to, or is a digital version of the analog signal.

C. Working principle

An equivalent block diagram of the architecture in Fig. 1 (a) is shown in Fig. 1 (b). The input frequency f_{sensor} is the modulated sensor signal in the frequency domain and is equal to:

$$f_{sensor} = f_{nom} + K_{vco} \cdot V_{sensor} \tag{1}$$

with f_{nom} the free-running frequency and K_{vco} the linear gain factor of the sensor VCO. The frequency of the loop VCO equals

$$f_{loop} = f_{nom} + K_{vco} \cdot (\epsilon \cdot \beta \ + \alpha \cdot \psi) \tag{2}$$

assuming that both VCOs are identical, where $\epsilon = sign[\theta_e]$, θ_e is the phase error between the two VCOs, ψ is the accumulation of ϵ in time and β and α are the gain factors of the respectively proportional and integral path. The ratio $R = \beta/\alpha$ is defined as the stability factor and determines both the stability and the speed of convergence during start-up [10]. When the BBPLL is locked, the output of the loop filter exhibits limit cycles in the absence of VCO-induced jitter (phase noise) and it has been proven that in locked condition the average value of ϵ is zero [10]. This means that we can state:

$$V_{sensor} = \alpha \cdot mean(\psi) \tag{3}$$

with ψ the n-bit output of the digital counter. Depending on the wanted accuracy, the n-bit digital word ψ can be averaged over a longer period. In order to determine whether the PLL is in lock or not, a lock detection mechanism has to be deployed.

D. Transient behavior and lock detection

Due to its application in autonomous WSNs, the start-up and transient behavior of the PLL are also important, since this is included in the total conversion time. Fig. 3 shows the simulated transient and locking behavior from start-up of an 8 bit digital output for a constant sensor value with fixed parameters α and β and $1/f^2$-modeled phase noise added to the two VCOs. With little phase noise, the output exhibits a limit cycle with the covered values close to the desired value (see the top zoomed plot in Fig. 3). In this case it is possible to pick the digital 8-bit value closest to the actual value without filtering, but by employing a lock detector to detect the limit cycle. However, in the presence of much phase noise, the noise overrules the limit cycle and the digital output starts to act randomly around the desired value (see the bottom zoomed plot in Fig. 3). Although the average remains unchanged (statistically, over a longer period), it is not possible to make a correct decision in a short time with a lock detector because of the randomness of the signal. Since filtering of the output is not employed here to save energy, the absolute value of ψ determines the precision of the

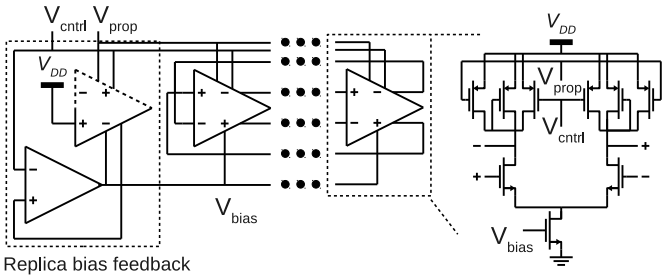

Fig. 4. 4-stage differential VCO with replica bias feedback. The differential cell is shown on the right.

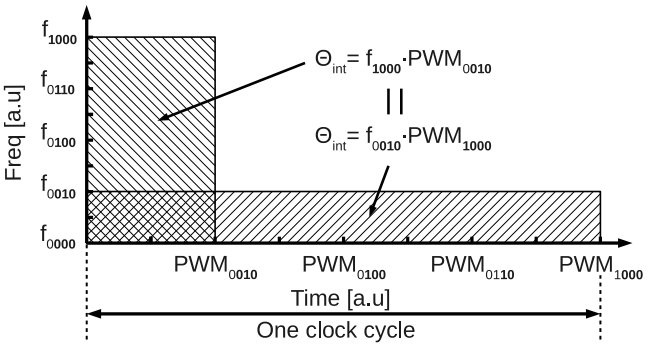

Fig. 5. The principle of pulse-width modulating the output of the DAC in the integral path.

digitization. Note that the resolution of the output is set by the resolution of the counter and that the precision is determined by the ability to pick the correct value out of the limit cycle. For a certain resolution, the value of α is fixed, leaving only one design variable β, whose value depends on the desired stability and convergence specifications. Once both parameters are determined, the specifications for the phase noise (jitter) of the VCOs can be derived, based on simulations, to meet the wanted precision. For 8-bit precision and resolution, at most -85dBc/Hz@100kHz (4MHz center frequency) phase noise ($1/f^2$) can be tolerated so that the limit cycles are still present and the lock detector can recognize them, as simulated.

To detect limit cycles and thus a locking behavior, digital circuitry is implemented to recognize locking patterns (limit cycles) at the output of the phase detector (also see Fig. 2). Simulations have shown that 6 different patterns in a data span of 10 subsequent samples are enough to detect every limit cycle. The lock detector is implemented as a 10-bit shift register with combinational logic to detect predefined patterns. Once a locking pattern has been detected, the lock detector outputs a flag to stop the conversion and turn off the sensor interface.

E. Coarse and fine tuning

It is clear that the transient behavior of the BBPLL from start-up to a locking condition is very important, since it is also included in the total conversion time. If the n-bit counter is initialized to $2^n/2$, for n=8, the acquisition time would take 128 clock cycles (worst case), excluding start-up behavior and cycles needed to detect a locking condition. To speed up this conversion time and to minimize the number of clock cycles, coarse and fine tuning is introduced. This means that the conversion is done in two phases: one in which the granularity of the step in the feedback path is larger (coarse tuning) and one in which it is equal to one LSB of the counter (fine tuning). The lock detector also determines whether the loop should go from coarse to fine tuning (identical lock detection mechanism). It can be calculated that the optimal distribution of the n bits is n/2 bits for coarse and n/2 bits for fine tuning [11]. This results in $2{\cdot}2^{(n/2)}/2$ clock cycles (worst case) or 16 clock cycles for n=8, which is a speed-up of 8 compared to the regular case (excluding overhead). As depicted in Fig. 3, at start-up a larger step size is used in the feedback loop by adding/subtracting 16 LSB instead of one LSB in the counter at every clock cycle. Since this speeds up the transient behavior significantly, we save much energy ($Energy = Power \cdot Time$), up to a factor 8x theoretically.

III. Implementation in CMOS

A. Voltage-Controlled Oscillator

For both the Sensor VCO and Loop VCO, a differential ring oscillator is implemented with replica bias feedback to bias the delay cells (Fig. 4) [12]. The replica bias network dynamically biases the current sources and forces the single-ended output swing between V_{DD} and V_{cntrl}, resulting in a linear tuning characteristic [12]. As already depicted in Fig. 1, the proportional and integral path are not added before the VCO, but are combined in the VCO by providing two almost equivalent inputs (V_{cntrl} and V_{prop}) to control the VCO frequency (see Fig. 2 and 4).

The load elements of the differential cell lead to a high dynamic supply noise rejection and the dynamically biased current sources provide a high static supply and substrate noise rejection, as has been shown in [12]. This leads to less influence of supply and substrate noise on the phase noise performance of the VCO, compared to single-ended ring oscillators in which environmental noise such as supply noise can kill the performance [13].

Regarding phase noise, -95dBc/Hz@100kHz (f_0=4 MHz) is obtained in simulations, satisfying the required specification of maximum -85dBc/Hz@100kHz. The power consumption of the oscillators is 12.9μW each.

B. Pulse-width modulated feedback

To save energy in the DAC of the integral path (see Fig. 1 (a)), only a 5-bit resolution DAC (with minimally 8-bit accuracy) is implemented instead of an 8-bit resolution DAC, as is depicted in Fig. 6. The extra 3-bit resolution is obtained by pulse-width modulating an extra LSB of the 5-bit resolution DAC. It is important to understand that the D-flipflop is a phase detector and not a frequency detector. This means that the integrated phase at the output of the Loop VCO during one clock cycle of the Sensor VCO is important and not the frequency. Therefore, it does not matter whether the frequency f_{0010} is integrated during the whole clock cycle or whether the frequency f_{1000} is integrated during $2/8^{th}$ of the clock cycle

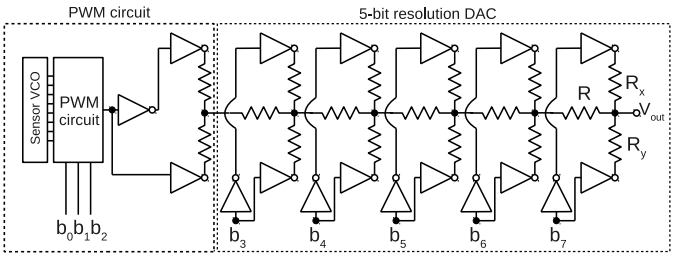

Fig. 6. The DAC in the integral path: this is a subranging R2R DAC with extra LSB to be controlled by the PWM circuit.

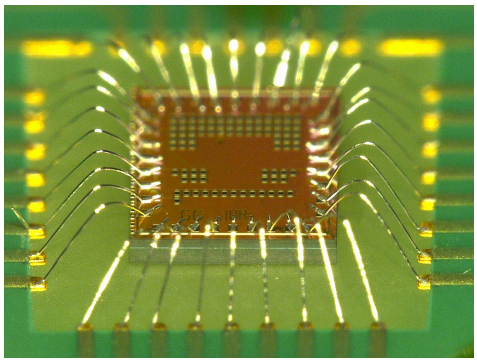

Fig. 7. Microphotograph of thechip prototyped in UMC130 CMOS technology. The active area is 455μm x 435μm.

(see Fig. 5). In this way only the frequencies f_{0000} and f_{1000} are used in the feedback loop, omitting the need for the 3 extra bits in the DAC. To divide the clock cycle of the Sensor VCO into 8 equal parts (=3 bit), the internal Sensor VCO signals (8 in total, because 4-stage differential) are used to generate the PWM signal which controls the extra LSB in the DAC (also see Fig. 2).

C. Subranging R2R DAC in voltage mode

The proportional path in the feedback loop only has two states (0 and 1), which means that the DAC in the proportional path can easily be implemented as a resistive divider. The DAC in the integral path, however, should have an output range which matches the output range of the resistive sensor divider, which is 10% of V_{DD} in this application. Due to matching constraints, this is very hard to implement with a voltage divider. In addition, to be able to implement PWM in the DAC, an extra LSB should be available that can be switched IN/OUT. To fulfill these requirements a subranging R2R DAC in voltage mode is implemented (Fig. 6) [14]. The output range is solely defined by the ratio of the resistances R_x and R_y [14]. Therefore we can avoid the use of low-output-impedance voltage references, which reduces the power budget significantly. Moreover, by using the R2R DAC in voltage mode instead of current mode, it can directly be connected to the high-impedance input of the Loop VCO. By using the R2R ladder structure, the extra LSB is also inherently present in the DAC and can be used to implement the PWM technique. With PWM tuning, the power consumption of the DAC dropped with 30 % from 28.7μW to 20.1μW, which is a 12% decrease of the total power consumption.

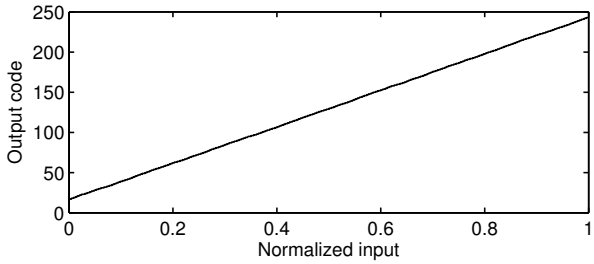

Fig. 8. Input-output characteristic of the sensor interface. 8-bit digital output code as a function of the normalized input range. The limited output range is due to mismatch between both oscillators, which means a decreased locking range.

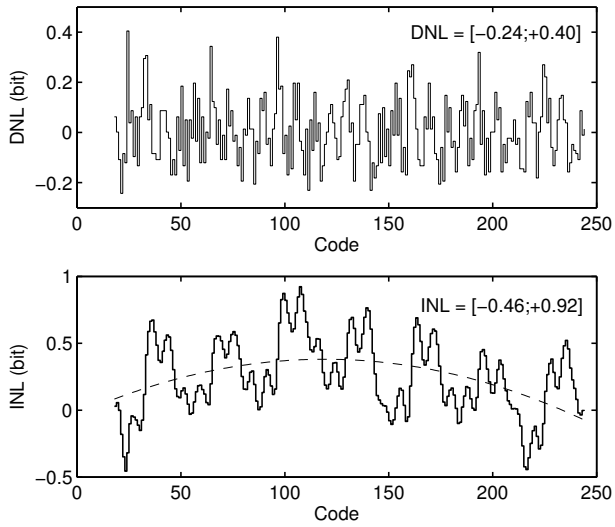

Fig. 9. DNL and INL (calculated with the best-fit method) as a function of the digital output code of the sensor interface.

IV. Measurement results

Fig. 7 shows the microphotograph of the prototype chip, which was fabricated in UMC130 CMOS technology and occupies an active area of 455μm x 435μm. Measurements have been performed with a resistive potentiometer of 10kΩ emulating the resistive sensor. The maximal variation of the emulated sensor resistance is $\pm$10%, meaning that the dynamic input range of the interface is 10% of the supply voltage (e.g. 360-440 mV at V_{DD} = 0.8V). Fig. 8 shows the measured input-output characteristic of the sensor interface at V_{DD} = 0.8V. From the plot it is clear that not the entire output range is covered. This is due to the offset between the characteristics of the Sensor VCO and Loop VCO, which makes that the lock range of the PLL is decreased. As a result, the output dynamic range is decreased, which results in a degradation of the ENOB. However, this can easily be solved by adapting the gain factors in the feedback path during design. At V_{DD} = 0.8V, the measured peak DNL error is -0.24/+0.40LSB, and the peak INL error is -0.46/+0.92LSB, as shown in Fig. 9. The INL shape clearly shows second-order non-linearity, which is mainly due to the second-order non-linearity of the characteristics of the VCOs. The recurring $'M'$-shape is due to the 3-bit PWM tuning in the feedback loop. At the same supply

TABLE I
COMPARISON OF RECENT RESISTIVE SENSOR INTERFACES

Reference	Topology	Input sensor variation	ENOB	Power [μW]	Conversion time [ms]	FOM (pJ/bit-conv.)	CMOS techn[μm]	Supply voltage [V]	Measurement
[5]	time-based	$\pm$ 100 %	14.13	366	1	20.4	.13	1.2	Yes
[15]	amplitude-based	$\pm$100%	12.4	6000	10	11101	.35	3.3	Yes
[6]	time-based	$\pm$ 70 %	13	27.5	5	16.78	.35	2.5	No
[16]	amplitude-based	$\pm$1.6 %	21	1350	100	64.37	.7	5	Yes
[4]	time-based	$\pm$10 %	8.90	124.5	0.05	13.03	.13	1	Yes
This work	time-based	$\pm$10 %	7.72	61	0.02	**5.79**	.13	0.8	Yes

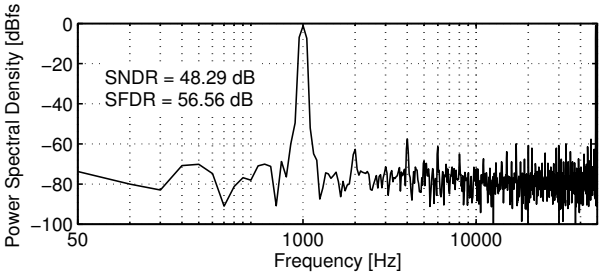

Fig. 10. Output power spectral density with f_s=50kHz and an input signal of -1dB$_{FS}$.

voltage, the output spectrum is measured at a sample frequency of 50kS/s and an input signal amplitude of -1dB$_{FS}$. The second-order distortion is the limiting factor for the SNDR, which is measured to be 48.29 dB, resulting in 7.72 ENOB. The measured SFDR is equal to 56.56 dB.

At V_{DD}=0.8V, the maximum power consumption is measured to be 61μW and the average conversion time for one sample from start-up is measured to be less than 20μs. The lock detection mechanism to detect the limit cycles has proven to be robust during measurements, confirming that the phase noise specifications are within the specified range. A comparison with the state-of-the-art for resistive sensor interfaces is given in Table I. The Figure of Merit (FoM) to compare the energy efficiency is defined as follows:

$$FoM = \frac{Power[W] \cdot Conv.time[s]}{2^{ENOB}} \quad (4)$$

Although 7.72 ENOB is relatively low compared to the other interfaces, it performs better in terms of power and conversion time, resulting in a superior FoM of only 5.79pJ/bit-conversion, which is state-of-the-art for resistive sensor interfaces.

V. CONCLUSION

This paper has described a low-power, 8-bit resolution, fully-integrated time-based sensor interface for resistive sensors. It is optimized towards low power and fast conversion time to increase the energy efficiency. The introduced coarse and fine tuning to decrease the transient behavior of the PLL can speed up the acquisition time up to 8x, which translates to energy savings per conversion. The pulse-width modulation technique in the feedback loop results in a 12% decrease of the total power, due to the 3-bit savings in the resistive R2R DAC in the integral feedback path. Combined with the scaling of V_{DD} to 0.8V instead of 1.2V in UMC130 CMOS technology, the total power consumption of the chip is only 61μW. The sensor-to-digital converter achieves a SNDR of 48.29dB, or 7.72 ENOB, and a one-sample conversion time of less than 20μs worst-case. This results in a state-of-the-art energy efficiency of 5.79 pJ/bit-conversion for resistive sensor interfaces. The energy efficiency combined with the fast start-up time makes this sensor interface very suitable for autonomous WSNs.

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