

A Sub- μA Power Management Circuit in $0.18\mu m$ CMOS for Energy Harvesters

Biswajit Mishra, Cyril Botteron, Gabriele Tasselli, Chritian Robert and Pierre-André Farine
Ecole Polytechnique Fédérale de Lausanne, Electronics and Signal Processing Laboratory, Neuchâtel, Switzerland 2000
Email: biswajit.mishra@epfl.ch

Abstract—We explore a miniature sensor node that could be placed in an environment which would interrogate, take decisions and transmit autonomously and seamlessly without the need of a battery. With the system completely powered by an energy harvester for autonomous operation, the power management becomes crucial. In this paper, we propose an ultra low power management circuit implemented in $0.18\mu m$ CMOS technology. As part of a stringent power requirements and very limited power offered by the energy harvesters, the proposed circuit provides a *nanowatt* power management scheme. Using postlayout simulation, we have evaluated the power consumption of the proposed power management unit (PMU) and report results that compares favorably to the state of the art.

I. INTRODUCTION

One of the key challenges in pervasive computing and wireless sensor networks is energy harvesting, where the focus is to develop energy harvesters to power electronic devices, particularly in wearable and embedded sensors where batteries are cumbersome or impractical. The key to efficient use of such systems is to optimize individual subsystems and look at them holistically [1]. Another important aspect relates to the generated voltage and/or current from the harvester, which may be too low to be directly used by the sensor node. Typically, the voltage (power) generated from a solar (cell area of $25mm^2$) or vibration energy harvester ($\sim 5\mu W/mm^3/g^2$) is of the order of few tens of mV (nW) to a couple of hundreds of mV (μW to mW). Therefore it is usually necessary to up-convert the voltage generated from the energy harvester by a booster stage that typically suffers from low efficiency. Most of the reported research on boost converters for energy harvesters employs microwatt power management schemes and suffer from low efficiency [2], [3], [4], [5]. Moreover, within indoors, the harvesters produce limited power, the power being in the order of nW to a few μW [6]. In this case, as long as the power consumption of the PMU and node is less than the generated power, the sensor node will be able to obtain energy autonomy. Therefore, for these nodes to have the ability to accumulate energy, nW power management circuit is essential. In this paper, we discuss the design and performance of a sub- μA power management circuit consuming nW power - fitting to the power constraints of such energy harvester powered nodes. When compared to reported PMU's in the literature, our proposed PMU has lowest power and compares favorably with state of the art sense and transmit sensor nodes [2], [3], [4], [5].

II. PROPOSED PMU

The conceptual sensor node shown in Fig 1 consists of a solar or vibration harvester, a PMU, a sensor interface (Sensor IF), an Ultra WideBand transmitter (UWB TX), and an antenna. The Low Dropout Regulator (LDO), voltage monitor, digital control circuit, Ultra Low Power Clock circuit (ULP Clock), $100ns$ Clock, power switches P_1 , P_2 and storage capacitors C_1 and C_2 constitute the proposed power management unit (PMU).

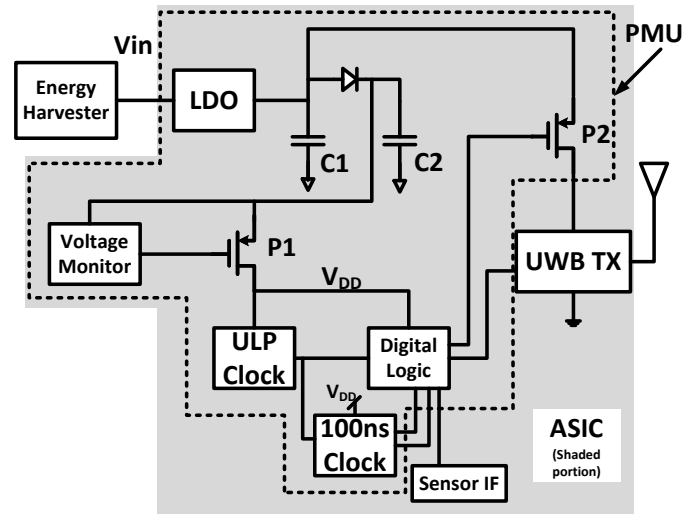


Fig. 1: Block Diagram of Nanowatt Power Management Unit

The PMU interfaces the energy harvester with a diode to prevent any back current from the solar harvester and an optional AC-DC (not shown in Figure) for the vibrational harvester. The tiny amount of harvested power is being trickle charged in the capacitor and cannot be used on a continuous basis. Hence the PMU is responsible for converting the energy generated from the harvester into a usable form. Moreover, the voltage generated from the harvester is not stable. Therefore, the LDO is used to provide a stable output, saturating at $1.8V$ and the energy is stored in capacitors C_1 and C_2 for powering up the voltage monitor, sensor interface, ULP Clock, digital logic and other circuitry. As the energy stored in the capacitors raises, the voltage level which is continuously sensed by the voltage monitor also raises. As soon as it reaches a defined threshold voltage, the voltage monitor closes the PMOS switch P_1 . The voltage monitor is ON all the time and

as it consumes static power, thus it must be carefully designed for low power. Once the switch P_1 is closed, the ULP clock and the digital logic are enabled. The digital logic consists of two timers with a periodicity of $6sec$ and $96sec$, and generates control/enable signals for reading and processing the sensor data every $6sec$ and transmitting it every $96sec$. Thus, the UWB TX circuit is only enabled by the P_2 switch every $96sec$ to minimize standby power consumption. If the energy is inadequate for operation or the harvester is not able to provide enough energy during any phase of PMU operation, the voltage monitor disables P_1 . As soon as the voltage reaches a specified voltage threshold, the PMU resumes operation. Furthermore, to isolate the supply voltage variation due to the higher current requirements for UWB transmitter provided by C_1 , another storage capacitor C_2 is used.

In the following sections, we discuss the design and performance extracted from post-layout simulations of the sub-blocks that constitute the PMU (for the UWB-TX block, the reader is referred to [11]).

III. SUBTHRESHOLD LOW DROPOUT REGULATOR

The transistor level schematic of the low dropout regulator (LDO), adapted from [7], is shown in Fig 2. The LDO regulates the input voltage greater than $1.8V$ to a stable V_{DD} at $1.8V$. The LDO is designed to operate in the subthreshold region so that the current consumption is low. The basic blocks are the reference voltage, error amplifier, bias network, resistive divider and the series MOS transistor switch. The output voltage is given by $V_{out} = V_{ref}(1 + \frac{R_1}{R_2})$ where R_1 and R_2 are the upper and lower values of the resistances from the resistive divider circuit. The error amplifier compares the output voltage sampled from the resistive divider circuit with the V_{ref} and controls the current through the MOS transistor switch. The current is either increased or decreased depending on whether V_{out} is low or high.

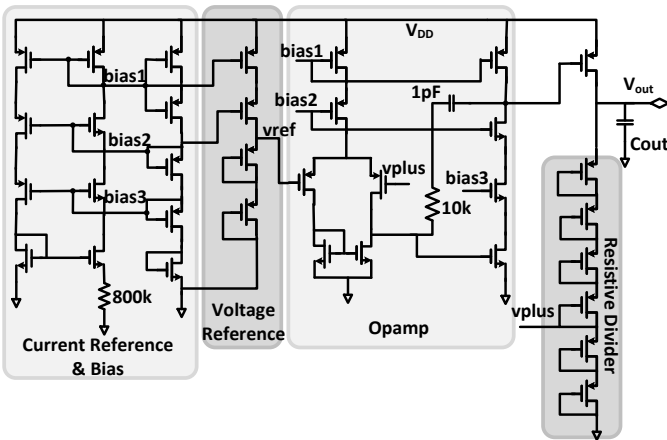


Fig. 2: Schematic Diagram of Low Dropout Regulator [7]

As shown in Fig 2, a PTAT current reference which is required to design the V_{ref} is used to generate the regulated voltage as well as bias the amplifier. The PTAT voltage in

the weak inversion is $V_{ref} = \frac{kT}{q} \ln \frac{(W/L)_2}{(W/L)_1}$ that generates a PTAT current $I_{ref} = \frac{V_{ref}}{R}$ of approximately $21nA$ through the resistor R (adjusted to $800k$), that is extracted by the current mirror to bias the operational amplifier. The bias circuit generates the bias voltage by stacking the transistor diodes that act as resistive dividers. It is optimized for subthreshold operation and ultra low power consumption. The series-connected transistors in leakage mode contribute to less than a few nA current. The bias circuit improves the I_{ref} circuit in terms of linearity and supply rejection. As the subthreshold current I_{ds} is dependent on the gate voltage and V_{ds} , cascoding reduces the dependence on the supply voltage.

The error amplifier is a two stage opamp with cascoded output stage and is also designed to operate in the subthreshold region to reduce the quiescent current throughout the voltage and temperature range. The opamp used in the LDO has a DC gain of $54dB$ and a UGBW of $200kHz$ and consumes $42nA$. At $2.2V$, the bias circuit consumes $42nA$, V_{ref} consumes $24nA$ and the divider circuit consumes $22nA$. It draws a total current of $130nA$ at $2.2V$ and $215nA$ at $3V$. It is worth noting that, as the LDO supply can vary, the series MOS switch at the output stage is chosen to operate at a higher breakdown voltage.

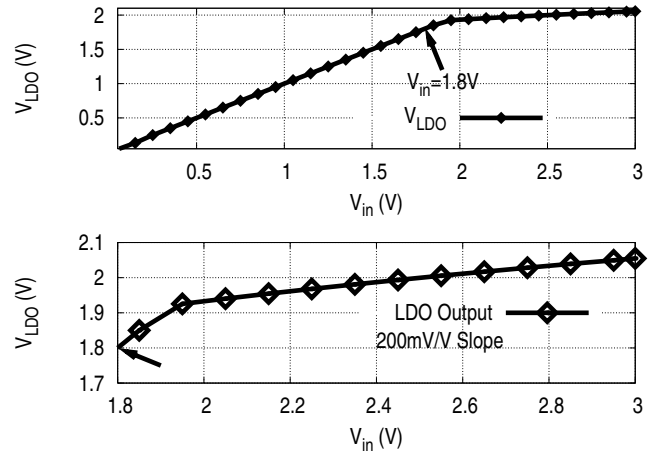


Fig. 3: V_{out} v/s V_{in} of LDO

The DC response of the LDO is shown in Fig 3. The top plot shows the linear response up to $1.8V$ while the bottom plot shows a $\frac{200mV}{V}$ slope for the operating region above $1.8V$ due to the moderate gain achieved by the subthreshold operation.

IV. ULTRA LOW POWER CLOCK CIRCUIT

The block diagram of the proposed clock circuit is shown in Fig 4. The clock circuit provides a $50kHz/20\mu s$ clock input to the digital logic. It consists of a voltage reference circuit (V_{ref}), a clock oscillator and a level shifter circuit. These three circuit blocks are capable of operating at low voltages, i.e. at subthreshold voltages and consume very little power which is one of the fundamental requirements for energy harvester powered electronics [9]. As shown in Fig

4, the output of the V_{ref} block is fed to a bias circuit (with diode and a PMOS transistor) that provides a constant current and then a constant supply voltage (V_{SRC}) to the ring oscillator. The reference output voltage saturates to $230mV$ with approximately $500mV$ at the input. The generated supply voltage (V_{SRC}) at this stage is $390mV$ (below the threshold voltage of the transistor) for the ring oscillators to operate in the subthreshold region. The rail to rail swing of the clock output is $390mV$. As the supply voltage of the load circuit is higher, the amplitude of the clock circuit needs to be brought back to the V_{DD} level or the supply voltage. This is done by the level shifter stage. The voltage reference circuit is similar to the one discussed in section V-A. The V_{ref} generates a reference voltage that is used for the bias circuit to generate the supply voltage for the ring oscillator. The ring oscillator and the level shifter is explained in the following.

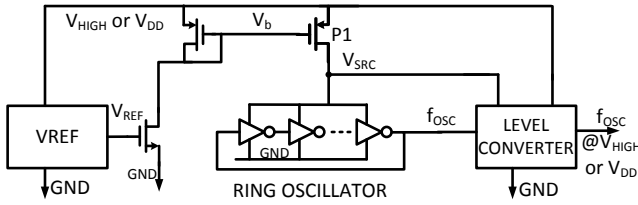


Fig. 4: Ultra Low Power Clock Circuit

A. Ring Oscillator

As depicted in Fig 4, the ring oscillator consists of 7 inverter stages that are sized for ultra low power operation. The supply voltage from the V_{ref} and bias circuit is held to a nearly constant voltage (V_{SRC}) so that the current drawn is constant over input voltage. Given a constant bias voltage $V_{DD} - V_b$, the sensitivity of the oscillation frequency ($f_{osc} = \frac{1}{t_d}$) to the supply voltage (V_{DD}) is related with the following equation:

$$t_d = \frac{C_{OSC} V_{SRC}}{\mu C_{ox} \frac{W}{2L} (V_{DD} - V_b - V_{th})^2 \lambda} \quad (1)$$

Where C_{OSC} is the capacitance of a single stage, V_{SRC} is the source voltage for the oscillator usually at $390mV$, μ is the mobility, λ is channel modulation index (process parameters), C_{ox} is the oxide capacitance, W and L are the width and length of the transistor respectively, V_{DD} is the supply voltage of the circuit, V_b is the bias voltage and V_{th} is the threshold voltage of the transistor. As can be seen from the simulation results (Fig 6b), the frequency has a sensitivity of approximately $24kHz/Volt$ when V_{DD} was varied from $0.5V$ to $1.8V$. We also observe that the sensitivity increases with V_{DD} close to or below $0.5V$ because the transistor P1 operates in the linear region. The transistors are sized so that the frequency at $V_{SRC} = 390mV$ is $50kHz$. The ring oscillator operates at subthreshold voltages and can be operated down to $120mV$. It consumes $5nA$ at $500mV$. The power doesn't increase significantly when the transistors are resized to operate at a slightly higher frequency. It is worth noting here that the clock frequency can be tuned to a wide range of frequencies, limited

only by the operating frequency of the level shifter that can operate reliably up to $100kHz$.

B. Subthreshold Level Shifter

The level shifter converts the voltages between the subthreshold to above threshold (V_{DD}) voltages is adopted from [8]. With no additional circuitry associated, the level shifter is an ideal component for the ultra low power operation. The diodes (D1 and D2) are connected to the cross coupled PMOS transistors (P1 and P2) as shown in Fig 5 where the pull up ability of the PMOS transistors adapts with the input logic voltage. The $V_{GS} (= V_{PD})$ of the diode is very small and in steady state the PMOS pull up diodes are either in ON or OFF state. When the input switches from 0 to 1, the $V_{GS} (= V_{PD})$ of PMOS diode D1 will not change quickly as it operates in the subthreshold region. However, the input logic '1' will weakly turn on NMOS N1. Due to the weak pull up of D1, the current of N1 pulls down node X and the transistor P2 is turned on. This activates the feedback circuit and ensures correct operation for subthreshold voltages.

As seen from the Fig 6a, the level conversion occurs from subthreshold voltages from as low as $330mV$ converting the input signal to a higher voltage level available as $V_{DD} @ 500mV$. The circuit consumes $422pA$ while operating at $500mV$.

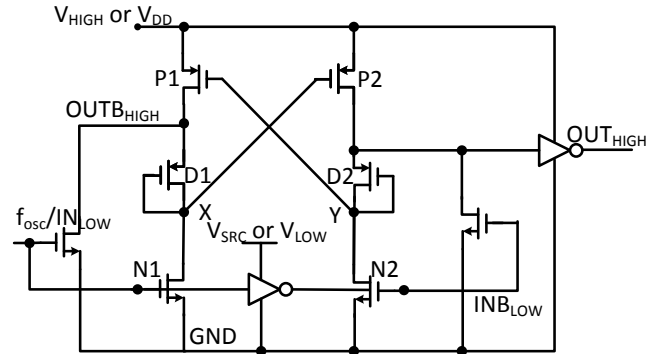


Fig. 5: Level Shifter Circuit

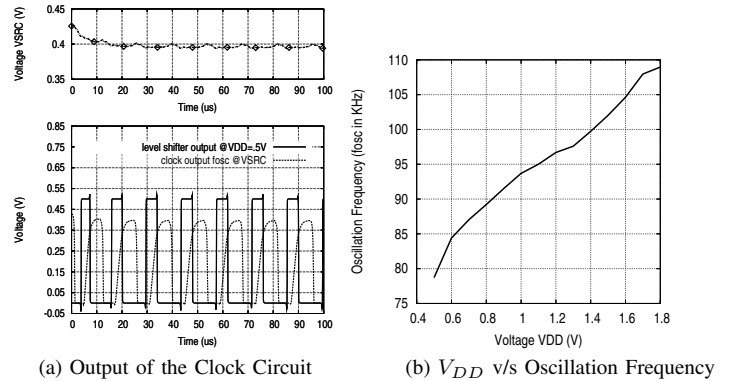


Fig. 6: (a) Output of the Clock Circuit and (b) V_{DD} v/s Oscillation Frequency

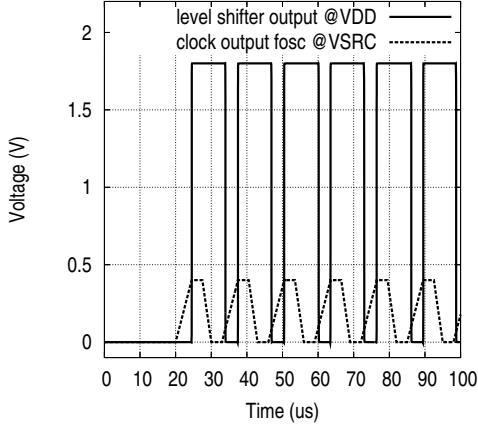


Fig. 7: Output of the Clock Circuit from Level Shifter Stage

The circuit simulations are carried out using CMOS $0.18\mu\text{m}$ BSIM4 physical models. From the simulation results as shown in Fig 6a and Fig 7, the low power clock is capable of operating from subthreshold voltages to maximum voltages. For example, when the V_{DD} reaches 500mV , the V_{SRC} is 390mV . In this case, the oscillator rail to rail swing is 390mV . However in the subsequent stages the level shifter will convert this voltage to 500mV as shown in Fig 6a. For the full range, the clock oscillation amplitude as low as 330mV can be level converted to 1.8V , shown in Fig 7. Several circuit simulations were performed and it was found that the clock circuit consumes 6nA at 500mV and 13nA at 1.8V . This translates to 3nW and 24nW at these voltages which confirms the ultra low voltage consumption of the proposed clock circuit.

V. VOLTAGE MONITOR

The block diagram of the voltage monitor consisting of two window comparators and a D flip flop is shown in Fig 8. The ideal response of the voltage monitor is shown in Fig 9. The operation of the voltage monitor is as follows. As the voltage ramps up in the storage capacitors, both window comparators will respond at a given voltage threshold. *e.g.*, the comparator 1 is designed with a proportional voltage circuit at $V_{0.15DD}$ (15% of V_{DD}) that sets to 1 the output of the D flip flop when V_{DD} is above 1750mV . The second comparator 2 will reset the D flip flop output when V_{DD} at the storage capacitors C_2 becomes lower than 1450mV (in between 1450mV and 1750mV , it is ensured that the energy is sufficient to provide power to the PMU circuits). Therefore, if the level of the storage capacitor is below the stop threshold voltage of 1450mV , the voltage monitor disconnects the rest of the circuit by disabling the switch P_1 .

A. Window Comparator

As shown in the Fig 10, the transistor level schematic of the window comparator consists of V_{ref} , proportional voltage generator $V_{0.xDD}$ and a comparator with an ultra low power

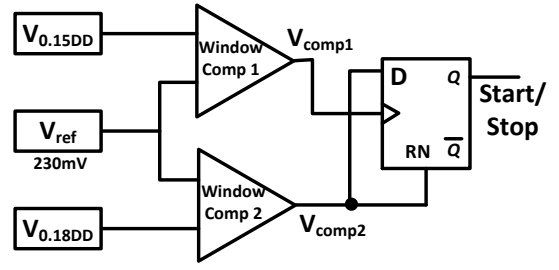


Fig. 8: Block Diagram of the Voltage Monitor

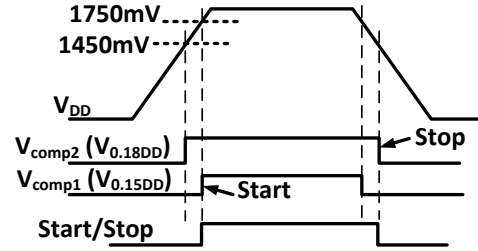


Fig. 9: Voltage Monitor Start Stop (ideal response)

inverter and is similar to the design in [6]. As the energy harvester charges the capacitor C_1 and C_2 the V_{DD} rises. This voltage generates two voltages: V_{ref} and $V_{0.xDD}$, a proportional voltage of V_{DD} . While V_{DD} rises, the V_{ref} saturates to 230mV at 500mV (Fig 12) while $V_{0.xDD}$ varies proportionally to V_{DD} as shown in top plot of Fig 11. As the proportional voltage ($V_{0.2DD}$) goes higher than V_{ref} , the comparator output V_{comp} is high (Fig 11). The final output is provided from the two diode connected current starved inverter that limits the short circuit current that consumes very low power.

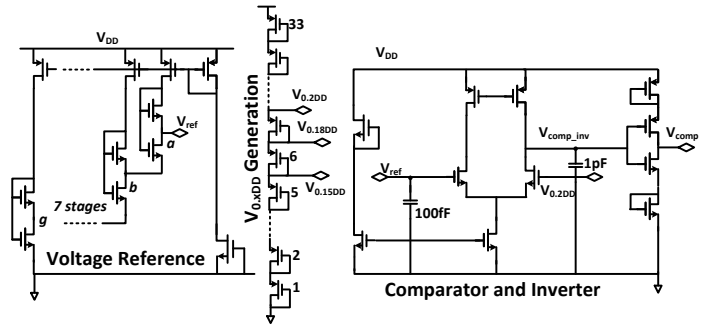


Fig. 10: Window Comparator Schematic

As shown in Fig 12, the voltage reference [10] within the voltage comparator, consists of elementary Proportional-To-Absolute-Temperature (PTAT) voltage source to bias the amplifier. The two transistors (stacked NMOS) act as elementary PTAT source that operate in the weak inversion. The current supplied to each cell goes through the bottom transistors of the subsequent cell. Also, the DC biasing voltage source is

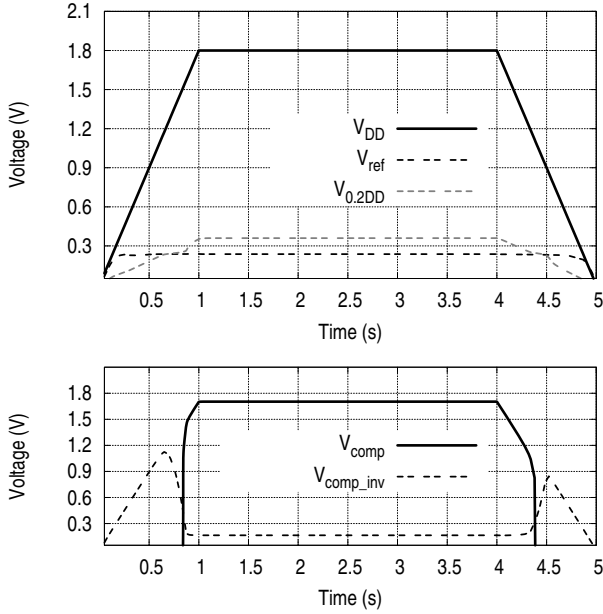


Fig. 11: Voltage Comparator Output

removed as the current source is biased in the subthreshold region that results in ultra low power consumption for the circuit. The current consumption is negligible for the V_{ref} at $13pA$ at $500mV$.

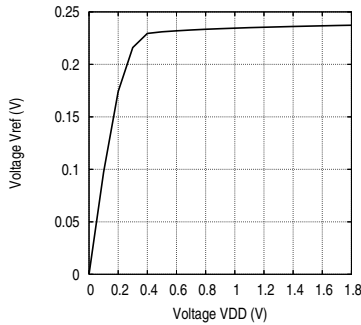


Fig. 12: DC response of the V_{ref} Circuit

The 33 identical stacked diode connected PMOS transistors generate a proportional voltage (marked $V_{0.xDD}$ in Fig 10). The transistors are sized so that the energy consumption is minimal. Out of the 33 transistors, the taps are taken at 5^{th} , 6^{th} and 7^{th} transistors from the bottom of the stack to obtain $V_{0.15DD}$, $V_{0.18DD}$ and $V_{0.2DD}$ respectively. Both the V_{ref} and the proportional voltage generator is fed to the single stage opamp comparator. The postlayout simulation results in Fig 13 show the ‘START’ enabled when “ V_{comp1} ” goes high and disabled when “ V_{comp2} ” goes low. The output response is recorded in seconds and is not an issue because the charging time of the capacitors by harvesters is also of the same order. The current consumption of the voltage monitor is $4nA$ at $1.8V$.

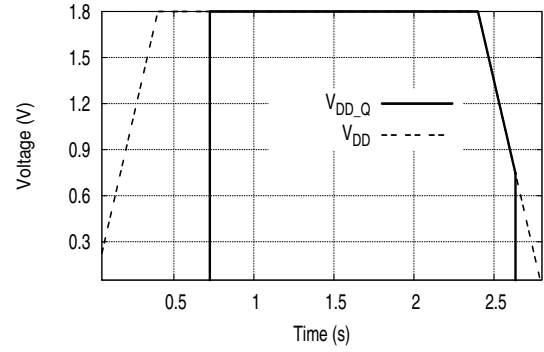


Fig. 13: Voltage Monitor Start Stop (simulated)

VI. DIGITAL CIRCUIT OPERATION AND RESULTS

The digital circuit generates the control sequences based on the timers for reading and transmitting sensor data. When the switch P_1 is disabled (Fig 1), the circuit doesn’t start during which time the storage capacitor is charged. At start up, when P_1 is enabled, the operation of the digital control can be described as a state flow as following.

- **state 1** When the V_{DD} is $1.8V$, Start is enabled \rightarrow go to state 2;
- **state 2** Every $6secs$ log the sensor data into the register array \rightarrow go to state 3;
- **state 3** Log data from sensor interface \rightarrow go to state 2 until 16 bits have been logged \rightarrow go to state 4;
- **state 4** Enable UWB (en_UWB) and wait for $600\mu s$ \rightarrow go to state 5;
- **state 5** Send the symbols(10 pulses) every positive edge of the μs clock \rightarrow go to state 6;
- **state 6** Check if the Start is still enabled \rightarrow go to state 1 else \rightarrow wait for the capacitors to charge while staying on state 6;

As shown in Fig 14, the UWB transmitter is enabled before the actual data transmission ($600\mu s$). This is done to meet the setup and timing requirements of the wake up circuits within the UWB block [11]. The control sequence is generated to optimize power consumption of the sensor node, as the power consumption of the UWB transmitter during the sleep and active period is $80\mu A$ and $25mA$ respectively. After the setup period, every positive edge of the μs clock (driven from the ULP clock), the $100ns$ clock block generates trigger pulses set apart at $100ns$ as shown in the Fig 14.

As can be seen in the bottom plot of the simulation in the Fig 14, the 10 trigger pulses (as UWB_nosym) is used to encode the 4 bit sensor data from the sensor interface (sensor implemented as a DIP switch) as 10 bit symbols. Each of these symbol consists of first two bits as ‘1’ and the rest 8 bits different for every symbol. The trigger to UWB transmitter signal “trig2UWB” is derived from the digital block using the trigger pulses. For example, the ‘UWB_nosym’ are simple

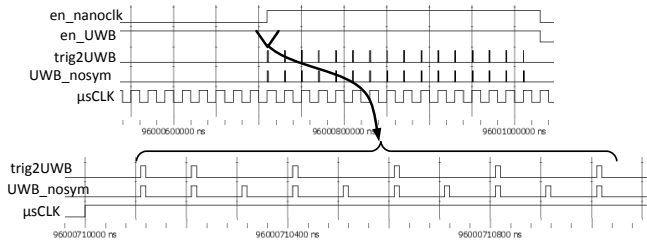


Fig. 14: Timing Simulation

trigger pulses (“111111111”), while the ‘trig2UWB’ is coded as “1101010101”. Where the first two bits are always ‘1’ that is used for receiver synchronization while the rest are the data bits. The 16 symbols (top plot of Fig 14) comprises of the 16 sensor data that is sent in each of the positive edge of the 20 $\mu sclk$. It was found out from simulation that the storage capacitor C_1 with $50\mu F$ is sufficient to provide the necessary energy for transmitting 16 symbols or 160 pulses.

As the total power consumption of the PMU is the sum of power consumption of voltage monitor, digital circuit, ULP clock and switches, the leakage flow of the power switches P_1 and P_2 is also important. Furthermore, the power switches P_1 and P_2 should supply enough current to digital circuit and ULP Clock ($213nA$) and UWB transmitter ($25mA$). Therefore there is a lower limit of the width of these MOS transistors. We evaluated both NMOS and PMOS transistor supplying a higher drive current $1\mu A$ and $40mA$ for the digital circuit and the UWB transmitter respectively with $|V_{ds}|$ set at $50mV$. From simulation, it was found that PMOS switch has a lower gate width and lower leakage current requirement than the NMOS switch. From the simulation we also observed that, P_1 leakage was negligible. However due to a higher drive current to the UWB transmitter, the width of the power switch P_2 was $1mm$ and the leakage current was $17nA$.

The floorplan of the complete circuit implemented in CMOS $0.18\mu m$ technology is given in Fig 15. The size of the circuit is $1.5mm \times 1.5mm$.

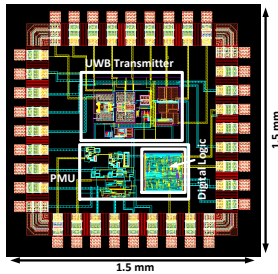


Fig. 15: Floorplan of the PMU ASIC

Table I shows the power consumption of the individual blocks of the PMU that have been presented above. The PMU consumes a total of $364nA$ at $1.8V$. A comparison of the state of the art publications is shown in Table II and shows that our proposed PMU has the lowest current (power) consumption of $364nA$ ($655nW$).

Block	Current	Voltage
LDO	$130nA/215nA$	$2.2V/3.0V$
Voltage Monitor	$4nA$	$1.8V$
Digital Circuit	$200nA$	$1.8V$
ULP Clock	$13nA/6nA$	$1.8V/500mV$
P_2	$17nA$	$1.8V$
Total	$364nA$	$1.8V$

TABLE I: Current Consumption of Different Blocks of PMU

PMU	This Work	[2]	[3]	[4]
Total	$364nA$	$1.1\mu A$	$1.4\mu A$	$70\mu A$

TABLE II: This Work Compared to Reference Publication

VII. CONCLUSION

A sub μA power management circuit implemented in $0.18\mu m$ CMOS is presented that focussed on minimizing the leakage current of the LDO, voltage monitor and power switches thereby reducing the overall power consumption of the circuit. The postlayout simulated results of the power management circuit describe the operation with sub μA current consumption. We conclude that as long as the power harvested from the harvester exceeds the power consumed by the PMU (*i.e.* $655nW$), the sensor node would operate autonomously.

ACKNOWLEDGMENT

The authors thank the NCCR-MICS Swiss National Science Foundation (SNSF) for the research support. We thank Steve Tanner for his support on SoC Encounter.

REFERENCES

- [1] B.H.Calhoun *et al.*, “Body Sensor Networks: A Holistic Approach From Silicon to Users,” *Proc. of the IEEE*, v. 100, no.1, pp.91-106, Jan. 2012
- [2] E.J.Carlson, K.Strunz, B.P.Otis, “A 20 mV Input Boost Converter With Efficient Digital Control for Thermoelectric Energy Harvesting,” *Solid-State Circuits, IEEE Journal of*, vol. 45, no.4, pp.741-750, April 2010
- [3] I. Doms *et al.*, “Capacitive Power Management Circuit for Micropower Thermoelectric Generators With a $1.4 \mu A$ Controller,” *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 10, pp. 2824–2833, 2009
- [4] H.Lhermet *et al.*, “Efficient Power Management Circuit: Thermal Energy Harvesting to Above-IC Microbattery Energy Storage,” *Solid-State Circuits Conf., Digest of Tech Papers. IEEE*, pp.62-587, 11-15 Feb. 2007
- [5] Q.Yifeng *et al.*, “ $5\mu W$ -to- $10mW$ input power range inductive boost converter for indoor photovoltaic energy harvesting with integrated maximum power point tracking algorithm,” *Solid-State Circuits Conf., Digest of Tech Papers. IEEE*, pp.118-120, 20-24 Feb. 2011
- [6] C. De Roover, M.Steyaert., “Energy Supply and ULP Detection Circuits for an RFID Localization System in 130 nm CMOS,” *Solid-State Circuits, IEEE Journal of*, vol.45, no.7, pp.1273-1285, July 2010
- [7] T.T. Le, “Efficient Power Conversion Interface Circuits for Energy Harvesting Applications,” *PhD Thesis, Oregon State University*, 2008
- [8] H. Shao and C.Y. Tsui, “A robust, input voltage adaptive and low energy consumption level converter for sub-threshold logic,” *Solid State Circuits Conference, ESSCIRC 2007. 33rd European*, pp. 312 – 315, Sep. 2007
- [9] U. Denier, “Analysis and Design of an Ultralow-Power CMOS Relaxation Oscillator,” *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 57, no. 8, pp. 1973-1982, Aug. 2010
- [10] E. Vittoz and O. Neyroud, “A Low-Voltage CMOS Bandgap Reference,” *Solid-State Circuits, IEEE Journal of*, SC-14, no. 3, pp. 573–577, 1979
- [11] C.Robert *et al.*, “Low power ASIC transmitter for UWB-IR radio communication and positioning,” *Indoor Positioning and Indoor Navigation (IPIN), 2010 Int Conf. on*, pp.1-7, 15-17 Sept. 2010