SoC Low-Power Practices for Wireless Applications

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***Abstract*— this paper describes current practices regarding low power SoC aimed at wireless applications.**

Keywords- microprocessor, wireless application, gate-level models, DVFS, AVS, voltage stack, power management, low-power

I. INTRODUCTION

ST-Ericsson has developed several SOC for smart-phone applications combining high performance and ultra-low power consumption. Most recent FD-SOI chips have been praised by experts. Results and trends will be provided in this panel.

The three pillars of SOC low-power architecture are Dynamic Voltage and Frequency Scaling (DVFS), Adaptive Voltage Scaling (AVS) and the art of controlling DVFS and AVS.

II. LOW-POWER ARCHITECTURE: DVFS

DVFS is implemented by combining various techniques covering clock distribution, voltage domains and power islands, and several voltage operating points (OPP).

A. Clock Distribution

FD-SOI technology provides actual processing capability down to extremely low voltage levels. The SOC takes advantage of this to enable a wide range of use cases from ultra-low power up to compute intensive use cases involving CPU and multi-media accelerators.

Good clocking distribution relies on the right compromise in selecting the frequency generators and sources. This is made possible by low-power, flexible, clock generators capable of dynamically switching from one clock source to another

Clock distribution also consists in implementing intensive clock gating throughout the design. This goes beyond the use of clock gating of commercial logic synthesizers. Modern GALS architectures bring the flexibility to switch on only the clocks of the active IPs or parts thereof. Automated clock gating is also implemented by means of local state machines detecting the lack of activity in parts of the design.

B. Voltage Domains and Power Islands

The distribution of voltage domains throughout a complex SOC involves combining constraints from system level (power management supply device), memory technology, analog component supply needs, and finally the digital logic technology.

Each voltage domain is further divided into few power islands thereby providing extra power saving granularity. Such islands can be around the CPU cores, multimedia IPs, high speed links, memory controllers, etc.

C. Power & Clock Management

Controlling clock activation, frequency selection, power islands and voltage levels lies at the heart of low-power architecture. For instance switching a power island on or off requires proper settings of isolation cells, switch controls for the logic, memories, etc.

III. AVS

Adaptive Voltage Scaling (AVS) also called process compensation is a technique for managing performance variations due to process dispersion, and for reducing the power consumption. Generally speaking, AVS will define optimal power supply level at a given performance [1] [2].

In this panel we will present performance and power improvements obtained by means of our unique AVS methodology. It has been applied successfully on 45 nm bulk products and is now developed for our most recent 28 nm FD-SOI technology.

IV. CONCLUSIONS

ST-Ericsson has demonstrated several products implementing extensive DVFS and AVS techniques. These drastically improve performance and power consumption for smart-phone applications.

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