Ultra-Wide Voltage Range Designs in Fully-Depleted Silicon-On-Insulator FETs

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Abstract **— Todays' MPSoC applications are requiring a convergence between very high speed and ultra low power. Ultra Wide Voltage Range (UWVR) capability appears as a solution for high energy efficiency with the objective to improve the speed at very low voltage and decrease the power at high speed. Using Fully Depleted Silicon-On-Insulator (FDSOI) devices significantly improves the trade-off between leakage, variability and speed even at low-voltage. A full design framework is presented for UWVR operation using FDSOI Ultra Thin Body and Box technology considering power management, multi-VT enablement, standard cells design and SRAM bitcells. Technology performances are demonstrated on a ARM A9 critical path showing a speed increase from 40% to 200% without added energy cost. In opposite, when performance is not required, FDSOI enables to reduce leakage power up to 10X using Reverse Body Biasing.**

Keywords—energy efficiency, low voltage, adaptive architectures, FDSOI, Ultra Thin Body and Box

I. INTRODUCTION

With the increasing complexity of today's MPSoC applications, extremely high performance has become the main requirement. However, high performances do not only mean high speed but also low power. For example, in wireless internet devices, very high speed is mandatory for games or video computing while it is necessary to save dynamic and static power for low speed applications in order to improve the battery life. The convergence between high speed and low power is very difficult to reach. Most of the time, ultra low power architectures cannot reach high speed and conversely, at high speed, a lot of power is consumed.

Using energy efficient architectures is the only way to achieve a good compromise between speed and power. For each functional point, the architecture should be able to find an optimum energetic state while considering applicative constraints. The emerging solution is to use Adaptive Voltage and Frequency Scaling (AVFS) architectures [1]. Compared to a worst case DVFS approach, an adaptive architecture is able to dynamically adapt its optimum functional point to the real Process-Voltage-Temperature (PVT) case [2] The objective is to save power at same speed or to increase the speed for an equivalent power budget.

Clearly, the more we reduce the voltage supply, the more the energy decreases. The minimum energy point is found at low voltage as described in [3] and even near threshold voltage. Those last two years, we can find lots of works dealing either with high speed or very low voltage. Considering DSP design, [4] is the best figure found in the literature in 22nm technology reaching 3 MHz at 280 mV. On the other hand, lots of work are proposing very high speed DSPs up to 1,8 GHz but to the detriment of power [5]. In the middle range, low power DSPs are described in [6] with an energy of 120µW/MHz but those works are not compliant with very high speed constraints. To improve energy efficiency while respecting widespread speed constraints, an Ultra Wide Voltage Range (UWVR) operation is needed [4]. Moreover, the need to increase the speed at low voltage while maintaining very high speed at nominal voltage is still a key issue for the convergence between very high speed and ultra low power.

Designing such UWVR systems at the nanometer regime introduces many challenges due to the emphasis of parasitic phenomenon effects driven by the scaling of bulk MOSFETs, making circuits more sensitive to the manufacturing process fluctuations and less energy efficient. How to improve the trade-off between leakage, variability and speed at low-voltage? Obviously the trend is to use thin film devices. Intel has proposed FinFET vertical structures [7] and STMicroelectronics is developing fully depleted silicon-on-insulator (FDSOI) devices. Undoped thin-film planar FDSOI devices are being investigated as an alternative to bulk devices in 28nm node and beyond, thanks to its excellent short-channel electrostatic control, low leakage currents and immunity to random dopant fluctuation. This compelling technology appears to meet the needs of nomadic devices, combining high performance and low power consumption. A major challenge for this technology is to provide various device threshold voltages (V_T), trading off power consumption and speed.

The work presented in this paper has contributed to the development of an UWVR multi-V_T design platform in FDSOI planar technology on Ultra Thin Body and Box (UTBB) for the 28nm and below technology nodes. In this framework, the key elements of the UWVR design platform have been studied. Based on this analysis, UWVR standard cells libraries and SRAM bitcells have been developed. The use of an efficient Body Biasing (BB) will allow a better performance tuning for high energy efficiency. Finally, the technology performances have been evaluated on a critical path extracted from the ARM Cortex A9 processor.

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II. FDSOI ULTRA THIN BODY AND BOX TECHNOLOGY

UTBB FDSOI is a high-k metal gate planar technology (Figure 1). The source and drain are raised to reduce the access resistances There is no channel doping nor pocket implant making the process simpler as bulk. The Box thickness is 25nm leading to a good trade-off between Drain/Source-to-Substrate parasitic capacitance and body factor. A back plane, either n-type or p-type, is implemented underneath the Box to improve the Short Channel Effect (SCE) and adjust V_T. Back bias or Hybrid/Bulk technology is feasible after removing the Box and finally, Shallow Trench Isolation (STI) are used to electrically isolate the devices.

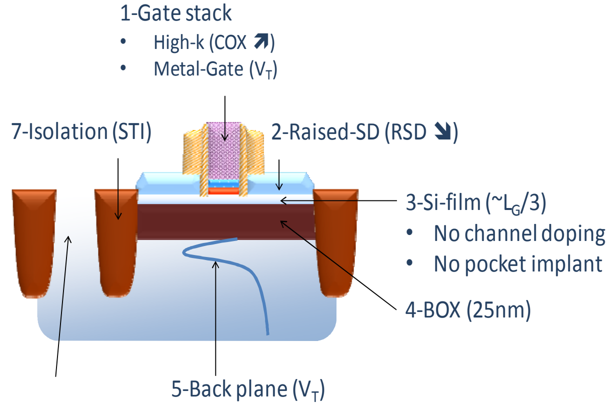


Figure 1 - Cross section of a UTBB-FDSOI transistor

A. *Ultra-thin Buried Oxide*

In Fully-Depleted SOI technology, the silicon film, where the active area of the transistor is located, is thinned down to approximately one third of the minimum gate length value [8]. This is done in order to have a good electrostatic control of the channel, i.e., a low Drain Induced Barrier Lowering (DIBL) value [9], by cutting the deep field lines originating from the drain. In a 28nm UTBB FDSOI node, the silicon film thickness T_{SI} is approximately 8-9nm.

For UTBB FDSOI technology, the choice was made to use a thin Box and this brings a number of advantages: first, it creates a Back-interface, which can be thought of as a back-gate, whose polarization value modifies the threshold voltage (V_T) of the transistors. The Body Factor, representing the V_T sensitivity to the back-gate voltage, is equal to 85mV/V for a 25nm Box. Given that the back-gate voltage also called Back Bias (BB) can vary over a 2V amplitude, the V_T value can be greatly modified dynamically, enabling circuit designers to define several Operating Points. The second advantage of this thin Box is that, combined with an n- or p-type backplane (a doped area beneath the Box), it can bring transistors with two different V_T values, for the same gate stack. It means that the technology offers different ways to modulate the threshold voltage first by providing a multi-V_T platform and secondly by enabling an efficient Body Biasing at circuit level. This innovative UTBB FDSOI mutli-V_T composition is detailed in Section II.

B. *Immunity to Short channel Effects and Variability*

The combination of UTBB and back-plane greatly reduces the DIBL compared to Bulk, as shown in Figure 2, acting as an electrostatic booster.

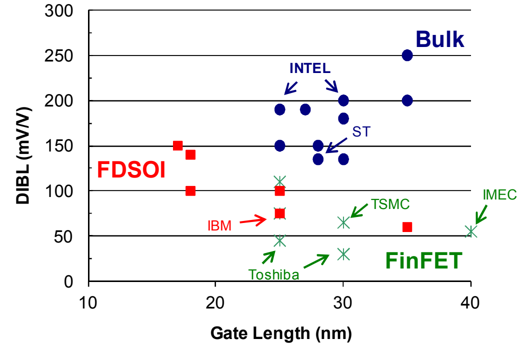


Figure 2 - Measured DIBL values as function of the gate length. Comparison with corresponding Bulk and FinFet

FDSOI transistors have undoped channels, in order to remove the major source of variability in current deep submicron technology, namely the Random Dopant Fluctuation [10]. It has to be noted that the backplane is doped, as said above, but this has no impact on variability. The consequence of using undoped silicon films is record low variability, as shown in Figure 3.

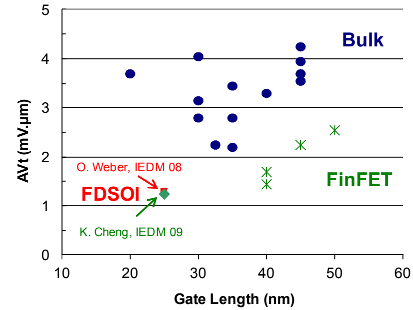


Figure 3 - FDSOI Variability benchmarking with other technologies

III. DESIGN CONSIDERATIONS FOR UWVR

In this section, we focus on the development of an Ultra Wide Voltage Range multi-V_T design platform using the technology described before. The key elements of the UWVR design platform are based on a multi-V_T management at device and circuit levels, specific and optimized UWVR standard cells libraries and SRAM bitcells.

A. *Power/Speed Management and UWVR Capabilities*

1) *Multi-V_T*

UTBB FDSOI technology enables multi-V_T devices as well as fine V_T adjustment thanks to various knobs from both process and design all illustrated in Table I. Among them, well known knobs that have already been used in bulk technology are gate stacks, gate trimming and channel counter doping.

This technology proposes an inherent multi-V_T platform with various knobs either at technological or design levels. It allows the users to find statically or dynamically the best tradeoff between speed and power.

TABLE I. VT TUNING KNOBS

from process	advantages/drawbacks
Gate stack (bulk-like)	+ 2 possible V_T by choosing a n-type or p-type gate stack - Increase complexity and cost when more than 2 gate stacks
Gate trimming (bulk-like)	+ Reduce gate capacitance when the active area decrease - No V_T modulation on long channel devices
Si-film counter doping (bulk-like)	+ Finely tune the V_T - Degrade variability and mobility
Back plane type (FDSOI-specific)	+ 2 possible V_T by choosing a n-type or p-type doping + No impact on variability and mobility
from design	
Back biasing (bulk-like but exacerbated in FDSOI)	+ V_T modification in static (fixed BB voltage) or dynamic (dedicated BB generator or switch between two BB voltages)

The V_T of UTBB FDSOI devices can be described by the following equation:

$$V_{Tsat} = V_{T0} + r(V_{B0} - V_B) - SCE - DIBL \quad (1)$$

with V_{T0}, the part of V_T due to the front face, r, the body factor, V_{B0}, the part of V_T due to the back face, V_B, the back biasing voltage, SCE, the short channel effect, and DIBL, the additional SCE in saturation mode.

The gate stack and the Si-film counter doping (front face) affect V_{T0}, while the gate trimming affects SCE and DIBL (V_T roll-off effect). The specific FDSOI knob (back face) is defined by V_{B0}, which mainly depends on the Back Plane work function (from 4.1eV to 5.1eV).

2) Body Biasing Techniques

The body factor in FDSOI technology can be described as the capacitance ratio between back and front face with the channel position, $X_{channel}$, when $V_{GS}=V_T$ [11]:

$$r = \frac{T_{OX} + \frac{\varepsilon_{SiO2}}{\varepsilon_{Si}} X_{channel}}{T_{BOX} + \frac{\varepsilon_{SiO2}}{\varepsilon_{Si}} \left(T_{Si} - X_{channel} - T_{dep}\right)} \quad (2)$$

With T_{BOX}>20nm, the BP depletion (T_{dep}) can be neglected. Therefore, only T_{OX}, T_{BOX}, T_{Si} and $X_{channel}$ parameters define the body factor. In the 28nm UTBB-FDSOI technology platform of STMicroelectronics, T_{Si}=7nm, T_{BOX}=25nm, T_{OX}(n)=1.35nm T_{OX}(p)=1.5nm and X_{bar} is about 1 or 2nm. In this way, the body factor for both nMOS and pMOS achieves more than 85mV/V [12], which is equivalent to bulk technology. Nevertheless, the body factor in UTBB FDSOI technology does not degrade with the scaling. It can be maintained or increased by the reduction of Box thickness at each technology node.

To bias, statically or dynamically, the Back Plane through the Wells, existing supply voltages (V_{DD}, GND) can be used. Back bias (BB) generators can also be used to finely tune the V_T (process compensation, negative voltages). V_T can be reduced or increased by applying forward back bias (FBB) or reverse back bias (RBB), respectively, as shown in Figure 4. It is thus possible to boost the speed or decrease the leakage.

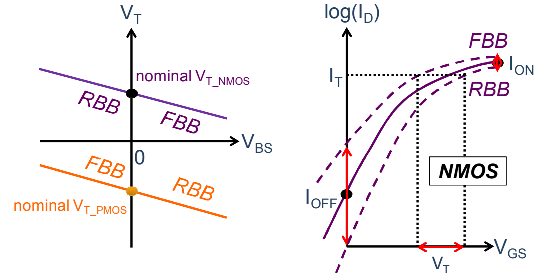


Figure 4 - Forward and Reverse Back Bias (FBB & RBB)

To avoid forward biasing of the p-Well/n-Well junctions, a specific BB range is defined for RVT and LVT standard cells, as presented in section II. Another solution to overcome this issue could be to use single well standard cells as detailed below.

3) Single Well Methodology

In addition to the dual n-Well/p-Well configurations, a Single Well (SW) architecture (Figure 5) can achieve an intermediate V_T level and this solution is unique and specific to UTBB FDSOI and easy to achieve at process level.

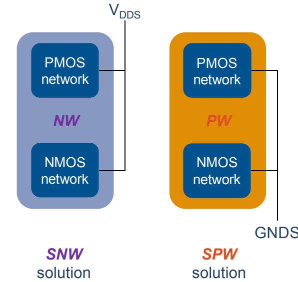


Figure 5 - Single N-Well (SNW) and single P-Well (SPW) configurations

[13] shows that Single Well design solution leads to an energy efficiency as high as LVT for a higher V_{DD}. With lower static power and higher dynamic power consumption, SW is a very attractive candidate for MPSoC applications where body biasing is not required or difficult to apply dynamically.

B. UWVR Library Cells

To optimize the standard cells for energy efficiency, various configurations of V_T flavor and symmetric or asymmetric Poly-Biasing values were compared using the critical path methodology developed in [14] in terms of Power-Delay-Product (PDP), leakage current, delay, and variability. A pareto-effiency metric [15] was used to find the optimal configurations for each criterion (Figure 6). The

couples of V_T flavors and Poly-Biasing values that induce high leakage current or delay lead to non-optimality and thus are discarded from the selection. Regarding the redundant configurations, the selection is made using the variability criterion, which means favoring LVT and high poly-biasing values. A set of 5 winning configurations were defined, and applied to a selection of 60 combinational cells, resulting in a complete offer of more than 300 standard cells.

A specific effort was made regarding critical cells. The clock tree cells were designed using LVT flavor, 10nm Poly-Biasing and multi-finger gates, offering both reduction of the variability and increased speed and slope quality of the clock signal. The flip-flops were checked functional using 6σ Monte-Carlo simulations across the ultra-wide voltage range. The input level shifter library is composed of common input and enable cells where the β-ratio was balanced through over-sizing to compensate the low voltage PMOS versus nominal voltage NMOS current, offering acceptable fall versus rise transition balance across the ultra-wide voltage range. The output level shifter is a single supply two-stage design than enables CMOS low-to high swing conversion in the 0.3V to 1.4V range using a MOS diode for voltage lowering.

The complete offer was characterized at ultra-low voltage centered corners in addition to industrial nominal corners.

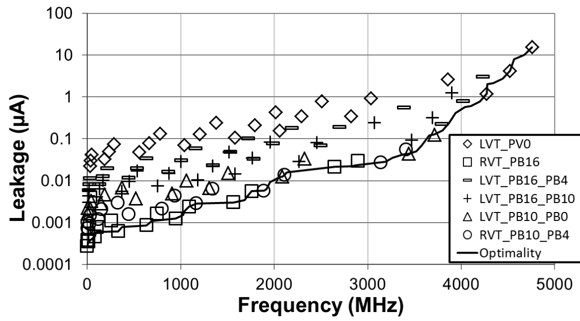
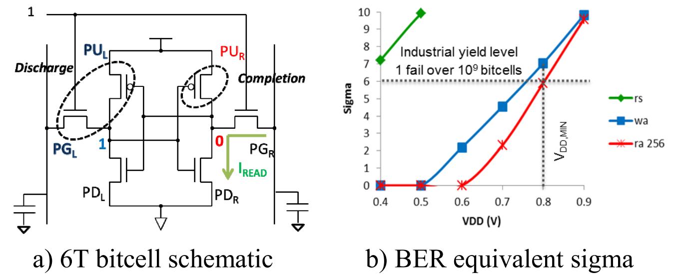


Figure 6 - UWVR Pareto-Efficiency of V_T and Poly-biasing combinations, leakage criterion

C. UWVR SRAM Bitcells

In UWVR framework, embedded SRAM circuits have to remain compatible with the system operating voltage conditions. However, SRAM design is facing severe challenge in maintaining sufficient bitcell Read-Ability (RA), Write-Ability (WA) and Read-Stability (RS) margins under relentless area scaling. One trend for these issues is to use an SRAM supply voltage regulator to keep the SRAM supply voltage higher than the circuit minimum supply voltage [16]. Low voltage solutions abandon 6T bitcell to bypass the write-ability read-stability contention or read fails caused by a lack of bitcell read current [17]. However, most of the 6T alternatives lead to an area overhead. It requires single-ended sensing instead of differential sensing and do not solve the interleave bitcell column issue. Over the memory circuit periphery, assist techniques, such as wordline boost, negative bitlines, V_{DD} droop and GND boost [18] are employed to expand the operating margins. The effectiveness of these techniques is related to the transistors σV_T, leading to more or less area and energy overhead. Sophisticated timing sequence controls have also been proposed, such as write-back scheme. During a write operation, read data are written back to the half selected bitcells. It is useful to solve the read modify write soft failures, but can increases the memory latency.

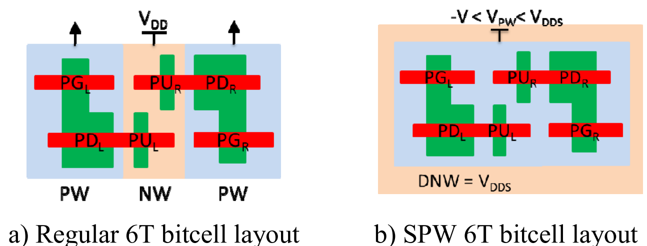
SRAM yield is mainly affected by soft failures that can be classified into three categories: failures in maintaining data stability (read-stability), failures in the bitcell read current to generate a target bitline differential voltage in the given access time (read-ability) and failures in the time to flip the content of the bitcell (write-ability). SRAM characterization based on dynamic margins, obtained through transient simulations; show that the minimum supply voltage usable is limited by Write-Ability and Read-Ability and not Read-Stability, as it is expected by regular static margins which consider an infinite access time (Figure 7). Read-ability cause of failure relies on the bitline load capacitance and the nMOS pass-gate (PG) and pull-down (PD) transistor strength (I_{READ}). Failures involved in write-ability depends on the bitcell ability to discharge the high logic level node, while guarantying the pull-up completion of the low logic level node (0V) towards a high level (V_{DD}) (Figure 7a). At fast clock frequency the pMOS pull-up (PU) completion becomes the first limiter.



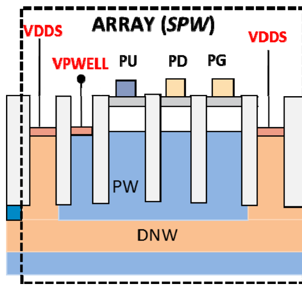
a) 6T bitcell schematic b) BER equivalent sigma

Figure 7 - a) 6T bitcell failures and b) BER equivalent sigma vs. VDD for RS, RA and WA (TT, 27°C, 2GHZ@1V, 256 bitcell/column)

To strengthen the PU, a single p-well (SPW) bitcell architecture was proposed in [19] (Figure 8). Both PMOS and NMOS transistors are placed over a common pWell, lowering the threshold voltage of the pMOS transistors, with no channel doping. Besides, RA is improved by forward biasing (V_{PW}>0V) the nMOS transistors. The PW is isolated from the p-substrate (PSUB) by using a deep n-well (DNW) tied to V_{DDS} (Figure 8).



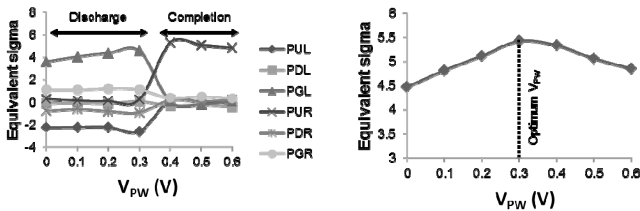
a) Regular 6T bitcell layout b) SPW 6T bitcell layout



c) Cross sectional view: SPW array

Figure 8 - SPW SRAM

Optimal V_{PW} voltage is trading-off by read-ability and write-ability. Varying V_{PW} leads to a dual effect on the impact of the discharge and completion mechanisms involved in write failures. Increasing V_{PW} reinforces the nMOS transistors at the expense of the pMOS transistor drivability. Maximum write-ability is reached when the bitcell becomes as sensitive to the discharge mechanism as the completion one. Figure 9 shows the write-ability yield variation versus V_{PW} for the bitcell studied in [19] at 0.6V. A maximum is reached when V_{PW} is roughly $V_{DD}/2$. At V_{DD} the yield is slightly higher than at 0V and the mechanism involves in failures became the completion. The good yield balance between 0V and V_{DD} makes the bitcell write-ability insensitive to V_{PW}, therefore bypassing the write-ability read-ability contention.



a) Transistor strength b) WA BER equivalent sigma

Figure 9 - Relative transistor strength impacting the WA BER vs. VPW (0.6V, TT, 27°C)

To boost the read-ability, this approach can be efficiently extended to the 8T bitcell. The 6T core dedicated for write-ability and read-stability is SPW, while the read-port is NW to boost the bitcell read current (Figure 10). The NW can be adjusted from 0 to V_{DD} to manage the performances and the static power consumption.

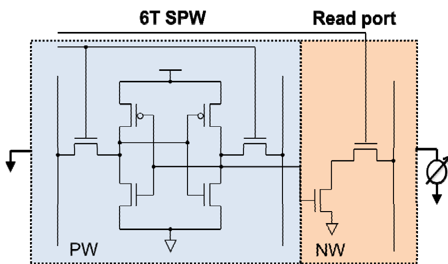


Figure 10 - SPW-NW 8T bitcell

IV. Circuit Level Benchmarking & Silicon Results

To assess how the improved transistor characteristics translate at circuit level, several representative IP blocks, including an ARM Cortex-A9 CPU core were benchmarked using eldo electrical simulations with silicon extracted models. The following benchmarks compare the figure of merits at the 28nm node of planar FD technology ("28FD") with a state-of-the-art low-power technology ("28LP") and a more performance-oriented, general purpose technology ("28G").

A. PPA: FDSOI vs. BULK LP and G Technologies

Figure 11 shows the competitive speed/leakage trade-off of planar FD vs. conventional bulk CMOS technologies at nominal voltage (0.85V for the G-type technology, 1V for 28FD and LP-type technology). For comparable leakage power, 28FD consistently outperforms both 28LP and 28G. In addition, applying forward back-bias (FBB) to the planar FD technology enables further pushing the performance, obviously at the expense of increased leakage, but without degrading the performance/leakage ratio (making this a possible solution for boosting the performance during short bursts). Moreover, with 200mV V_{DD} underdrive, the 28FD may yield the same speed performance as 28LP with a reduced leakage.

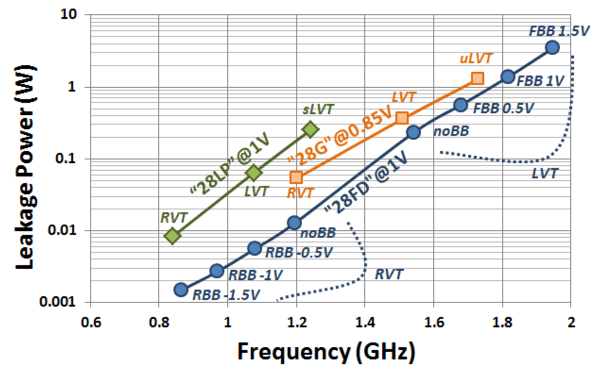


Figure 11 - Best operating frequency for any class of leakage (worst-case process corner)

B. Best Power Efficiency Across Use Cases

Besides getting the best possible performance for a selected class of leakage, it is important to have access to the best possible total power consumption (dynamic power plus leakage power) across a wide range of operating frequencies.

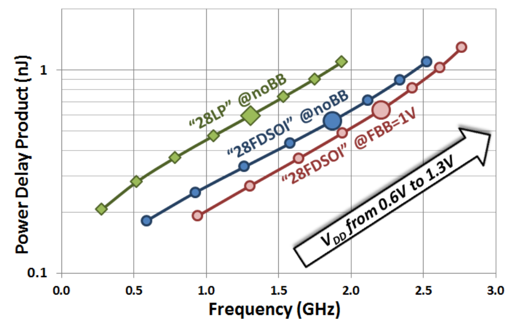


Figure 12 - Compared PDP of LP and planar FD technologies (LVT flavor, typical corner, T=30°C)

In Figure 12, the power-delay product (PDP) vs. frequency from 0.6 to 1.3V voltage range shows a speed increase from 40% to 200% without added energy cost. Moreover, FDSOI technology demonstrates attractive energy efficiency at same speed with a reduction of 50% of power consumption whatever the power supply applied. We can also observe that 28LP is penalized by high dynamic power consumption (V_{DD} is higher), which negatively affects total power figures; in contrast, the 28FD technology is power-efficient across the full V_{DD} and target frequency range. In addition, with adequate forward body-bias (FBB), it is possible either to improve energy efficiency by playing with V_{DD}/F_{BB} trade-off or reach ultra-high speed for bursts of activity.

C. *Wide Back-Biasing Range Opportunities*

In planar UTBB FD-SOI technology, a wide and effective back-biasing enables to adjust threshold-voltage of transistors, to either get more drive current (hence higher performance) at the expense of increased leakage current (FBB) or cut leakage current at the expense of reduced performance (RBB).

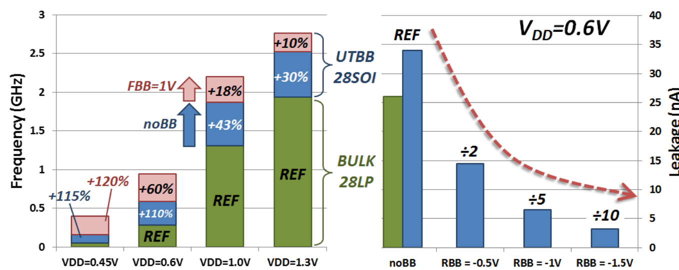


Figure 13 - a. LVT performance boost with FBB
b. RVT Leakage reduction with RBB

Figure 13a demonstrates an efficient frequency boost of planar FD compared with bulk technology at all voltages. With a forward-back-biasing of 1V, FDSOI exhibits very high speed gain from 43% at 1.3V up to 5X factor at 0.45V. In opposite, when performance is not required, planar FD enables to reduce leakage consumption by applying reverse-back-biasing as shown Figure 13b. At 0.6V (typical standby voltage), leakage current could be divided by 2X at -0.5V up to 10X at -1.5V RBB.

V. UWVR Applications and Conclusion

FDSOI UTBB technology presents all the capabilities for very high energy efficiency considering various MPSoC applications. Speed is improved at very low voltage and leakage power is reduced at nominal voltage due to inherent Back Biasing techniques. Ultra Wide Voltage Range operation is then possible and allows new opportunities for application processors requiring a tradeoff between power and speed depending on applicative constraints. Moreover, applications like low power wireless applications are also targeted due to the high performances at low voltage. It would be possible to deliver power to supply the system into a wireless environment considering for example energy harvesting technologies coupled to very high speed DSP into a fully adaptive architecture.

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