Fault Analysis and Simulation of Large Scale Industrial Mixed-Signal Circuits

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***Abstract*—High test quality can be achieved through defect oriented testing using analog fault modeling approach. However, this approach is computationally demanding and typically hard to apply to large scale circuits. In this work, we use an improved inductive fault analysis approach to locate potential faults at layout level and calculate the relative probability of each fault. Our proposed method yields actionable results such as fault coverage of each test, potential faults, and probability of each fault. We show that the computational requirement can be significantly reduced by incorporating fault probabilities. These results can be used to improve fault coverage or to improve defect resilience of the circuit.**

I. Introduction

Avoiding defect escapes and achieving high throughput are two of the main objectives of high volume testing. However, this is becoming increasingly challenging. Continuous progress towards higher levels of integration and higher performance necessitates manufacturing analog and mixed signal circuits with advanced digitally-tuned processes, which display higher defect rates. Defects alter the structure of the circuit; their manifestation is significantly different from process variations. Spot defects are particularly difficult to deal with as they are unpredictable and large in number in new technologies. Despite various robust design techniques, defects still persist and jeopardize test quality. Therefore, it is of utmost importance to prevent fault-related test escapes in order to maintain high test quality.

Fault coverage assessment and fault oriented test methods are mainly developed to address these challenges. Although these alternative approaches are investigated both in academia and industry, progress has been relatively slow. The method is approached with skepticism due to practicality issues and lack of a successful examples.

In this work, we aim at addressing challenges related to fault analysis and simulation of large scale analog circuits. We utilize analog fault modeling and inductive fault analysis techniques that are well-known approaches in the industry and academia. We complement existing IFA techniques with a relative fault scoring methodology to eliminate the need for extensive defect level information on the process. By using this fault importance scoring, we focus on the most likely faults for simulation while still maintaining a negligible DPPM impact due to faults that have not been analyzed which potentially escape the defined tests. We integrate the IFA and fault simulation process approach into the existing design flow at our company (to be disclosed later). We demonstrate this process on a large scale circuit with several thousands of transistors and show that fault simulation can be achieved withing reasonable simulation time while limiting the potential DPPM impact below 50 due to faults that have not been analyzed.

II. Fault Oriented Test

Fault oriented test is radically different from functional test approaches and follows a different flow. The need for fault oriented approach can be explained by contrasting it with functional test.

Process variation introduces deviation in device parameters. However, this variation typically does not result in a significant change in device behavior. Devices are designed to be stable and small perturbations from the nominal operation point result in small changes in the circuit state and therefore in performance parameters as circuit state is continuous with respect to process parameters. Therefore, deviation of performance parameters remain bounded and referred to as process induced performance variation. Testing and performance evaluation is easily extended to handle process variation through defining acceptable performance regions instead of performance points.

However, the situation is completely different for defective devices. Defects introduce diverse behavioral deviations. Different from process variation, defects may result in significant changes that cannot be modeled as perturbations. This can be best explained through a simple example. A broken wire on a feedback loop may not result in an immediate failure of performance parameters or may not even be observable. However, such a defect may result in unpredictable consequences, such as charge leakage/accumulation or coupling, that may result in data dependent failures. Specification tests may not detect this defect if the defect is not observable for the specified tests. This example demonstrates that defects cannot be approached as process variation but require a design/test flow tailored to guarantee device operation.

Analog devices are tested for functionality, i.e., specification based testing. In general, specification based testing may not guarantee proper device operation under fault scenarios. Specifications are high level constraints that guarantee functionality assuming the underlying implementation is structurally unaltered. Ensuring correct operation for structurally altered implementations (i.e., circuit with defects) is more challenging. Companies aim at reducing chances of misclassification by including additional tests at various stressing conditions and using structural testing techniques. These new tests are determined based on experience and trial and error, and

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therefore are subjective and can easily result in under or over-testing.

The main objective of this work is to address these challenges and provide an objective method to assess fault coverage rate of the available tests and provide a way of improving coverage by introducing new tests.

A. Prior Work

Analog fault modeling (AFM) offers a systematic way of analyzing the effects of faults. Originally, the method borrows the fault modeling idea from its digital counterpart, which has been a great success and de-facto method in the digital domain. However, the analog fault modeling approach needs to use more sophisticated modeling tools due to the complex nature of analog circuits. The method relies on mimicking physical faults by inserting fault models in the electrical domain (i.e. using resistors) or by altering component parameters and determining the coverage of the available tests. This enables assessment of the fault detection rate of already implemented tests and provides a way to increase detection rate by adding tests with higher coverage potential.

Early work on AFM focused on parametric faults and circuit level faults. [1] proposed an approach with process variation; while [2] investigated circuit level faults. Parametric faults are typically simulated with out-of-tolerance deviations [3], [4], while open and short faults are simulated via injecting respectively a large and small resistance [5]–[8]. Early work on fault modeling did not include the masking effect of process variation [9], [10], which is becoming increasingly prominent with more advanced processes. Process variation is incorporated in AFM [11], [12] at a cost of increasing computational complexity. Although AFM provides great insight in defective behavior and test coverage, it has not acquired wider adoption by the industry due to its extensive computational requirements.

B. Challenges

The main difficulty in applying AFM to practical circuits has been scaling of the method to large circuits due to its extensive computational requirements. Therefore, most of the published work used small scale circuits to demonstrate the concept. Although this created interest, the subject remained intractable for large circuits.

Due to the difficulties in dealing with large scale circuits and lack of automated tools, fault list generation has been performed based on prior knowledge (subjective) and the generated list is typically incomplete.

Moreover, faults are assigned equal importance due to the lack of process level defect mechanism information and layout level implementation information. This amplified the importance of insignificant faults and polluted the results deeming them inconclusive. In [13], the authors use an IFA based weighting approach to assign more accurate weights. However, this approach assumes equal fault density for all fault types.

Most of the circuits employ robust design techniques such as using wider wires for routing, and multiple devices, connections and routing paths to prevent breaks/opens. Hence, the effect of a fault is insignificant if it is deposited on such a structure. However, if all faults are assumed of equal importance, the number of unobservable faults will be large yielding a very small coverage rate. This is not only confusing but also discouraging as mature processes have a much higher detection rate.

C. Contributions

In this work,

1) We use an automated flow that estimates fault coverage rate using objective criteria.
2) Faults are analyzed and simulated with their probability of occurrence using defect density models. Hence, actionable results are produced. Fault simulation results can be used in test development to improve the coverage or in design stage to improve robustness.
3) We use probability enhanced inductive fault analysis (IFA) to generate a realistic fault list of an industrial large scale circuit. Layout-based fault list generation enables us to generate the complete fault list.
4) We calculate the probability of all faults based on layout level information. This enables us to address poor fault coverage issue as the faults are assigned a weight proportional to their significance.
5) After fault analysis and simulation, robust design techniques are isolated and are not penalized for their impact on fault coverage. We calculate fault probabilities using fault characterization data, such as relative fault densities.
6) For statistical analysis, we use a simple skew-based approach where we eliminate unnecessary simulations. Together with the elimination of insignificant faults, we show that the simulation time can be greatly reduced.

D. Fault Oriented Coverage Flow

A defect is defined as a structural change or a significant change in device parameters. Metal-to-metal bridging through extra metal or extra/missing via are some examples for structural changes, while significant deviation in threshold voltage is an example for parametric fault. Different from process variation, defects are typically local. In this work, we concentrate on structural type spot defects since they are difficult to detect and are the main reason of defect escapes. We evaluate the coverage capacity of available tests to detect potential faults.

Fault coverage of a set of tests can be evaluated using fault oriented testing. These steps are listed below:

1) Fault list generation
2) Injection of faults to the circuit (with process variation) one at a time
3) Simulation
4) Coverage assessment

In the first step, a representative fault dictionary is generated to model potential defect mechanisms. Faults are typically modeled at circuit level using resistors or more complicated models. Typically, a small resistance is used to model bridging faults, while a large resistance is used to model open faults. Fault list generation is a difficult task in general and requires both process level information on defect mechanisms and

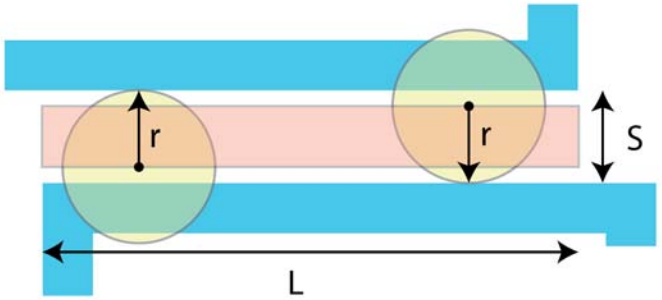

Figure 1. Critical area is the area of the effective regions susceptible for faults.

circuit/layout level implementation information. Typically the fault list is generated based on experience and schematic level fault extraction. However, these approaches result in subjective faults lists. They do not guarantee completeness nor are they capable of assigning occurrence probability for the faults. Inductive fault analysis is used to address these issues as explained in more detail in the following section.

The second and third step of a fault oriented test flow is injection of the extracted faults one at a time and simulation of the circuit to characterize faulty behavior. Finally in the fourth step, faulty responses are evaluated in terms of their detectability for each specified test condition. Detectability in this sense is defined as significant difference from fault free behavior. Detectability depends on observability and masking effect of process variation.

E. Proposed Inductive Fault Analysis Approach

IFA requires extensive characterization information on defect mechanisms and is difficult to obtain. In this work, we use industrial standard defect characterization information that is originally collected to assess yield of mixed-signal circuits. We used the most prominent fault types in our analysis, metal-metal bridge/break and via open/short type of faults. One of the unique feature in this is utilization of defect density, which enabled us to assess fault probabilities.

IFA is considered to be impractical due processing intensity required for fault list extraction. Initial methods [14] that relied on Monte-Carlo approaches were inefficient for large scale circuits. However, with the introduction of the critical area approach [15], [16], the method became more palatable. This approach improves efficiency in fault extraction by concentrating on fault-critical regions only. For example, a metal-metal bridge can occur if two metal traces at the same layer are placed adjacent to each other or metal traces at distinct layers overlap. Examples of these cases are closely routed wires and crossing wires. Critical area approach improves efficiency by concentrating on such close proximity or overlapping regions. The general critical area approach is represented in Figure 1 and is defined as the regions where structural changes takes place if fault are deposited. A bridging type example is shown in the figure. If a fault with radius "r" is deposited in the shaded region, a bridge fault is established.

We are interested in the area of this region as fault probability is directly proportional with this area, given in equation (1).

$$AC_{i,j} = L_{i,j}(2r - S_{i,j}) \quad (1)$$

where i is the fault index, while j is used to index multiple fault locations that can result in fault i. Note that equation (1) depends on a fixed fault radius. However, research has shown that faults have a range of sizes that can be best modeled with a probability distribution [13], [17]. Hence, conditioning equation (1) with equation (3) yield an expected critical area given in equation (2).

$$AC_i = \sum_j \int_{S/2}^{\infty} L_{i,j}(2r - S_{i,j})P(r)dr \quad (2)$$

$$P(r) = \begin{cases} \chi_0^{-2} r & 0 \le r < \chi_0 \\ \chi_0^2 r^{-3} & \chi_0 \le r < \infty \end{cases} \quad (3)$$

The number of expected faults can be calculated using equation (4) by incorporating defect density information.

$$\#def_i = AC_i DD_i \quad (4)$$

Fault oriented analysis can be used to estimate fault limited yield. In this work we concentrate on the testing aspect and evaluate relative fault probabilities in order to assess fault coverage rates. Hence, we calculate the conditional probability of each fault using equation (5), given that there is a defect. In this way, we can decouple the relative fault probability from the overall fault rate of the process.

$$P(def_i|def) = \frac{DD_i AC_i}{\sum DD_i AC_i} \quad (5)$$

Note that since equation (5) yields a relative probability for each fault, these probabilities will integrate to "1", hence yielding the condition that there is a fault in the circuit.

III. Methodology

Fault based coverage evaluation has been around for a while. However, practical demonstration of these approaches have generally not been convincing for the industry due to computational costs and failure to take fault probabilities into account. We demonstrate the practicality of the proposed method using the flow shown in Figure 2.

One of the critical steps in fault list extraction using IFA approach is spotting all potential fault locations. The method has been applied to small scale circuits but was not applied to large scale circuits due to lack of required tools. Fault extraction is a computation intensive process and requires automation tools which are not available for IFA. In order to automate fault extraction, we re-used several scripts that are available by Mentor Graphics that are originally developed to extract proximity regions for digital circuits. We used these scripts and developed an automated tool to extract critical regions and critical area of each region using equation (2). The automated IFA tool processes DEF/LEF files of the design that include geometrical and electrical information of the layout of the circuit and yields critical area parameter pairs (S,L). Then, these pairs are used to calculate critical area and probability of occurrence for all faults using equations (2-5).

It is obvious that due to the various defect mechanisms, the overall number of possible faults would be very large and

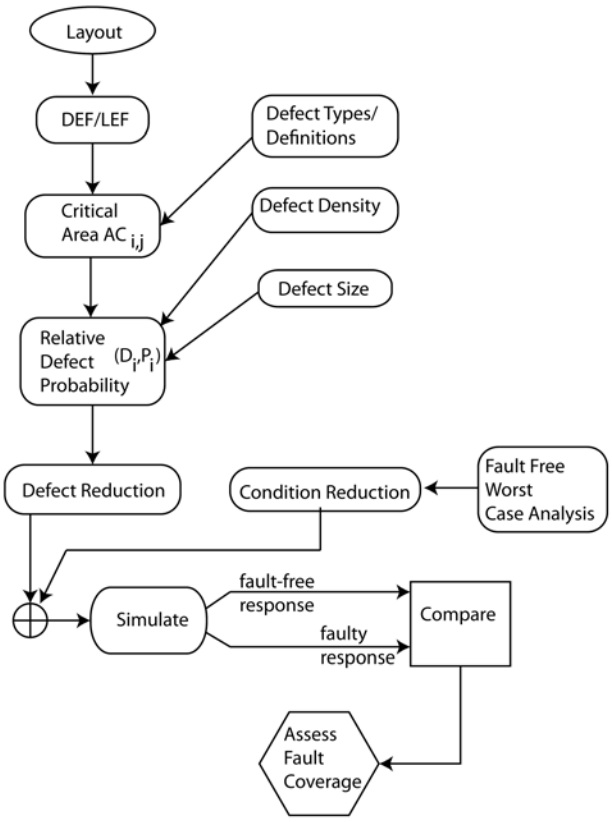

Figure 2. Fault Based Coverage Evaluation Flow

simulation of all these faults would be prohibitive. Here, we make the case of the relative fault probabilities to score the significance of each fault. Then, we select the most significant faults to focus on. The fault list can be selected for various scenarios of defectivity rates; this information need not be very accurate. Our main objective here is to limit the DPPM impact of faults that we will not simulate.

To link the relative fault probability information to an upper-bound of DPPM impact, we can make some assumptions: (a) all ungraded faults will be undetected, (b) all yield loss and customer returns are a result of faults. Based on these pessimistic assumptions, we can select a subset of most likely faults to simulate while limiting the DPPM impact of ungraded faults. For instance, if the relative probabilities of selected faults up to 99.9%, and the overall yield of the circuit is 90%, then the DPPM impact of the ungraded faults will be upper bounded by 100.

Once the fault list is generated, faults are injected one at a time and simulated with process variation. Process variation can be emulated depending on the available statistical model of the process. Typically Monte-Carlo or skew based methods are used to assess the effect of process variation.We use a very simple adaptive skew based approach for simulation. We first identify a set of skews that result in worst case performance degradation for the fault free circuit. Then, we simulate the nominal and worst case behavior of the defective circuits under the given test scenarios. If this behavior is significantly different than the behavior of the fault free circuit, then we deem this fault detected and move on. For instance, if there is complete signal or functionality loss, then the fault will be certainly detected. However, if there is a performance deviation, we take all process skews and assess the detectability in terms of overlap between fault-free and faulty-circuit responses.

	Specification Parameters	Acceptable range around nominal	Explanation
1	HP_BGAP	±5%	high power band gap
2	LP_BGAP	±5%	low power band gap
3	Vout1	±1%	Run mode
4	Vout2	±1%	
5	Vout1_sleep	±1%	Sleep mode
6	Vout2_sleep	±1%	
7	Vout1_wu	±1%	Wake-up mode
8	Vout2_wu	±1%	

Table I
SPECIFICATION PARAMETERS IMPLEMENTED IN THIS WORK.

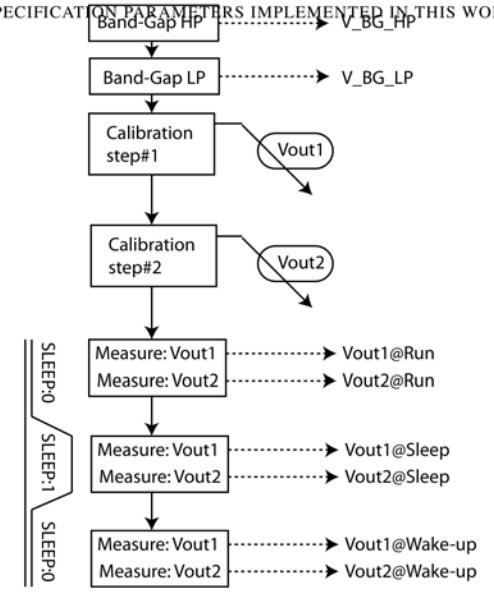

Figure 3. Test/Calibration scheme

A. Case Study: A Large Scale Power Management Circuit

We demonstrate our method on a large scale industrial power management circuit that consists of several thousands of transistors. The circuit provides two constant voltage supplies that provide low and high power and work at various loading conditions. Specification parameters of the circuit include output voltages of regular operation mode, sleep mode, and wake-up mode. Current test list for the circuit is given in Table I.

Specification parameters defined for the circuits are band-gap reference voltages and calibrated output voltages. Tolerance of band-gap circuits are 5% and calibrated specification parameter tolerances are 1%. Note that the two output voltages provided by the circuit are specified at three different states: run mode, sleep mode, and wake-up mode.

System level block diagram of the circuit is given in Figure 3. Note that the circuit includes calibration units and some of the specification parameters depend on these calibration units. Testing process of the circuit involves sequential measurement and calibration steps, also summarized in Figure 3. Voltage readouts are obtained for all calibration states and the calibration state that yields the desired output voltage is selected for both low and high power voltages. Once calibration parameters are determined, they remain permanent and used throughout the rest of the test process.

	VDD	Temperature	Process corners
parameters	3.5V, 4V, 4.5V, 5V	-40,25,125	1 typical +8 corners

Table II
CIRCUIT IS SIMULATED FOR VARIOUS SUPPLY VOLTAGE, TEMPERATURE AND PROCESS CORNERS.

corner	Temp	VDD
Typ	-40	3.5
Typ	125	5.5
Typ	25	5.0
wcs	-40	3.5
wcs	125	5.5
wcs	25	5.0
Rc_max	-40	3.5
Rc_max	125	5.5
Rc_max	25	5.0

Table III
WORST CASE DISPERSION CONDITION CAN BE EMULATED USING ONLY 9 OUT OF 108 POSSIBLE CONDITIONS.

Sleep mode voltages are obtained by putting the circuit in sleep mode through signal shown in Figure 3. This step ensures that the circuit is switched to stand-by mode and provides voltages specified for stand-by mode. Finally, the circuit is switched back to run mode (wake-up) and output voltages are recorded.

Faults are injected one at a time and simulated with process variation to measure response of the implemented tests. Each test parameter result is recorded with their corresponding variation. Simulations are run at different conditions listed in Table II.

Note that these conditions induce different effects on the circuit and require re-calibration for each condition.

Simulation time of the circuit at a particular condition is a few hours depending on the injected fault as the faults may result in convergence issues. Multiplying this number with the total number of combinations, 108, and the number of faults, it is clear that simulations are not affordable unless an optimized simulation method is devised.

IV. SIMULATION OPTIMIZATION

The purpose of taking measurements at different working conditions and injecting process variation is to ensure proper operation at various conditions, and most importantly worst case conditions.

In order to reduce simulation burden to an affordable level, we used only simulation conditions that resulted in significant performance dispersion. We evaluated device performance at all conditions and selected a condition if it results in a worst case scenario for any of the specification parameters. Hence, we have compacted total of 108 conditions to 9 conditions, listed in Table III.

As a second level of simulation budget optimization, we have eliminated insignificant faults that have low probability of occurrence. We have eliminated the faults that have probability of occurrence less than 10^{-12}, hence practically eliminating their contribution to defect escape level. Moreover, we sort the injected fault list such that most likely faults are simulated first. Thus, significant portion of the faults are simulated with less effort. We have observed that only a small fraction of the faults have a significant importance. Less than 1% of the faults are the most likely 99% of the faults.

Total # of faults	10200	Reduced (538)	Probability weighted
detected	80	80 [14.7%]	40.4%
not detected	312	312 [57.1%]	59.5%
not simulated	9810	146 [26.7%]	0.1%

Table IV
40.4% OF THE IMPORTANCE WEIGHED FAULTS ARE DETECTABLE USING THE IMPLEMENTED TEST LIST. 96% OF THE FAULTS HAVE ONLY 0.1% SIGNIFICANCE AND IS OMITTED TO REDUCE SIMULATION BURDEN.

V. RESULTS

We applied the proposed methodology to a industrial large scale circuit of thousands of transistors. Fault coverage results are summarized in Table IV. More than 10k potential fault locations are extracted and checked for detectability. Approximately 400 faults are evaluated due to long simulation time requirement. Out of the obtained results, 80 faults are identified as detectable by the implemented test list, while 312 of the faults are identified as undetectable, shown in the second column of Table V.

Note that the obtained results correspond to only 3.8% of the total faults and therefore do not provide a conclusive result. The second column shows what can be obtained without using probability information generated using IFA method. However, using the probability information we show that this 3.8% is in fact the most important 99.9% of the fault set and enables us to reach a solid coverage result.

Elimination of insignificant faults reduces the number of faults from ~10k to only 538 faults, shown in the third column.

Weighing the faults with their probability of occurrence information show that obtained results are in fact the most important 99.9% of the faults and show that evaluating only a small fraction of the faults is sufficient. Moreover, the coverage information is more realistic.

The importance of the results shown in Table IV is twofold. Firstly, the generated fault list is complete for the given fault mechanisms. This is a great advantage compared to schematic and knowledge based methods as they do not guarantee completeness. Since coverage computation directly uses the total number of faults, subjective fault list generation methods provide yield highly subjective results that bear little information. Therefore, it is necessary to use IFA method to obtain meaningful objective results. Secondly, the results show that incorporating probability information yielded meaningful coverage results. Coverage rate increased from 14.7% to 40.4% after using probability information which is closer to the actual yield level of an industrial product.

Although we have obtained a more realistic coverage estimate, the results may be discouraging as most test engineers expect to see a coverage rate close to 100%. However, analog circuits are bound to lower coverage rates due to observability issues and tolerance bounds of specification parameters. Different from digital circuits, analog circuits are allowed to perform in an allowable band of its operating region that results in masking some of the faults and therefore limiting the observability.

One of the contributions of this work is to demonstrate that fault coverage and functionality test are differently approached and are not perfectly compatible. We demonstrate this using

fault type	node1	node2	probability
bridge	dvss	avss	17.6%
bridge	vddpll_lp_fb1	avss	3%
bridge	dvss	vpd_fb	2.2%
bridge	net_0231	dvss	2.1%
bridge	vpb	vout	1.8%

Table V
MOST SIGNIFICANT UNDETECTABLE FAULTS. ALTHOUGH THE FIRST FAULT HAS VERY HIGH PROBABILITY OF OCCURRENCE, ITS HAS NEGLIGIBLE IMPACT ON DEVICE OPERATION. FAULTS WITH INSIGNIFICANT EFFECT CAN BE DROPPED FROM COVERAGE ANALYSIS TO OBTAIN REALISTIC RESULTS.

	Initially	After Fault reduction	After Condition reduction
#faults	10200	546	546
#conditions	108	108	9
total # of simulations	1.1M	~59k	4914
cumulative reduction	0%	94.6%	99.55%

Table VI
SIMULATION PLANNING AND OPTIMIZATION REDUCES COMPUTATION BURDEN BY 99.55%

Table V, where the most important un-detectable faults are listed. The most prominent fault is an analog-vss to digital-vss short fault that has 17.6% relative probability and is coincidentally undetectable. After discussing the potential effects of this particular fault with the design engineer of the circuit, we reached the conclusion that this fault poses no significant danger to the circuit operation. Therefore this fault type can be omitted in coverage analysis which would certainly boost the overall coverage level. Similarly, the rest of the list can be analyzed and insignificant faults can be dropped to obtain a coverage result reaching the actual yield level of the device. By reducing the number faults that one needs to analyze either through fault simulation or through fault scoring, we are able to go one step forward and individually analyze the faults that create most coverage problems and modify fault list, design, and test steps. For instance, if the above-mentioned fault posed a danger for the overall operation of the device, we would have to devise a test plan to detect it.

A. Simulation efficiency

Coverage results are obtained through efficient simulation planning and optimization. It is evident from our previous results that only a small fraction of the faults are significant and are sufficient to be analyzed therefore enabling simulation and analysis time to fit within an acceptable budget. We first perform fault reduction to drop insignificant faults and then perform condition reduction by using only worst case conditions. Simulation reduction results are given in Table VI. Fault reduction yields a 94.6% reduction, while condition reduction enables us to obtain 99.55% overall reduction in the total number of simulations. This corresponds to 224 fold simulation time reduction.

VI. CONCLUSION

Fault oriented testing offers superior test quality improvement. However, fault analysis of analog circuits is challenging and requires extensive process level information and compute-power. These challenges restrict the applicability of fault oriented testing of analog circuits for large scale industrial circuits. We propose an efficient flow to overcome these difficulties and demonstrate the method with a large scale industrial analog circuits with several thousands of transistors. Using the proposed method, we extract potential fault locations automatically, compute probability of each fault and calculate fault coverage of the test list of the circuit.

The obtained results are invaluable for test quality improvement. The analysis results can be used to optimize the test list while maintaining a high quality level or to modify the design to improve defect resilience. Fault probabilities enables us to assess fault priority for each fault and maximize fault coverage with a small number of tests.

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