Stochastic degradation modeling and simulation for analog integrated circuits in nanometer CMOS

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***Abstract*— Reliability is one of the major concerns in designing integrated circuits in nanometer CMOS technologies. Problems related to transistor degradation mechanisms like NBTI/PBTI or soft gate breakdown cause time-dependent circuit performance degradation. Variability and mismatch between transistors only makes this more severe, while at the same time transistor aging can increase the variability and mismatch in the circuit over time. Finally, in advanced nanometer CMOS, the aging phenomena themselves become discrete, with both the time and the impact of degradation being fully stochastic. This paper explores these problems by means of a circuit example, indicating the time-dependent stochastic nature of offset in a comparator and its impact in flash A/D converters.**

Keywords—analog integrated circuits; aging; reliability modeling and simulation

I. INTRODUCTION

The evolution towards nanometer CMOS technologies below 65 nm has introduced increasing reliability challenges in integrated circuits [1]. These include spatial problems such as increased variability and mismatch, temporal problems such as aging phenomena, and environmental operational problems such as EMI interference. The aging phenomena include both interconnect degradation (e.g. electromigration) as well as device degradation (e.g. BTI, Hot Carriers, Soft Breakdown). While transistor BTI and Hot Carrier degradation in larger CMOS technology nodes or for larger devices are rather deterministic and easier to model, these phenomena – like soft breakdown always has been – become fully discrete stochastic at lower technology nodes and for small devices, hence causing the aging to become stochastic across identical circuits. In addition, even within the same circuit, initial mismatch or different stressing may cause circuit performance to become stochastic and increasing over time. These problems will fully be illustrated in this paper by means of an example circuit.

This paper is organized as follows. Section 2 briefly describes the different transistor aging phenomena and the corresponding models used. Using an efficient statistical aging simulation tool, section 3 then illustrates the resulting time-dependent stochastic performance behavior by means of the increasing offset of a comparator used in flash A/D converters. Section 4 provides the conclusions.

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II. TRANSISTOR AGING PHENOMENA

A. Transistor Aging

When a transistor is stressed with some non-zero V_{GS} and V_{DS} voltages, time-dependent degradation phenomena occur inside the transistor. These cause a change of the transistor parameters (V_T, μ, r_o) as a function of time. This change may turn an initially fully functional circuit into a less or even non-functional circuit over time [2]. The amount of degradation of course depends on the stress applied to the device, but also on the temperature T and on design parameters such as the sizes (W and L) of the transistor. Fig. 1 qualitatively indicates the impact of these mechanisms on the I_{DS}-V_{DS} characteristic of a MOS device for some arbitrary stress time. The resulting degradation in for instance threshold voltage can typically be modeled with a power law dependence on the stress time t [3]:

$$\Delta V_T = A(V_{GS}, V_{DS}, T, W, L...)\, t^n \quad (1)$$

where n is the process-specific exponent of time. Both the value of n and the function $A(...)$ depend on the actual aging phenomenon considered. The most important transistor aging degradation mechanisms will now be discussed in more detail.

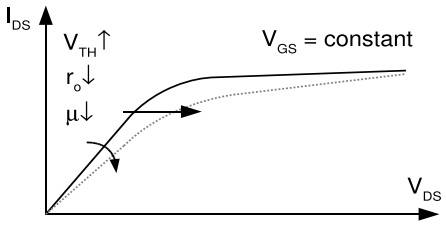

Fig. 1. Time-dependent variation of the characteristics of a transistor due to Hot-Carrier and BTI degradation [2].

B. Hot-Carrier Degradation

When a transistor is stressed, the large electric field near the drain end of a transistor in saturation produces hot carriers [3,4]. These carriers introduce both oxide and interface traps (near the drain) and a substrate current. This will gradually shift the device parameters. As holes are much 'cooler' than electrons, hot-carrier effects in nMOS devices are proven to be more significant than in pMOS devices [5]. A typical value of n in (1) is around 0.45.

C. Bias Temperature Instability

Two different Bias Temperature Instability (BTI) phenomena can be observed: negative BTI (NBTI) and positive BTI (PBTI). NBTI occurs in pMOS transistors when a negative bias voltage is applied, and especially at higher temperatures [6]. This effect is a significant reliability threat in both older SiO_2 and SiON technologies and is still a problem in newer high-K metal-gate technologies [7]. The PBTI effect affects nMOS transistors and results in a similar wear-out behavior as NBTI, but has only been observed in high-K metal-gate nMOS devices, and can be similar to or even larger than the NBTI effect [8]. Currently, there still is no full agreement about the microscopic origins of both BTI phenomena. Most authors argue that the NBTI effect results from a combination of hole trapping in oxide defects and generation of interface states (e.g. due to breaking of SiH bonds) at the channel oxide interface [9,10,11]. PBTI is believed to come from electron trapping in preexisting oxide traps, combined with a trap generation process [12]. The result is a shift in threshold voltage and mobility, similar to equation (1), but with a different exponent n (typically around 0.16) and a different function *A(...)*.

A peculiar property of the BTI mechanism is the relaxation or partial recovery of the degradation immediately after the stress voltage is reduced [13]. The relaxation of the threshold voltage shift has been observed to have approximately a logarithmic time dependence and spanning times from microseconds to days [14]. As shown in Fig. 2, NBTI degradation does not recover fully, leaving a permanent degradation *P* when the stress is removed. A complete model of NBTI useful for circuit analysis in a SPICE-like simulator is presented in [15].

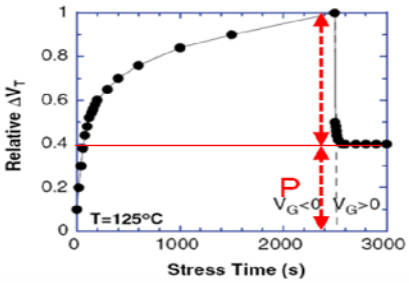

Fig. 2. BTI degradation showing partial recovery when the stress is removed, still leaving a permanent degradation P.

BTI effects in large micrometer-sized transistors are typically considered deterministic [15,16]. The application of a given stress on matched transistors therefore results in an identical shift of the transistor parameters. Scaling transistors down to nanometer dimensions, however, gradually changed these deterministic effects into stochastically distributed failure mechanisms due to the increasing impact of the individual trapping and detrapping events, as shown in Fig. 3 [17,18]. Both the moment in time and the impact of the events are stochastic. At device level this results in a time-dependent shift of the transistor parameters augmented with a time-dependent increase of the standard deviation $\sigma(V_T)$ on these parameters. Initially matched transistors, processed in ultra-scaled nanometer CMOS technologies, can therefore cause circuit performance failure resulting from this increased time-dependent transistor mismatch [19], as will be illustrated in section III below.

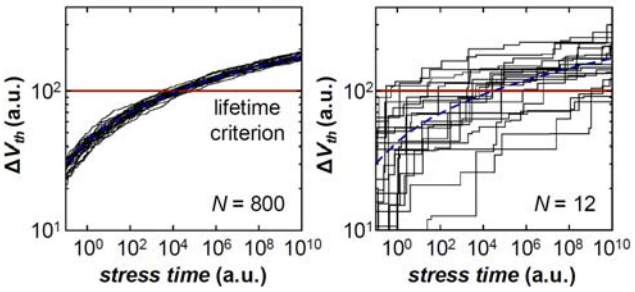

Fig. 3. Due to the discrete nature of the trapping and detrapping events, the time-dependent BTI-induced V_T shift becomes stochastic for small devices in sub-45nm CMOS [17,18], hence also making the lifetime being spread stochastically.

D. Time-Dependent Dielectric Breakdown

In nanometer CMOS the strong electric field across the gate oxide can cause oxide damage resulting in dielectric breakdown (BD). BD is a local stochastic phenomenon, and results in an increase of the transistor gate current. During the degradation process different BD modes can be distinguished. For oxide thicknesses below 5nm, hard breakdown can be preceded by soft breakdown (SBD) [20]. The latter can be observed as a partial loss of the dielectric properties, resulting in a smaller increase of the gate current compared to hard breakdown [21,22].

The probability to have *n* SBD defects at time *t* can be described with a Poisson distribution [23]:

$$P_n(t) = \frac{1}{n!}\left(\frac{t}{t_{SBD}}\right)^{\beta n} \exp\left(-\left(\frac{t}{t_{SBD}}\right)^{\beta}\right) \qquad (2)$$

where β is a process-dependent parameter with typical value 1.2, and t_{SBD} depends on the transistor area and the applied stress voltage. Being valid for fixed voltages, the above equation is slightly different for time-varying voltages. An approach for stochastically analyzing SBD is presented in [24]. Because SBD is a stochastic effect, it may result statistically in an increasing asymmetry over time between identical devices, hence also resulting in a time-dependent mismatch and offset in analog circuits.

III. ILLUSTRATION OF STOCHASTIC RELIABILITY ANALYSIS

Due to the impact of time-dependent degradation on integrated circuits, and especially analog integrated circuits, it is important to analyze quantitatively the impact of the above degradation phenomena and to identify potential reliability problems at design time, so that – if needed – the design can be modified to guarantee correct functionality and performance over the entire lifetime of the electronic product [19]. We will first briefly describe a proper reliability simulation tool that can be used for such analysis. Next, we will illustrate this analysis methodology to demonstrate the impact in an analog circuit of mismatch growing over time.

A. Stochastic Reliability Analysis Tool

In [25,26] an efficient method for reliability simulation is presented, which offers more correct reliability analysis results than commercial tools. It uses a short transient simulation that provides accurate information about the stress at every circuit node, while a degradation extrapolation ensures a fast simulation result with the error being managed carefully. Fig. 4 gives a schematic representation of this reliability simulation algorithm. The input to the simulator is a fresh (i.e. unstressed) netlist. A transient simulation over a short time period is performed on the input netlist. As circuit input a periodic time-varying signal is applied. Once the stress pattern on every transistor node is calculated from this initial simulation, it is extracted and passed on to a degradation model, which extrapolates the transistor degradation over a longer time period. This results in a shift in the operating point, requiring the same steps to be iterated a number of times. Finally, a degraded version of the netlist is created as an output. In such degraded netlist every transistor is represented by a subcircuit where the additional dependent sources model the shift in threshold voltage, mobility and output conductance respectively (see Fig. 5). A designer can use this output netlist to study the impact of degradation over the product lifetime and to identify the reliability weak spots in the design.

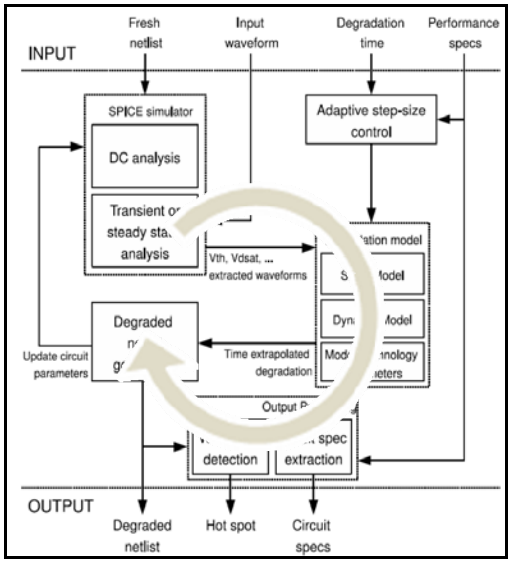

Fig. 4. Flow diagram of the efficient aging degradation analysis tool for analog circuits [25,26].

To include the statistical variations of the process parameters and/or the discrete stochastic nature of the aging phenomena, the above nominal reliability analysis needs to be repeated for a large number of statistical instances. To avoid time-consuming Monte-Carlo analysis, a more efficient variability-aware reliability analysis has been developed [26]. Efficiency in this flow is obtained by the pre-screening of important statistical parameters and an efficient calculation using response surface models built with design of experiment (DOE) data generation and regression. The method results in a nearly-linear overall simulation complexity as a function of the number of stochastic parameters.

To simulate even larger circuits with good accuracy in an acceptable CPU time, the methodology has recently also been extended to the hierarchical analysis of large circuits [27].

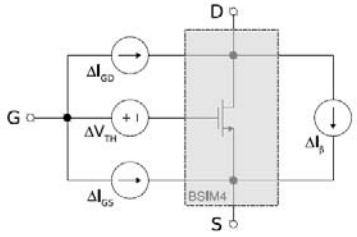

Fig. 5. Equivalent subcircuit for a degraded transistor with the original transistor being modeled by standard models such as BSIM4 and the time-dependent aging degradation being modeled by the additional dependent sources around the transistor. Such subcircuit model can be used in standard SPICE simulators.

B. Reliability Analysis of a Clocked Comparator

As example circuit to demonstrate the stochastic and hierarchical reliability analysis [28], we use a clocked comparator as shown in Fig. 6. Adding the impact of stochastic effects reveals a lot of extra information about the time-dependent performance of the comparator. The circuit is simulated in a 32nm CMOS predictive technology with 1V supply. The comparator is subjected to the following stress voltages: at the input of the comparator a sine wave with 0.4V amplitude and a DC bias of 0.5V is applied, while the voltage at the reference input is 0.2V. The circuit performances of interest are the input offset voltage and the slew rate. Model parameters for the process variations and stochastic aging effects are obtained from [29] and [16] respectively.

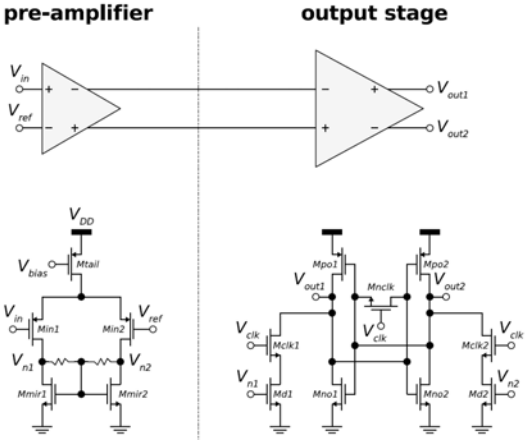

Fig. 6. Schematic of the clocked comparator example circuit used to illustrate the stochastic reliability analysis.

If $V_{in} > V_{ref}$, the stress voltage on the gate of transistor Min2 is larger than the voltage on the gate of Min1. Also, the stress on Md2 will be larger than the stress on Md1. As a consequence, Min2 and Md2, which age due to NBTI and PBTI respectively, will degrade more than Min1 and Md1 (see Fig. 7). On the other hand, if the input voltage is low and $V_{in} < V_{ref}$, the situation is reversed and Min1 and Md1 will age more than Min2 and Md2. The latter, however, only happens during

a small fraction of the time. Overall, due to this asymmetric stress applied at the circuit input, Min2 and Md2 will age more than Min1 and Md1. This results in a time-dependent increase of the mismatch between the transistors in the circuit and in turn affects the circuit performance. As a result of this, Fig. 8 shows that the input offset changes from nearly 0V to 1.27 mV over a time span of five years. The slew rate, which mostly depends on the transistor drive current and the output capacitance, remains fairly constant. The change in both performance parameters has a log(t) time dependence, which corresponds to the logarithmic time dependence of the NBTI and PBTI effect.

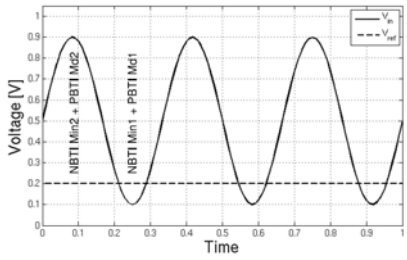

Fig. 7. Stress waveform applied to the example comparator circuit. The regions of degradation for the different transistors are indicated.

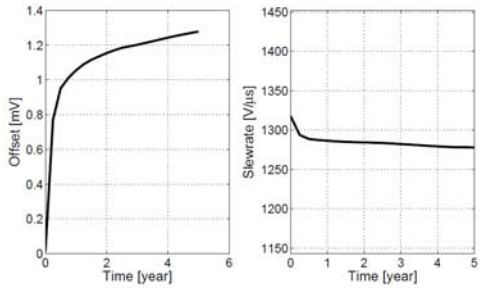

Fig. 8. Aging-induced circuit performance shift in the comparator: the input offset is very sensitive to circuit aging, while the slew rate remains more or less constant.

Fig. 9 (left) shows the V_T shift for every transistor in the circuit. The V_T shift of the output-stage transistors is very large, compared to the shift in the other transistors, although still rather small in an absolute sense (maximum shift is 41 mV). The reason is the application of large stress voltages to the transistors in the output stage (V_{GS} = V_{DD} when switched on). Nevertheless, the aging of the output transistors does not have a large impact on the performance the circuit. As shown in Fig. 9 (right), the results of the sensitivity analysis indicate how the offset shift mostly results from degradation in transistors Min2 and Md2, which also corresponds to the intuitive designer analysis.

Fig. 10 (left) shows the comparator input offset as a function of time, evaluated on 100 random samples evaluated with a circuit model generated with the DoE-based reliability simulator [26]. The mean offset shift corresponds to the result obtained from the deterministic reliability simulator (see Fig. 8). The figure can be used to get a first impression of the initial spread on the offset due to process variations, as well as the time-dependent shift due to deterministic and stochastic aging effects. Fig. 10 right depicts a cumulative density function (CDF) of the offset for a fresh circuit (time t=0s) and an aged circuit (time t=5years). The straight and dashed lines represent the evaluation of the circuit model, generated by the DoE-based stochastic simulator, in 100 sample points. The markers are 10 (different) sample points evaluated with the MC-based stochastic simulator. The results match very well, demonstrating a good accuracy of the circuit model. Although the average offset value shifts due to transistor aging, the spread on that value (which is a function of the slope of the CDF) does not change much.

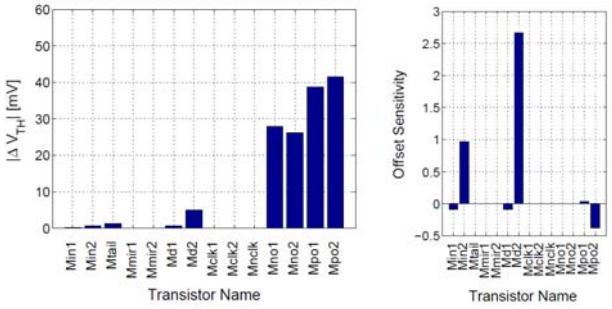

Fig. 9. Analysis of the aging-induced V_T shift of every transistor in the comparator (left), and sensitivity of the offset to the V_T shift of every transistor (right). Both aspects are needed to get a clear view on the impact of aging on circuit performance.

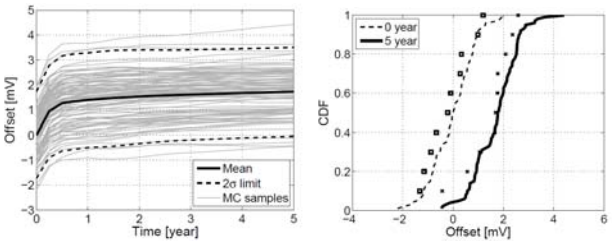

Fig. 9. Comparator offset as a function of the stress time for 100 random samples evaluated with the DOE-based stochastic reliability analysis (left). Cumulative distribution function of the offset for a fresh circuit (time t=0s) and for an aged circuit (time t=5years), showing both the results of 100 samples of the the DOE-based stochastic simulator (lines) versus 10 random samples with the MC-based simulator (markers) (right).

The circuit performance space for the two observed performance parameters for a fresh circuit and a circuit after a stress time of five years, is depicted in figure Fig. 10. The average slew rate remains more or less constant, which is in agreement with the deterministic simulation results depicted in Fig. 6. The offset, however, shifts a lot: the average offset shift increases to nearly 2mV, while some outlier samples even reach an offset value larger than 4mV. From this figure, it is clear that if a designer does not want this circuit to fail after 5 years, (s)he should either include redundancy or design the circuit taking into account the combined variation visualized by the two sample clouds in Fig. 10 [18].

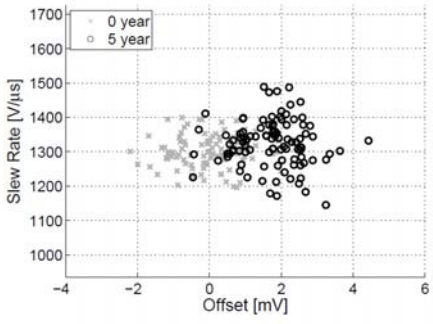

Fig. 10. The stochastic performance space for the offset and the slew rate for a fresh circuit and a circuit after a stress time of five years for the comparator example circuit in 32nm CMOS.

Finally, Fig. 11 shows the predicted time-to-failure distribution when the failure criterion $|V_{offset}| > 2.5mV$ is used. A 95% confidence bound on that prediction is also given. Due to the logarithmic BTI time dependence, 10% of the samples fails before one year, while after 5 years of stress another 12% has failed. The average offset shift does not surpass the 2.5mV limit. Nevertheless, due to process variations and stochastic aging effects, part of the samples do fail before the intended circuit lifetime. This result demonstrates the importance of using a stochastic reliability simulation instead of only a deterministic simulation.

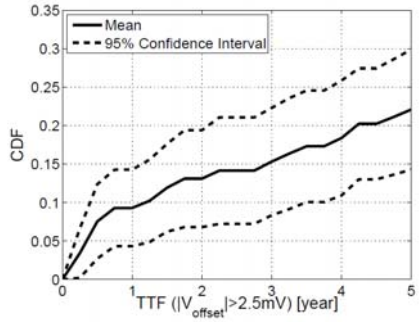

Fig. 11. The cumulative density function for the time to failure of the comparator circuit (together with 95% confidence interval bounds). A circuit is considered to fail if the offset surpasses 2.5 mV.

C. Reliability Analysis of a Flash Analog-to-Digital Converter

The clocked comparator analyzed above is now integrated in a 6-bit flash analog-to-digital converter (ADC), as shown in Fig. 12. The reliability of this converter is simulated with a hierarchical reliability simulator [27] in a predictive 32nm CMOS technology with 1V supply voltage [29]. The analog part of the circuit consists of more than 1000 circuit elements. The ADC contains 63 clocked comparators, each comparing the input voltage to a different reference voltage. The accuracy of an ADC is typically described by the effective number of bits (ENOB), which in its turn is determined by the integral (INL) and differential (DNL) nonlinearity of the converter. Both the INL and DNL are mainly determined by the mismatch between the resistors of the reference ladder and by the input-referred offset of each comparator. Right after production, both are only determined by process variations, but mismatch can change over time due to BTI effects.

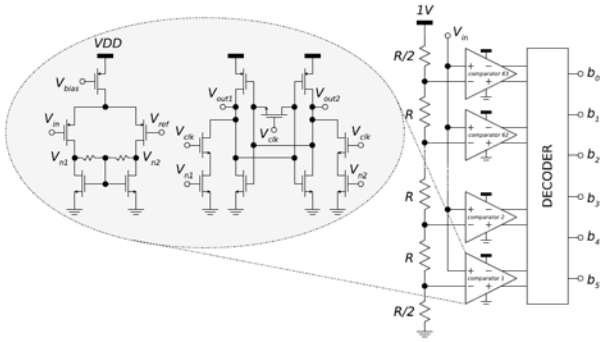

Fig. 12. Flash analog-to-digital converter in which the clocked comparator is used to compare the input signal with the reference values.

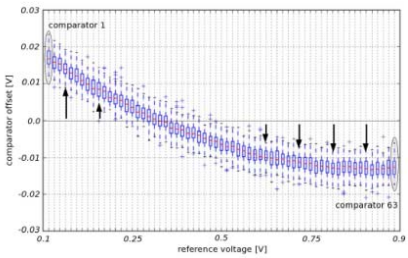

Fig. 13. The input-referred offset voltage for each flash ADC comparator after 1 year of stress and for 100 random samples, all evaluated with the comparator subblock model. The arrows indicate the offset shift between the initial state and after wear-out.

The clocked comparator is modeled as a one-system subblock, with the reference voltage as a circuit input that can vary between the ground and the supply voltage. As an input to the ADC, a sine wave with a fixed frequency of 100Hz, an amplitude of 0.4V and a DC bias of 0.5V was applied. The evaluation of the comparator model, built using the active sample selection algorithm and the FFX regression method [30] returns a tuple of time-dependent input-referred offset voltages after different stress times. Figure 13 depicts the input-referred offset for each comparator after 1 year of stress and for 100 Monte-Carlo samples, all derived from the comparator subblock model. Comparators at the top and the bottom of the reference ladder are particularly sensitive to transistor aging since they suffer from large asymmetric voltage stress. The bottom comparator for example (i.e. comparator 1 in Fig. 12) is at one side stressed by a very low reference voltage, while the other side sees the ADC input (i.e. the sine wave signal). Since NBTI is exponentially dependent on the magnitude of the gate voltage stress, this results in a large threshold voltage mismatch between the input transistors (on average the shift is 17mV after 1 year for comparator 1). A similar effect can be observed for comparators at the top of the reference ladder (e.g. comparator 63 in Fig. 12). As a result, the input offset increases over time and causes a reduction of the ENOB.

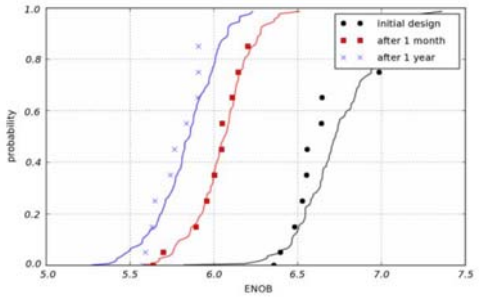

Fig. 14. Normal probability plot of the ENOB of the flash ADC for 100 random samples evaluated with an hierarchical simulator (solid lines) and 10 samples evaluated with full system simulations (markers) for the fresh circuit and the aged circuit after 1 month and 1 year.

Fig. 14 shows a normal probability plot of the ENOB right after production, after 1 month of operation and after 1 year. The solid lines are the ENOB as computed by the hierarchical models of the comparators, while the markers represent the ENOB calculated from a full system aging simulation with a Monte-Carlo-based stochastic aging simulator. It can be seen how process variations cause a large initial spread on the ENOB, while the graph shifts towards lower values due to aging effects. A good correspondence between the model and the full system simulations is observed. Moreover, the logarithmic time dependence of the NBTI effect is also observed. The discrepancy at time zero is due to the limited number of full system simulations (only ten).

The demonstrator circuit has been simulated on a dual-quad core 2.8GHz Intel Xeon processor with 8GB of RAM. The model build time for the comparator subblock took 31 minutes, while the evaluation of the entire converter took 1 minute and 41 seconds for 100 Monte-Carlo samples. Evaluation of just one Monte-Carlo sample using a nonhierarchical deterministic reliability simulator took 1 hour and 55 minutes. This results in a speedup of 360x when evaluating 100 random samples with both methods.

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