Role of Design in Multiple Patterning: Technology Development, Design Enablement and Process Control

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***Abstract*—Multiple-patterning optical lithography is inevitable for technology scaling beyond the 22nm technology node. Multiple patterning imposes several counter-intuitive restrictions on layout and carries serious challenges for design methodology. This paper examines the role of design at different stages of the development and adoption of multiple patterning: technology development, design enablement, and process control. We discuss how explicit design involvement can enable timely adoption of multi-patterning with reduced costs both in design and manufacturing.**

I. Introduction

With feature dimensions reaching the nanometer scale, manufacturing is no longer the sole enabler of technology scaling. Design-technology co-optimization is key to ensure economically viable, timely adoption of technologies.

A. Design-Patterning Interactions

Design and technology interact in three stages during the technology lifecycle:

- *Technology development.* Goal of a technology is improvement in design metrics such as power, performance and area as well manufacturing metric of cost. In context of patterning, layout configurations that are difficult to manufacture are identified. Technology developers then need to decide on which layout configurations to enable – by pushing the manufacturing process – and which ones to forbid in the design. To make such decision, a prediction of the design implications of forbidding/allowing each configuration is needed [1]–[3].
- *Design enablement.* All modern technologies require significant changes in the design flow. This is especially true for layout design. Layout restrictions imposed due to peculiarities of manufacturing processes are increasingly common and require changes in cell layout as well as placement and routing methodologies. Hotspot checkers [4,5] as well as lithography-aware placement [6] and routing [7] are examples. Timely technology adoption requires its timely enablement in design.
- *Process Control* Geometric control of patterning can be very pessmistic; small fragment errors average over full features which themselves average over critical paths. Moreover, not all features and paths are equally important. As a result, design-aware electrical setting of process control requirements is important [8]. Design-aware optical proximity correction [9,10] and mask inspection [11] have already been shown to have significant advantages.

B. Multiple-patterning lithography

Conventional optical lithography has reached physical limits at 22nm technology node. Unavailability of the next-generation lithography (e.g., EUV) for high-volume manufacturing has made the extension of optical lithography with multiple patterning the only viable solution for further technology scaling.

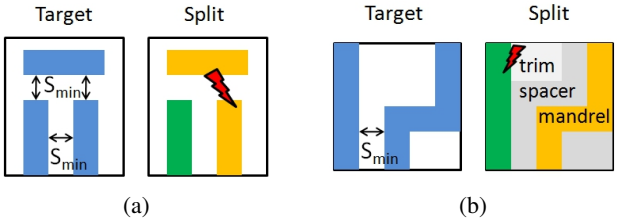

Figure 1. Examples of a LELE forbidden pattern (a) and a SADP forbidden pattern (b). S_{min} denotes the minimum spacing of single-patterning.

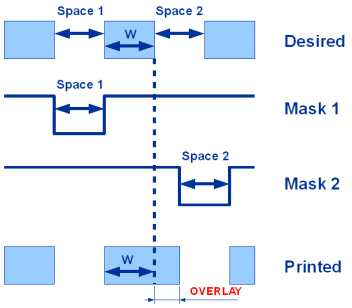

Figure 2. Example showing translation of overlay error into CD variation in negative-tone DP process.

Multiple-Patterning lithography (MP) enhances the resolution of a lithographic system by using multiple lithography-exposure steps to form a single IC layer. The simplest form of MP is Double-Patterning lithography (DP) involving only two exposure steps. MP/DP can be implemented with different manufacturing processes with the most viable being the Litho-Etch-Litho-Etch (LELE) and Self-Aligned Double-Patterning (SADP), a.k.a. spacer double patterning. In LELE DP, layout features are split into two sets, each getting formed with a separate litho-etch step. This layout decomposition effectively relaxes the pitch of each exposure compared with that of the final printed-image on wafer (ideally by half). In SADP, sidewall spacer defines either spaces or lines depending on the tone of the process. A first set of patterns is formed in a first exposure, a thin film is deposited around the first set of patterns in a spacer-like process, and extra printed features are trimmed away using an additional exposure known as trim exposure.

In all various processes of MP, layout decomposition (a.k.a. coloring) is constrained so that features assigned to the same exposure meet the pitch/spacing requirements of single-patterning process. As a result, each of the different flavors of MP imposes restrictions on the design layout. For example, the pattern in Figure 1(a) cannot be manufactured with LELE because the pattern cannot be decomposed into first and second exposures without violating the minimum spacing requirement; whereas, the pattern of Figure 1(b) cannot be manufactured with SADP because the pattern cannot be decomposed without violating the minimum spacing requirement in the trim exposure. Patterns that are not manufacturable with MP are referred to

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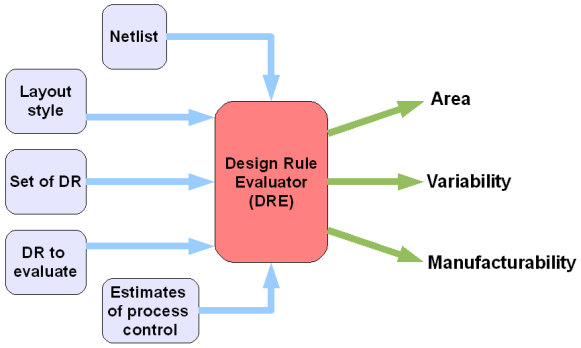

Figure 3. Overview of the Design Rule Evaluator (DRE) [1].

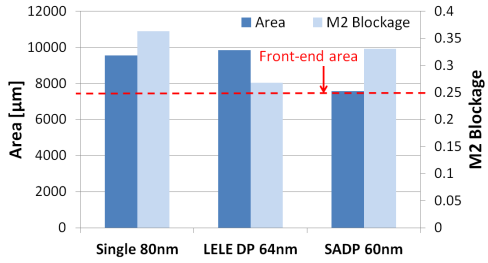

Figure 4. Total cell area and M2 blockage results for M1 patterning: 60nm pitch with SADP and 64nm with LELE DP with conservative rules to avoid conflicts compared with 80nm pitch with single-exposure 1D patterning.

as MP conflicts. Failure to reach a conflict-free layout decomposition solution is one of the biggest technical challenges for adopting MP.

MP conflicts can be dealt with either during technology development by a correct-by-construction approach or post-layout design enablement by a construct-by-correction approach. In the correct-by-construction approach, geometric constraints – known as design rules – are imposed on layout to prevent conflicts. In the construct-by-correction approach, forbidden layout configurations are detected in the layout and are removed using automatic or manual fixing. The correct-by-construction approach and its effectiveness will be examined in Section II. Similarly, the construct-by-correction approach will be examined in Section III.

Overlay is the positional accuracy with which a pattern is formed on top of an existing pattern on the wafer [12]. In MP, overlay effectively translates into CD variability [13,14] as illustrated in Figure 2. Meeting the requirements for overlay control is believed to be another big challenge for deploying MP technology [15]. In Section IV, we will show how design information can be used to reduce the overlay-control requirement for MP.

Since DP has two separate exposure and etch steps, two independent critical dimension (CD) populations exist: one for shapes formed by the first exposure/etch step and another for shapes formed by the second exposure/etch step as depicted. Overlay error between gates of different exposure/etch steps is a contributor to this bimodality problem. An obvious consequence of bimodality is a larger within-die CD/delay variation [14,16]. Another serious consequence of the bimodality problem is the loss of spatial correlation. [17] examines timing problems that arise due to bimodality and proposes placement perturbation to mitigate them.

II. Role of Design in MP Technology Development

One way of dealing with MP conflicts at the technology-development stage is through a correct-by-construction approach. In this approach, MP design rules (i.e., coloring and overlay rules) are imposed on standard-cell layout generation and conservative MP design rules are used at the design/cell interface to avoid any possibility of a conflict after placement and routing. Designing

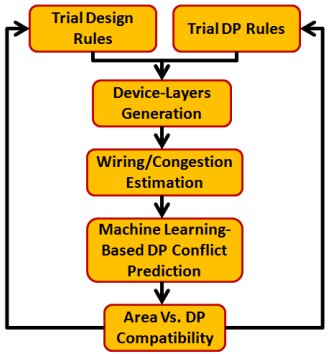

Figure 5. Overview of our methodology for exploration of DP design rules.

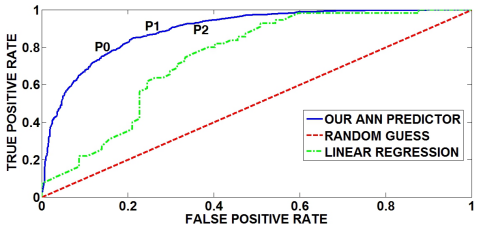

Figure 6. ROC curve for our ANN model compared with those of linear regression and random guess.

with MP rules is believed to be a hassle and conservative rules are expected to have a significant cost in terms of area [18,19]. Additionally, in a previous work [1], we develop a framework for design rules evaluation, DRE (see Figure 3), and use it to evaluate the density impact of using conservative MP rules for standard-cell layout generation that would virtually eliminate any possibility of MP conflicts. The results are depicted in Figure 4. Even after scaling the M1 pitch from 80nm to 64nm, LELE DP with conservative rules lead to a larger layout area compared to single-exposure patterning. SADP with conservative rules and M1 pitch of 60nm achieves near-minimum area (i.e., near-front-end area) but fails to mitigate the M2 blockage (i.e., parts of M2 that are used within cells and blocks design-level routing).

An alternative method is to construct layouts with design rules that would bring MP conflicts down to a manageable number, making manual or automated fixing possible. For this approach to be examined, a method for studying the effect of rules on MP conflicts as well as layout area is needed. An explicit layout generation based approach such as [20], though possible, is cumbersome, inflexible and not generalizable for the purpose of assessment of the inherent "DP-friendliness" of rules.

In our previous work of [21], we propose a novel framework: DP DRE for evaluating DP rules in combination with layout rules efficiently and at the exploration stage of technology development. The methodology flow is depicted in Figure 5. Given trial design rules and DP rules, the first step is to generate the layout of front-end layers. This is performed using DRE, which can generate front-end layers accurately and efficiently (< 1 hour for a 100-cell library). Next, wiring-layers layout are estimated and congestion is predicted using a fine-grained probabilistic wiring-estimation method. This estimation is fast and flexible and eliminates the evaluation dependency on the router's specificities. In the last step, the presence of DP conflicts in the layout is predicted using a machine-learning approach. In particular, fine-grained estimates of wiring congestion and estimates of layout features (e.g., line-ends and L and T-shapes) and their distribution are given to a machine-learning model, a feed-forward back-propagation artificial neural network.

The machine-learning model was tested and compared with real data. The model achieves a positives-detection rate of 82.5% and a

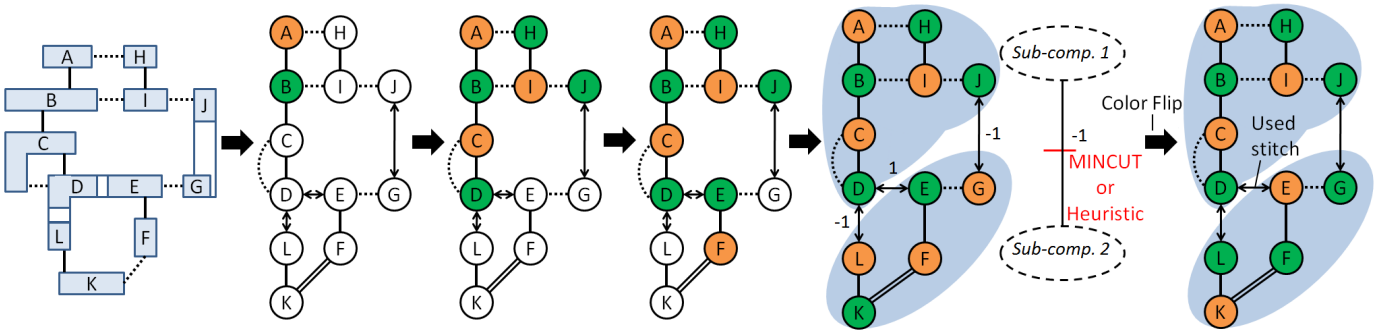

Figure 8. An illustrating example showing each step of the coloring process for an isolated region of the layout: (1) construct conflict-graph with violation-arcs and stitch-arcs, (2) identify connected components and sub-components – i.e. connected components in graph when stitch arcs are ignored, (3) pick a violation-arc with preference to more critical violations and color its two connected nodes with different colors, (4) add connected arcs of newly colored nodes to first-in-first-out queue to be processed next, (5) repeat steps 3 and 4 until all arcs in sub-component are processed, (6) pick a stitch-arc at random and perform coloring of new sub-component as described before, (7) flip colors of sub-components to reduce/minimize stitches – using either a heuristic algorithm or a minimum-cut formulation/algorithm.

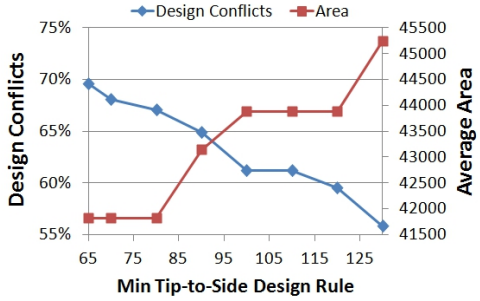

Figure 7. "Design Conflicts" and area of benchmark designs for range of M1 minimum tip-to-side design rule.

negatives-detection rate of 80% (see Figure 6).

We use the methodology to conduct rule-exploration studies. In one experiment, we study the conflict/area trade-off with changing the minimum tip-to-side design rule for M1. We define a metric for DP-compatibility of design layouts, "Design Conflicts", which takes into account conflicts within standard-cells as well as across their boundaries post-placement. For a same-color spacing fixed at 130nm (2× min spacing for all three same-color rules) and for each rule value, "Design Conflicts" and area of benchmark-designs are depicted in Figures 7. Interestingly, a non-linear trend is observed in both cases for conflicts as well as design areas, which reveals optimization opportunities. For example, increasing the tip-to-side rule from the original value of 65nm to 80nm can reduce "Design Conflicts" with almost no area increase.

With design support, more radical changes in double patterning process are also possible. For instance, in [22], we have proposed a single (critical) mask double patterning technology which generates the second exposure by a "shift" of the first exposure but requires tweaks to the design rules and layouts.

III. Design Enablement of Multiple Patterning

In this section, we briefly discuss two aspects of design enablement of DP: decomposition of layout into two exposures and incremental layout legalization to resolve non-decomposable layouts. Specifically, we review prior art and present our work from [24] on MP layout decomposition and post-layout automated fixing of MP conflicts.

A. Layout decomposition

Layout decomposition is essentially a color-labeling problem [23]. The difference from the labeling problem of graph theory in a MP process with repeated litho-etch steps (i.e., LELE) is that a single layout polygon can be split and formed by different exposures. The location where different masks join is called a stitch. Although stitching complicates the labeling problem and stitches may be a cause for yield loss, stitching can remove many MP conflicts without the need for changing the original layout. In a self-aligned process (i.e., SADP), layout decomposition is a more difficult problem. Although stitching is not allowed in this case, polygons may be formed by the composite of the first-exposure mask (a.k.a. mandrel) and trim mask. SADP layout decomposition cannot typically reach a conflict-free mandrel and trim masks for conventionally drawn bi-directional layouts.

MP layout decomposition, has been the topic of extensive research: rule-based coloring and stitching at pre-defined location [25,26], ILP-based coloring with stitch minimization as an objective [27]–[29], minimum-cut-based stitch minimization [30], and heuristic-algorithm-based with multiple objectives including stitch minimization [31]. Most works perform segmentation of the layout into rectangles prior to coloring. This segmentation has many drawbacks [24]. First, it complicates the problem as it forces the consideration a lot of extra stitch locations that should never be used. The second drawback of segmentation is that it forces the method to use a single spacing-rule value. It makes the handling of multiple same-color rule values difficult.

We follow a different approach for the DP coloring than prior works. Specifically, we use DR-dependent projection to determine the features that may cause DP conflicts and their actual, possibly non-rectangular, shapes (as in [29]). We then formulate the problem as a labeling problem. We perform the coloring in $O(n)$ and follow with color-flipping to reduce/minimize the number of used stitches (details in Figure 8). We offer two methods to perform this color-flipping: a $O(n)$ heuristic algorithm and $O(n \log(n))$ minimum-cut-based algorithm that reaches an optimal solution. In our method, all candidate stitches that may be useful are automatically identified and are reduced by the algorithm. Because we use all candidate stitches, our method guarantees a conflict-free coloring solution when the layout has no conflicts that are unresolvable with stitching (a.k.a. native conflicts).

Although coloring cannot resolve a native conflict, deciding what features go on the same color can affect the efficiency of the conflict removal (see Figure 9). To take advantage of this observation, we design our layout-coloring algorithm to allow for preferred coloring and be aware of violation criticality.

We tested our DP coloring method on the polysilicon and M1 layers. For dense M1 layouts, our heuristic-based flipping leads to at most 3.8% larger number of stitches than that achieved with the our MINCUT-based flipping, which has the same run-time complexity as [30], and can be up to 167× faster. layouts presented in and compare the results. For less dense layouts polysilicon layouts, our

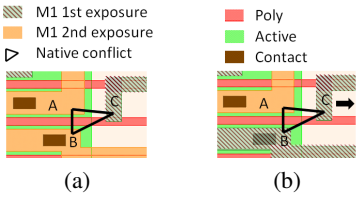

Figure 9. Layout-coloring of features of an odd cycle can affect the efficiency of conflict removal. In (a), the conflict is on M1 between shapes A and B and can only be fixed if the gates are spaced apart and area is increased; in (b), the conflict is on M1 between shapes B and C and can be fixed by moving C in the direction of the arrow without increasing area.

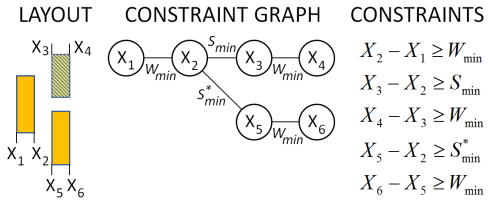

Figure 10. Example of x-direction constraint graph construction and constraint definition for a double-patterned layer. W_{min} is the minimum width rule, S_{min} is the side-to-side different-color spacing rule, and S^*_{min} is the side-to-side same-color spacing rule.

heuristic-based flipping is up to 80× faster than the ILP-based approach of [27].

B. Layout legalization

Prior works on post-layout MP conflict removal [33]–[35] generally formulate the problem as an integer linear program – ILP (except [35]), which is excessively time-consuming to solve. Moreover, they do not perform a layout legalization in a general context and, therefore, the removal of one conflict may create new conflicts in other parts of layout or design-rule violations at other layers. Previous works in this area also uses layout-segmentation, which lead to some drawbacks in addition to the ones discussed earlier.

We propose post-coloring conflict removal and layout legalization simultaneously across multiple layers through edge-based layout compaction. In our method, compaction is formulated as a linear program (LP) with *minimum perturbation problem*, unlike [35] that uses minimum-area metric for compaction. The proposed methodology allows the layout designer to design with conventional single-patterning layers and design rules, masking the complexity of dealing with double-patterning layers and requirements.

We represent the colored layout as a constraint graph where nodes correspond to the layout edges and arcs correspond to design rules that need to be met between any two layout edges. Arcs are assigned weights that correspond to the values of rules as illustrated in Figure 10. Layer-to-layer connectivity is maintained through rules between the layers, which are represented in the graph by arcs between nodes of the different layers.

We define mask layouts of any multiple-patterned layer as stand-alone layers. Same-color spacing rules, between features of the same mask, including complex spacing rules, are mapped into arcs between the nodes of the stand-alone mask layer in the constraint graph. Rules that define the interaction between the two mask layouts (e.g., minimum overlap length) are mapped into arcs between the nodes of the two stand-alone mask layers. For the interactions across different layers in the stack (e.g., M1 and contacts), we define any double-patterned layer as the union of its two mask layouts and map across-layers design rules into arcs between nodes of the union layers. As is common in layout compaction, the two-dimensional minimum perturbation problem is simplified by solving the one-dimensional problem successively (in x and y directions). We formulate the 1D minimum perturbation problem as a LP.

Table I
DP CONFLICT-REMOVAL RESULTS WITH FIXED/UNFIXED AREA ON CELLS AND MACRO LAYOUTS FROM A COMMERCIAL 22NM LIBRARY.

	Original		w/ Fixed Area	w/ Area Increase	
Cell	**N. Area**	**Conflicts**	**Conflicts**	**Conflicts**	**Area Increase**
LCB	1	**1**	**0**	-	-
latch1	1.6	**3**	**2**	0	9.1%
oai	1.6	**2**	**0**	-	-
scan latch	2.3	**5**	**3**	**0**	6.2%
xor	2.4	**2**	**0**	-	-
latch2	4.3	**19**	**8**	**0**	3.3%
nand4	4.7	**4**	**0**	-	-
latch3	5.3	**4**	**3**	**0**	5.4%
nand3	6.7	**7**	**0**	-	-
LCB ctrl1	13.7	**13**	**7**	**0**	8.3%
LCB ctrl2	50.3	**53**	**31**	**0**	9.1%

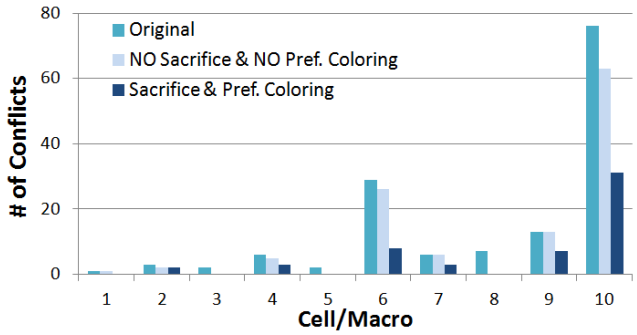

Figure 11. Number of conflicts with the fixed-area flow for the different cell and macro layouts showing the effects of using preferred coloring (see Figure 9) and the possible sacrifice of redundant contacts and M1 pin segments.

In actual layouts, several conflicts on the M1 layer are caused by segments that are added to cover redundant contacts/vias or to maximize the pin-access region. Since these are *not absolutely required*, we allow the *possible* sacrifice of redundancy and extra pin segments to improve the results of the DP conflict removal. Specifically, we pre-process the layout prior to the coloring to remove potential sacrificial segments. During the legalization and conflict-removal, these features are recovered whenever possible without creating any new violations by adding recommended rules between the new segment edge and the initial edge.

We tested our MP conflict removal framework for LELE DP on the M1 layer of a commercial 22nm standard-cell and macro layouts (double-patterning for M1 was assumed). The results are given in Table I. For standard cells, the method removes all DP conflicts without any area increase in five out of nine cells; for the remaining four cells, the method still removes all conflicts with a 6% average increase in area. For macro layouts, the method reduces the number of DP conflicts from 13 to 7 conflicts for one macro and from 53 to 31 conflicts for another without any increase in area. When the area is allowed to increase, the method removes all remaining conflicts with an average area increase of 8.7%. The runtime of the entire flow for the largest macro layout (460 transistors) is less than one minute in real time (< 2 seconds CPU time).

Preferred coloring and possible sacrifice of non-crucial layout features (via/contact redundancy and pin segments) makes conflict removal more effective. To quantify the impact of these two methods, we run our framework with fixed area and while enabling or disabling the two methods (results in Figure 11). Up to ∼4X less conflicts can be achieved when the methods are applied for standard cells and up to ∼2X less conflicts can be achieved when the methods are applied for macros.

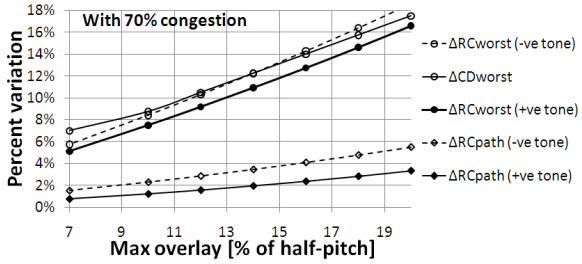

Figure 12. Plots of average and worst case CD and C variations versus requirement of maximum overlay with 70% congestion in positive and negative DPL.

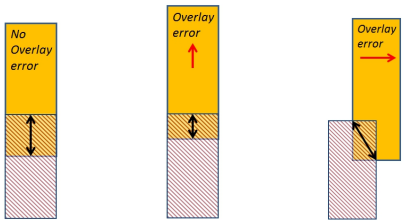

Figure 13. Example of a stitch in a vertical line (a), a possible failure with overlay error in Y direction that may occur after lineend pullback (b), and a possible failure with overlay error in X direction due to narrowing (c).

The way we formulate the conflict-removal problem permits the extension of our methodology to layout legalization for TP and SADP. To apply the methodology for TP, TP coloring is performed instead of DP coloring and the three mask-layouts of any triple-patterned layer are treated as three stand-alone layers. All TP rules that define the interaction between these three mask-layouts (i.e., spacing and overlap rules) are mapped into constraints between the stand-alone layers. And, rules that define the interactions between the triple-patterned layer as a whole and the top/bottom-level layers (e.g., contacts/VIA layers) are mapped into constraints between edges of the union of the three mask-layouts and the edges of the top/bottom-level layers. In a similar fashion, the methodology can be applied for SADP; all that is needed is a SADP-coloring method as [36] and a set of design rules to ensure SADP compatibility of the layout as in [37].

IV. Role of Design in MP Process Control

Overlay control is the most critical process challenge for DP [38]. In [39], we electrically evaluate overlay errors for metal-layers DP to *study relative importance of different overlay sources and interactions of overlay control with design parameters* and derive methods to alleviate within-layer overlay problem in DP. In addition, we explore processing options including positive-tone dual-line (overlay error affects metal spacing and hence capacitance only) and negative-tone dual-trench (overlay error affects metal width and hence both resistance and capacitance) processes.

Overlay induced electrical errors tend to average out across wires (due to directional nature of overlay), nets (which can be further emphasized by explicitly alternating or "swizzling" colors during decomposition) and critical paths. Even though overlay error translates into CD variation in DP, our conclusion (see Figure 12) is that *overlay requirement can be relaxed if electrical variation is the base for determining the requirement* rather than the conventional CD variation metric. Moreover, the work concludes that *positive process is preferred over negative process from an electrical perspective* as long as width and spacing are equal for metal layers. The expected worst-case electrical variation for a path is much smaller for the case of positive-tone process than in the case of a negative-tone process.

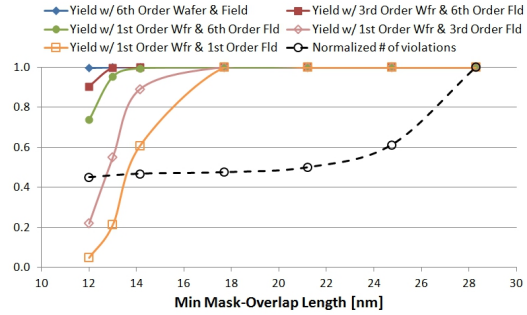

Figure 14. Interaction between overlap-margin rule and various overlay control strategies. Metrics are yield and number of DP conflicts in the design.

Design rules that define interactions between different layers (e.g., metal overhang on via rule) or different mask-layouts of the same layer (e.g., mask overlap) effectively serve as guard band for overlay errors. For defining these rules during process development, a prediction of the yield loss due to overlay is needed. If overlay is characterized entirely as a field-to-field error, then the probability of survival (POS) for the die is equal to the POS of the most overlay-critical spot in the layout, say k. On the other extreme, if overlay is characterized entirely as a random within-field variation, then POS of the die is k^n, where n is the total number of critical spots in the design. Hence, depending on the overlay characteristics, rules can either be grown to suppress yield loss or shrunk to reduce the layout area.

In [40], we offer a general framework for exploring the interaction between design rules, overlay characteristics, and overlay-modeling options. We develop a model for yield loss from overlay that considers overlay characteristics including the residue after overlay correction and the breakdown between field-to-field and within-field overlay. The proposed framework is the first of its kind and it can be *applied during process development to better define overlay-related design rules* and *to project the overlay requirement of the process* thereby informing alignment strategies in the process. The framework was used in this work to explore DP and overlay-related rules for the M1 layer. The framework is more general, however, and can be used to explore other inter-layer overlay rules, for different MP technologies, and at other layers.

As an example, consider the overlap-margin rule which is triggered whenever a stitch is introduced between the different mask layouts of the same layer. One of the main reasons for yield loss associated with stitches is overlay errors between the first and second exposures in DP. Therefore overlap margin has a direct impact on yield. Consider for example a stitch in the center of a vertical line as shown in Figure 13. An overlay in the Y direction may result in an insufficient mask overlap and cause an open defect after line-end pullback; an overlay in the X direction may cause the wire to become too narrow at the stitch leading to failure. In addition, the overlap-margin rule affects the DP-compatibility of the layout. The larger the overlap length is, the lesser candidate-stitch locations the layout will have. Hence, while a large and conservative overlap-length rule is likely to inhibit most yield loss of stitches caused by overlay, such overlap length may result in excessive re-design efforts and area overhead to ensure the layout conforms to DP.

We use the framework to study the effects of the minimum overlap-margin rule in LELE DP process at the 14nm node. The results, depicted in Figure 14[1], show the strong interaction between the rule value and overlay-control options as well as the overall impact on yield and DP-compatibility. Higher order overlay modeling require

[1]The number of DP-spacing violations are normalized with respect to the case with the largest number and DP coloring of the layouts was performed using a minimum same-color spacing of 1.5× the half-pitch.

more overlay samples to calibrate models for overlay compensation but can result in reduced residual overlay error. Interestingly, few nanometer changes in the rule value may allow the use of a less stringent overlay model without significant impact on DP-compatibility. For example, increasing the minimum mask-margin length from 12nm to 16nm would allow the use of a first-order wafer/first-order field-level overlay model instead of a sixth-order wafer/sixth-order field-level model with negligible increase in number of DP violations. This can directly translate to significantly reduced overlay metrology and alignment costs in the production process.

V. Conclusions

One of the biggest changes in the lithography landscape is multi-patterning lithography which will be the key enabler of scaling (especially given the significant process challenges in other next generation lithography alternatives such as EUV). Explicit engagement of design throughout the technology lifecycle (technology development, design enablement and process control) has turned out to be indispensable in adoption of multi-patterning affordably.

In this paper, we have given a few example of design-technology co-optimization in context of double-patterning:

- DP-DRE: a framework for optimization of double patterning design rules during technology development.
- Enablement of double patterning in design flows through fast layout decomposition and automatic legalization of layouts.
- Design-aware optimization of overlay control requirements and alignment strategies.

The semiconductor industry is likely to see several radical changes in the fabrication and device technologies in the next decade. Conventional after-the-fact changes to design methodologies and tools to fit technology leads to wasted effort and under-utilization of technology and delays its adoption. Design-assisted technology scaling can help dramatically reduce costs and time of technology development and adoption.

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