Configurable I/O Integration to Reduce System-On-Chip Time To Market:DDR, PCIe examples

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Abstract— The availability of protocol features with iterative configurability is central to the successful adoption of reusable IP in SoC development. However, the promise of ultimately shrinking the SoC development TTM whilst also allowing greater resourcing efficiency can only be realized with a comprehensive approach to delivering the software, digital and analog components of the protocol to the SoC top level integration as IP subsystems with the correct integration views. This talk will discuss quantitatively how the combination of configurability, quality and integration at the IO protocol can systematically reduce the SoC development and resource plan. It will be demonstrated with examples for DDR and PCIe IO protocols as well as examples from application specific SoC's.

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