

AIR (Aerial Image Retargeting) : A Novel Technique for In-Fab Automatic Model-Based Retargeting-for-Yield.

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Abstract—In this paper, we present a novel methodology for identifying lithography hot-spots and automatically transforming them into the lithography-friendly design space. This fast model-based technique is applied at the mask tape-out stage by slightly shifting and resizing the designs. It implicitly does a similar functionality as that of the Process Window OPC (PWOPC) but more efficiently. Being a relatively fast technique it also offers the means of providing the designer with all the design systematic deviations from the actual (on-wafer) parameters by including it in the parameter-extraction flow. We applied this methodology successfully to 28-nm Metal levels and showed that it efficiently (better quality and faster) improves the lithography-related yield and reliability issues.

Index Terms—RET, Resolution Enhancement Techniques, PWOPC, Optical Proximity Correction, LFD, lithography Friendly Design, DFM

I. INTRODUCTION

DURING the past two decades, Optical Proximity Correction (OPC) [1], [2] has been evolving from rule-based mask correction to Model-Based OPC (MBOPC) targeting the geometrical design fidelity and achieve the designers geometrical design intent on wafer. Later on, OPC has also provided the means of preventing catastrophic Process Window (PW) failures on wafer through Process Window OPC (PWOPC) [3], [4] methodology, where the cost function used in OPC correction is not only the Edge Placement Error (EPE) between the design and the wafer print image but also includes the worst-case scenarios of the on-wafer printing within the process window variations. All these OPC techniques fall under the category of traditional OPC, where the design is fragmented into small fragments and each fragment can move independently to improve the design fidelity based on the its cost function. Another approach in doing OPC is using Inverse Lithography Techniques (ILT) [5] to get the final mask (both mask and SRAFs) by using the aerial-image fidelity as the cost function in an inverse-lithography methodology. ILT results in better yield, but on the expense of a dramatic increase in the computation power and the mask complexity.

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Now, with the adoption of PWOPC as an essential component of the mask-tape-out flow, the wafer data is showing an increasing systematic deviation from the design-intent [6], which forces the designers to unnecessarily use wider guard-bands (which should account only for random variations) to take this systematic deviation into account. If this systematic deviation can be modeled efficiently (i.e. can be taken into account using a computationally fast but robust technique), it would allow the designers to consider this effect into design. The challenge is that the parametric extraction tools have no access to how the final design would look like on wafer.

In the design process, it is desirable to include all systematic deviations accurately using fast models. This is very important for the yield rampup and the final product availability and maturity. The current approach for including the design deviations is shown in figure (1), where all geometric-based yield enhancing re-targeting is included before the deviation in the electrical parameters is fed-back to the simulation. The problem with this approach is that 1) it does not include all the design-deviations that happens during the mask tape-out. For example it assumes perfect etch-process correction, which is a good approximation, but yet not perfect. 2) Also it does not include the PWOPC retargeting which can reach a value of few nanometers. The problem with PWOPC retargeting is that it cannot be included without running full OPC and full verification, which is very time consuming. Figure (2) shows a more accurate approach to include all the design-deviations in the mask-tapeout flow, but unfortunately it is very computationally intensive. It is of great benefit to develop a technique that allows the reproduction of the Lithography friendly retargeting while being much faster than PWOPC so that this design deviation can be included in the design process.

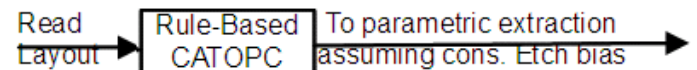


Figure 1. A schematic diagram explaining the current extraction flow.

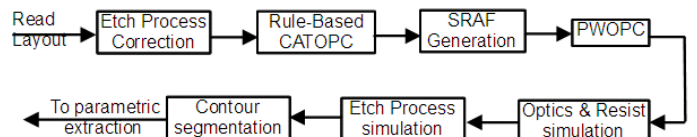


Figure 2. A schematic diagram of an ideal extraction flow.

In this paper we are introducing a novel and fast model-based retargeting technique called Aerial Image Retargeting (AIR). It is based on the optical simulation (Aerial Image) of the OPC target. This technique is 1) capable of improving the yield by automatically transforming the Lithography hot-spots into Lithography-friendly designs during mask tape-out. 2) Offers improving the mask tape-out preparation time. 3) Fits better in the flows targeting the modeling of the systematic design-deviations at the mask tapeout phase. The proposed flow is shown in figure (3), where AIR output is a lithography-friendly target that the OPC is capable of converging safely to it (i.e. no deviation between the on-resist-image), then without performing any the exhaustive simulations for OPC, the AIR output is passed to the etch simulator to compute the final (on-wafer) results, which can then be supplied to the parasitic-extraction tools to model any systematic deviation in the mask-preparation flow. This will enable the designers to tweak their designs for the best circuit performance. Another advantage is that the output of this flow is already segmented (i.e. not contour-like), which suits better the parasitic-extraction tools.

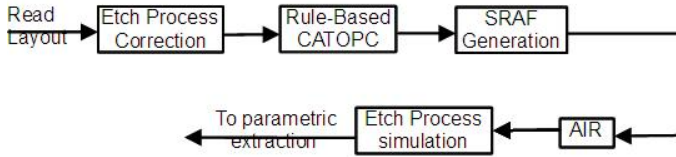


Figure 3. A schematic diagram explaining the proposed fast and accurate AIR-Based extraction flow

In section II, we will be reviewing the current Back End design re-targeting approaches, followed by the explanation of the novel Aerial Image Retargeting (AIR) concept in section III. Section IV contains the testing results and showing the yield improvement when AIR is applied and how it can be used modeling the systematic deviations in the mask-tape-out flow.

II. DESIGN RE-TARGETING APPROACHES

Rule-based CATastrophic OPC (CATOPC) has been applied as an essential step during the mask tape-out flow for all sub 100nm nodes [7]. The purpose of CATOPC is to re-size non-lithography friendly designs so that the design geometries are shifted to a more Lithography-robust design space. This is applied using a table-driven approach, where every design width-pitch combination gets the necessary bias needed to shift towards a more Lithography-safe design space. Figure (4) shows an illustrative example of CATOPC used in the industry. Such re-designing information is provided to designers implicitly in their models and it is transparent to the designer.

However, rule-based CATOPC and the current extraction flow are facing a serious challenge. First, due to the increased sensitivity of the designs to their proximity, the determination of the amount of resizing needed is no more dependent only on the direct neighboring design shapes but also on the shielded shapes. Which makes the width-pitch relations not sufficient to describe the required design biasing. Second, as the CATOPC

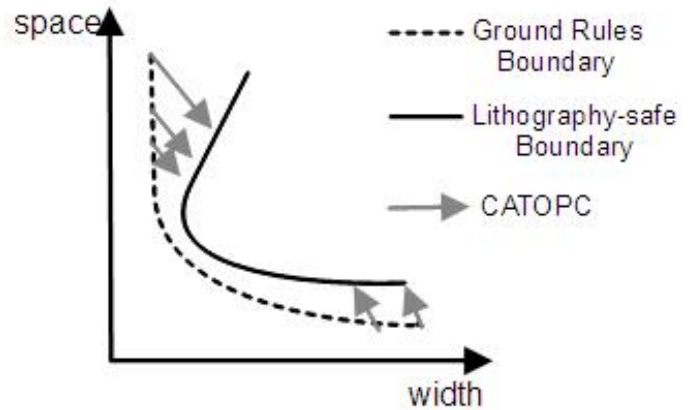


Figure 4. An illustrative diagram explaining the CATOPC process and how it drives OPC targets to lithography-friendly regions.

rules are extracted from 1D through-pitch patterns, they are not necessarily the best for 2D complex designs.

All this makes PWOPC inevitable, where all the proximity effects due to shielded designs or 2D design complexities are corrected-for (re-sized) during OPC using a model-based technique. However, this is on the expense of adding the systematic deviation discussed in the previous section. There are several re-targeting approaches in PWOPC [8], [9], but unfortunately, all of them require performing full PWOPC in order to extract the on-wafer design, which is very computationally intensive and cannot fit efficiently into the parameter extraction flow. One good thing is that PWOPC deviations are in the order of few nanometers in the 32nm and smaller nodes compared to the rule based CATOPC which can deviate more than 10 nm. However, the accuracy level dictated by ITRS and market competition requires that this deviation be modeled.

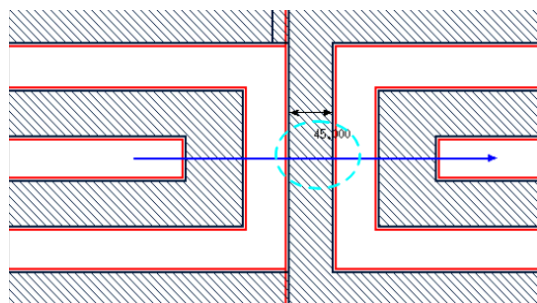
In the next section, we are proposing a novel technique that provides 1) an accurate and fast model-based approach to do PW-based-retargeting of non-lithography-friendly designs to improve the yield, 2) provides the possibility to improve the mask-tapeout flow Turn-Around-Time (TAT), 3) being fast, this technique can be efficiently integrated in the parasitic-extraction flow and included in the simulation models.

III. AERIAL IMAGE RETARGETING (AIR) CONCEPT

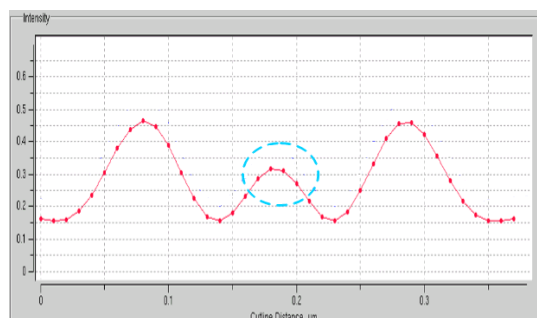
In the previous section we concluded that an efficient (accurate and fast) model-Based OPC target correction is needed to achieve better lithography-Friendly targets. This technique needs to be accurate and computationally efficient so that it can be effectively used in the OPC production environment. Also, if this approach can catch most of the retargeting needed to have a PW-friendly OPC target, then this would enable two important benefits. First, on the fab's side, reducing the computation needed for better yield. This is mainly because the post-AIR OPC target is more lithography-friendly and accordingly a simpler OPC recipes are needed. Second, it is possible to model the PWOPC systematic deviation between the design intent and the final on-wafer characteristics.

Aerial Image Retargeting (AIR) identifies the weak PW designs (hot spots) and classifies them into width sensitive

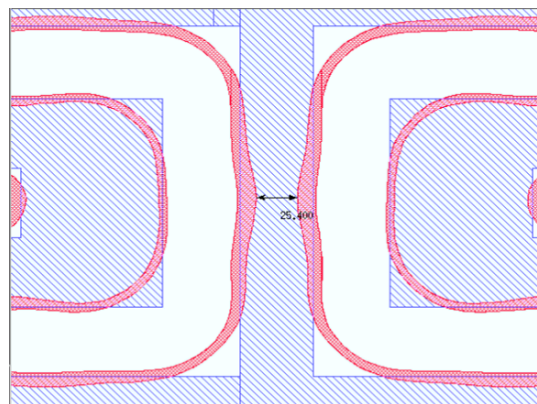
and space-sensitive. This is based on evaluating the optical signature of the design (which also includes the proximity effects). The optical signature (also known as the aerial image signature, because the resist effects are not included in it) is computed for the OPC target (i.e. it's a pre-OPC simulation). Then the design is divided into small fragments (similar to what happens in regular OPC), but their movement (retargeting) is extracted from a look-up table. This look-up table is developed by the DFM and OPC Engineers after training the recipe on a wide and yield-challenging design space. This movement is a change in the OPC target and should not be confused with the OPC where the target fragments move to minimize their Edge Placement Error (EPE) between the printing image and the design intent.



(a) Hot-Spot position and the critical direction.



(b) Aerial Image distribution along the critical direction.



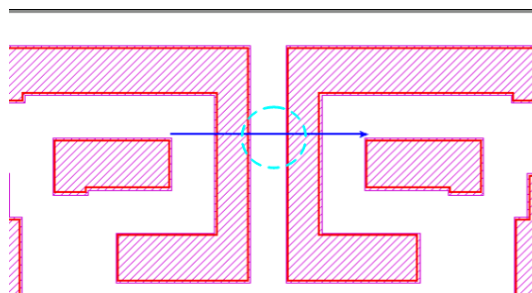
(c) Post-OPC through PW verification of the design showing bad soft pinching.

Figure 5. Analyzing hot-spot (1).

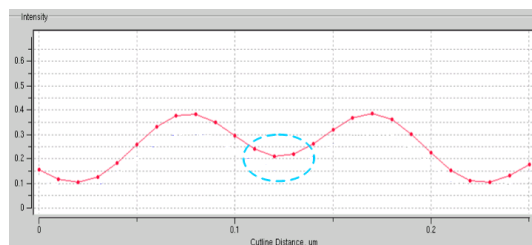
Similar to the rule-based CATOPC, where the resizing value is determined by the width-space combination, the AIR resizing value is coded in a table based on the Aerial Image signature using parameters like I_{max} , I_{min} (Maximum

and Minimum optical intensity along the simulation site respectively), Aerial Image Slope, as well as the optical field curvature at the simulation site. This adds several degrees of freedom and is more capable of identifying Lithography hot spots based on the Optics which is the root cause of Lithography limitations. Accordingly, even if the design is 2D it can be fixed independent of all different proximity effects and any surrounding designs.

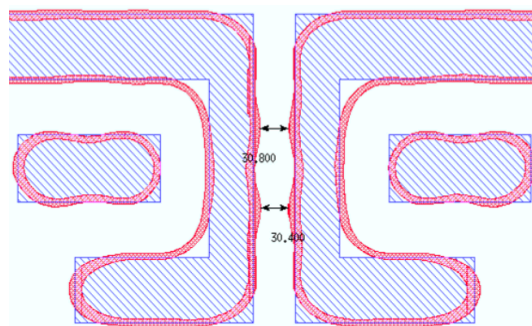
Figures 5 and 6 show two different hot-spots (with the same width-space combination), but in the same time they exhibit a radically different post-OPC yield issues. It is obvious that both designs exhibit radically different aerial image signature, which we claim to be the origin of the lithography-yield issues. We propose using the aerial image signature in capturing and classifying lithography hot-spots because they can generically identify the lithography-related yield issues better than the geometrical description techniques. Moreover, using aerial image signatures in capturing hotspots is much faster than relying on the full model-based lithography hot-spots capturing techniques (i.e. doing full OPC+lithography simulation).



(a) Hot-Spot position and the critical direction.



(b) Aerial Image distribution along the critical direction.



(c) Post-OPC through PW verification of the design showing soft bridging.

Figure 6. Analyzing hot-spot (2).

To test the assumption above, we ran OPC on a chiplet that is designed to contain all the lithography-challenging designs.

Then we mapped the PW worst widths (pinching) and spaces (bridging) to the aerial image maps (similar to width-space maps in figure1, but with I_{max} and I_{min} instead). Figure 7 shows the AI map for the width-sensitive designs, where each contour represents hot-spots having the same measurement through the process window, the smaller the number gets (on the legend) the worse it is from a lithography (yield) perspective. So for example in the figure the point (0.3,0.14) represents the worst design signature and results into severe pinching, then as the designs signatures starts to get away from this point, the failure severity starts to get better. Accordingly, we can conclude that for such map the designs with aerial image signature closest to (0.3,0.14) need a large positive bias (retargeting) to counter the effect of the bad initial design. One important observation from figure (10) is that the contours follow a monotonic behavior, which indicates that the AI signature can solely identify the PW weak areas. Moreover, using the aerial image contours curvature and the aerial image slope would add extra degrees of freedom in describing the PW more accurately and allows better separation between the both width and space weak designs.

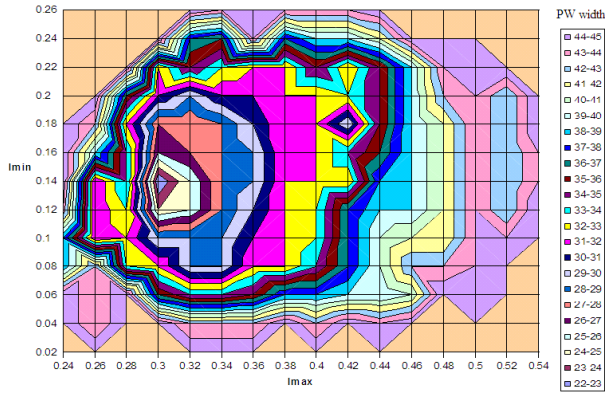


Figure 7. The PW Contours Verification width errors mapped on the I_{max} - I_{min}

It is of particular interest to see if the aerial image contrast could alone serve as a single variable for identifying weak PW designs.

$$C = (I_{max} - I_{min}) / (I_{max} + I_{min}) \quad (1)$$

In figure 8, we are plotting the contours of constant contrast overlaid on the I_{max} - I_{min} map shown earlier, while the color coding represents the severity of the hot-spot. It is very evident that the contrast cannot describe the weak PW areas by itself.

AIR is thus capable of doing a Lithography-aware retargeting of the design that is very similar to that done during PWOPC (as PWOPC sacrifices the design fidelity (EPE) if the design is suffering from poor PW performance). However, AIR is capable of doing this retargeting 1) As a pre-OPC step, i.e. not linked to OPC, 2) Very computationally efficient (consumes less resources than that needed by a single nominal OPC iteration), 3) fits better in the parasitic-extraction flow and the modeling of the systematic PWOPC deviation from the original designs presented in figure (3).

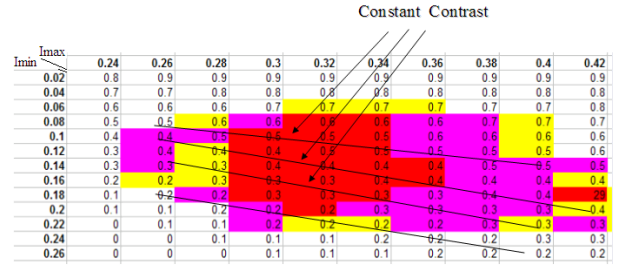


Figure 8. Mapping the contours of constant contrast on the I_{max} - I_{min} map (while the severity level is color coded). It is shown that for the same contrast value passes through different regions of the map that goes between very critical and non critical.

IV. AIR RESULTS

In our testing of AIR, we bench-marked AIR against a 28nm flow for metal level. A generic AIR recipe (table) was generated based on the known problematic designs and interpolation was used to guess the proper biases for missing data. The AIR recipe was also optimized for run-time optimization, where the simulations were only performed on edges that have a potential of bridging or pinching (i.e. relatively small width or space), as well as optimizing the simulation parameters for speed.

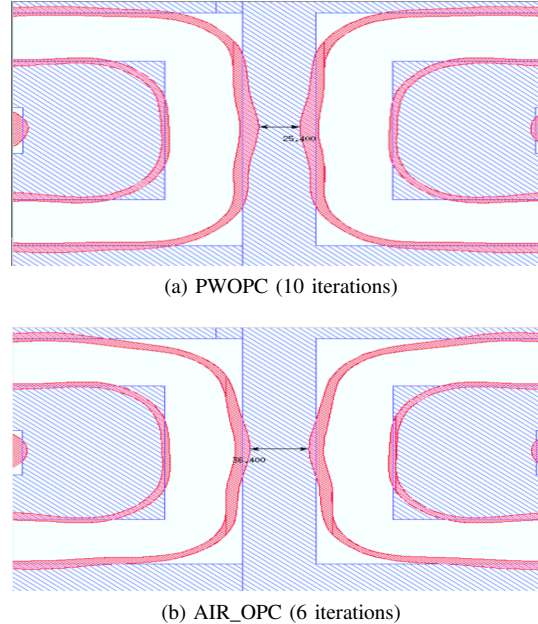


Figure 9. Comparing PWOPC recipe vs. OPC+AIR for hot-spot (1).

The results below are comparing the process window performance of regular PW OPC with 10 iterations against AIR followed by 6-iteration OPC. We are focusing not only on the huge quality improvement achieved by AIR (reducing the number of Lithography hot-spots), but also on the excellent improvement in the overall run-time of the Mask-correction flow, where the AIR OPC target is more lithography-friendly with better convergence due to the MEEF reduction accompanied by the auto-correction of the target.

In figures 9, 10, and 11, we are showing several designs comparing 10-iterations PWOPC through-PW verification against the through-PW verification of the AIR+6 OPC

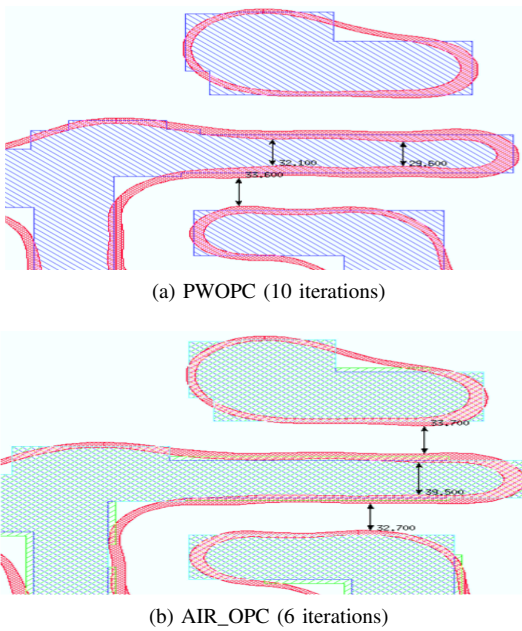


Figure 10. Comparing PWOPC recipe vs. OPC+AIR for hot-spot (2).

iterations. It is obvious that AIR automatically transformed the designs into lithography-friendly designs and OPC is capable of converging to the target more quickly.

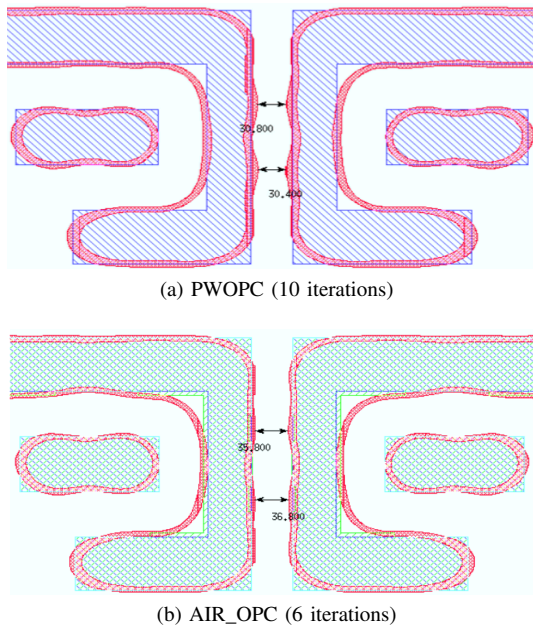


Figure 11. Comparing PWOPC recipe vs. OPC+AIR for hot-spot (3).

Figure 12 shows the distribution of the PW errors on the test chip, where the x-axis is the PW error measurement (the smaller the value the worse the design becomes from a lithography perspective) and the Y axis is the PW error count in the chiplet. It is evident from the distribution that the hot-spots distribution has improved a lot and many of the critical errors were translated to the safe range (i.e. transformed into lithography-friendly OPC targets).

Figure 13 shows the overall run-time of the mask tape-out flow with and without AIR, the introduction of AIR itself

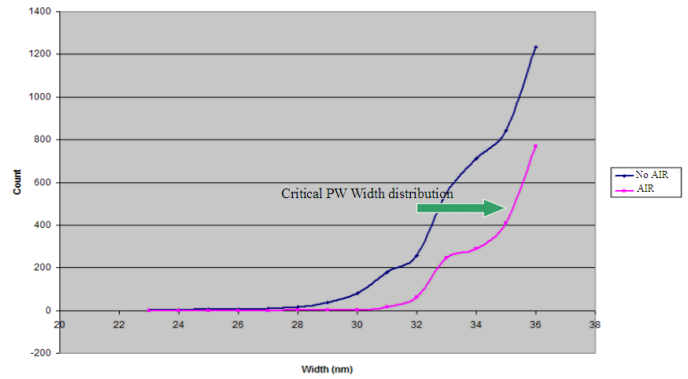


Figure 12. Hot spots Width distribution

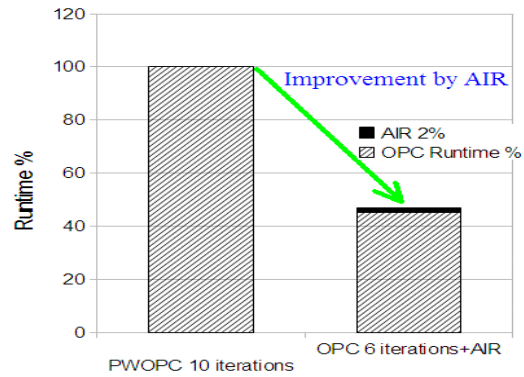


Figure 13. Comparing the Runtime of PWOPC and AIR+OPC

didn't consume more than 2% of the total run-time, while due to the clear benefit it gives on OPC, we can see up to 55% overall run-time reduction. The more appealing feature is presented in figure 14, where it is obvious that AIR was capable of reducing the hot-spots count from ~300 instance to only 5 in the test chip, which represents a significant yield improvement.

V. CONCLUSIONS

In this work, we presented a novel technique to identify Lithography hot-spots based on their Pre-OPC aerial image

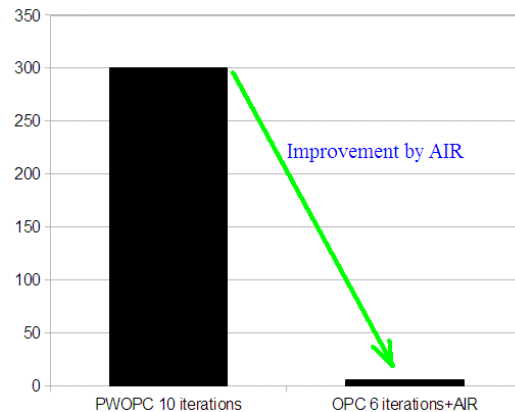


Figure 14. Comparing Hot-spots count between PWOPC and AIR+OPC.

signature and automatically fix them using a generic biasing recipe that is developed in parallel with the OPC recipe. It offers an excellent yield improvement. Moreover, this technique is very fast and computationally efficient. We also proposed using this novel approach in the parasitic-extraction flows to provide the designer with a more accurate final (on-wafer) information of all the design levels, while being faster in the same time. We tested the technique on a 28 nm metal level and it shows a huge yield improvement in addition to improving the OPC convergence, where our optimized AIR recipe does not consume more than 2% of the OPC flow.

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