Current Source Modeling for Power and Timing Analysis at Different Supply Voltages

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***Abstract*—This paper presents a new current source model (CSM) that allows to model noise on supply nets originating from CMOS logic cells. It also captures the influence of dynamic supply voltage changes on power consumption and cell delay. The CSM models n/pMOS blocks separately to reduce the complexity of model components. Compared with other CSMs, only two-dimensional tables are needed. This results in low characterization times and high simulation speed. Moreover, no re-characterization is needed for different supply voltages. The model is tested in a SPICE simulator. A reduction in transient simulation time by up to 53X was observed in the results, while the error in delay and current consumption was typically less than 3 percent.**

I. Introduction

Ensuring correct timing, signal integrity, and power consumption of an integrated circuit is an essential part in physical synthesis. To manage the complexity of modern ICs, each problem is tackled in a separate timing, noise, and power analysis. Mutual dependencies are traditionally treated in a quasi static manner. For instance, supply currents are first derived from a timing analysis and a power library, and are then used to estimate the IR drop. Thereafter, timing analysis is re-run for the lowered supply voltages using k-factor derating or other models such as in [17]. Power analysis itself not only requires efficient simulation algorithms for huge RLC power grid circuits [11], but also accurate delay and power models. Quite often, a logic cell is modeled as ideal switch with series resistor and parallel capacitor [16], or as time varying current source producing a triangular-shaped current [3]. Newer models, such as in [13], [21], or the current source models, ECSM and CCS, use multiple time points to model the current waveforms at power and ground (PG) pins [1], [18]. ECSM and CCS also model the cell output current in this way. Therefore, they achieve higher accuracy for timing analysis especially for highly resistive interconnects and when IR drop is considered [7]. The actual port currents are calculated by interpolation of current waveforms from ECSM/CCS libraries which were characterized for three different voltage levels. However, despite modeling waveforms more accurately, these models still rely on clean signal transitions and pre-simulated waveforms. They cannot handle nonlinear noisy waveforms. On the other hand, CSMs proposed by academia support arbitrary signal shapes as they provide output currents as functions of port voltages instead of slew rate and output load [4], [5], [12]. They consist of at least one voltage-controlled current source and further capacitors or charges. CSMs can be used for accurate timing analysis [2], [9], [22] or noise analysis [6]. However, to the best of our knowledge, none of the approaches deals with supply noise which affects logic cells, nets, and analog components. Furthermore, almost all CSMs assume constant supply voltages which limits their accuracy gains because IR drop or Ldi/dt spikes are ignored. Besides this shortcoming for timing analysis, almost no CSM can be used as a cell model for power analysis because CSMs typically model only the output current. Only a few approaches, which will be discussed in Sect. II, also model the supply currents but at the expense of very high model complexity. The new CSM proposed in this paper overcomes these problems. It is a simple model which accounts for the influence of dynamic supply voltage variations on signal delay and power consumption. It can be used not only for separate timing and power analyses but also for a combined simulation of logic and supply nets. The accurate timing analysis supports arbitrary signal waveforms and dynamic supply voltage variations. At the same time, the model generates accurate supply current waveforms which can be used in a separate power grid simulation.

One of the largest concerns with CSMs is the required simulation effort for building libraries, especially for an increasing number of PVT corners. Most CSMs require a large number of transient simulations which must be performed in addition to the simulations needed for noise and power models. Library characterization can be accelerated by having one holistic cell model for timing, noise, and, power analysis. Ideally, the required simulations are simple and do not need to be repeated for different supply voltages. The CSM presented in this paper is such a model. It consists of only a few 2D lookup tables (LUTs) to keep characterization times low and simulation performance high. It is a versatile model which allows combined power/timing/noise analysis since it provides a cell's output current and the currents drawn from PG nets. No restrictions are made on power grid model, voltage waveform, or load model. The CSM works well for a range of different operating voltages to account for both static and dynamic IR drop as well as different voltage domains. Trade-off between accuracy and speed can be made by varying the size of the LUTs. It is fully integrated into a modern SPICE simulator

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to speed up already efficient tools. However, it can also be used in other, more tailored tools for noise, timing, or power analysis.

The remainder of this paper has the following structure: After reviewing existing CSMs with the focus on supply currents in Sect. II, the new Pullup/Pulldown-Model (PXM) and its characterization are presented in Sect. III. Section IV analyzes model accuracy and speedup.

II. Existing approaches

Current source models are electrical models of logic cells which provide voltage-dependent port currents. Almost every CSM approach for timing analysis models these currents as a function of input and output voltage, and assumes constant supply voltages. Except for a few methods, CSM library characterization has to be repeated for every V_{dd} value, even to account only for static supply voltage drops. The approach of [10] accounts for static voltage drop by linear sensitivities of model components with respect to V_{dd} and therefore avoids re-characterization. However, the model is only accurate for small deviations of V_{dd} and does not consider V_{ss} variations. Moreover, because only the cell output current is modeled, this CSM can only be used for timing analysis. In the approach of [5], only the DC short circuit current has been modeled as a separate voltage-controlled current source of the input and output voltages. The dynamic CSM components are determined through a number of transient simulations. The influence of V_{dd}-drop on output and short circuit current is not considered.

In [14] a CSM for multiple-input switching is also used for power analysis. Each port current is modeled by a voltage-controlled current source and several voltage-controlled capacitors which are connected to all ports. To model the influence of dynamic V_{dd} variations, each model component is a function of all other port voltages and V_{dd}. This allows for usage in power analysis and to consider non-ideal supply nets in timing analysis. However, model complexity is exponential in the number of control voltages which poses new challenges for characterization times, memory requirements, and simulation speed. For a simple inverter model, at least 12 3D LUTs are needed, not considering variations of V_{ss}. The data in each LUT might be compressible by methods such as described in [8].

Transistor-oriented approaches, such as in [15] or [19], replace complex transistor equations by simpler device models. Often at least one 3D LUT is used to model the static current. These approaches are very general. However, since each CSM replaces an individual transistor, the number of instances is high and always requires a SPICE-like simulator, which makes such models less suited for gate level analysis.

III. PXM Model

Figure 1 shows the proposed Pullup/Pulldown-Model (PXM), which models the port currents for the PG pins, dd and ss, the input signal pin, i, and the signal output pin, o. The model targets single input switching, and hence a separate PXM is generated for each input pin. Also, each PXM models one channel connected block (CCB), which consists of pMOS and nMOS transistors. Cells like BUFFERs, ANDs, ORs, are automatically divided into CCBs. The final model then comprises several abutted PXMs.

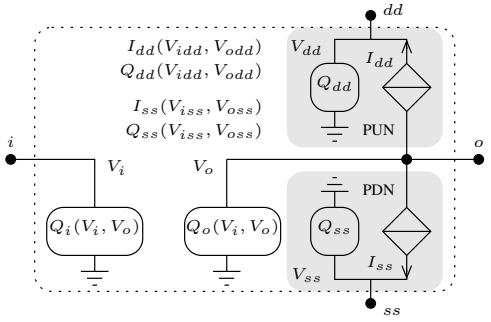

Fig. 1: Proposed PXM model for CMOS logic cells

Deriving and characterizing PXMs follows a transparent modeling methodology. Instead of matching the port behavior of a black box, the transistor netlist of a logic cell is the base to derive the model components. This allows fast and accurate cell characterization and reduces model complexity.

As shown in Fig. 1, the PXM consists of two static voltage-controlled current sources (VCCSs) and four voltage-controlled charges (VCQs). These elements generate the total port currents for signal and PG pins. Each VCCS models the effective static current from PG pin to the signal output for pull up network (PUN) and pull down network (PDN) of the CCB. This allows to model supply currents and output current without additional VCCSs. Similar to most CSMs approaches, the VCCS are implemented as LUTs. For existing methods, these components are controlled by input and output potential, V_i and V_o. To model the effect of different supply voltages, these existing models require at least one 3D LUT for the output current. In this new model however, the lookup tables are indexed in terms of two voltages only: input-to-rail, V_{idd}/V_{iss}, and output-to-rail voltage, V_{odd}/V_{oss}. Thus, the LUTs of the PUN are not controlled by V_i, V_o, V_{dd}, and V_{ss} but by $V_{idd} = V_i - V_{dd}$ and $V_{odd} = V_o - V_{dd}$. This is physically correct, since a transistor current is a function of V_{gs} and V_{ds}. Hence, the currents in the PUN are functions of V_{idd} and V_{odd} but are independent of V_{ss}. As a result, the PXM components I_{dd} and I_{ss} are independent of the absolute values of signal and PG pins. Hence, the model captures the influences of transient PG voltage variations using only two 2D LUTs, and it is also applicable to different voltage domains without re-characterization.

The dynamic characteristics of the logic cell are modeled by four VCQs yielding additional currents $I_{dyn} = \frac{d}{dt}Q$. The charges for PG pins are similar to the VCCSs except that their currents are only sourced into the PG nets and not into the output node. They account for charges at PG pins that act as symbiotic decoupling capacitance for other switching cells and comprise nonlinear transistor charges and charges stored at linear parasitic capacitors.

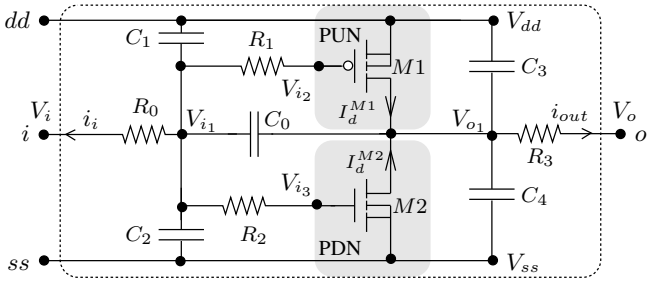

Fig. 2: Inverter with parasitics

Algorithm 1. Deriving Measurements for PG pins

for PG_PIN p in [ss, dd] **do**
  for all Transistor M connected to p **do**
    I_p+= $I_{p,DC}(M)$;
    Q_p+= $Q_p(M)$;
  for all Capacitor C connected to p **do**
    Q_p+= $C \cdot V(C)$;

Dynamic input and output currents are modeled by the time derivatives of Q_i and Q_o. These port charges account for all charges stored at the signal pins. It is clear from the transistor netlist in Fig. 2 that Q_i and Q_o physically depend on V_i, V_o, V_{dd}, and V_{ss}. To avoid 3D LUTs or further VCQs, these port charges of signal pins are modeled as functions of V_i and V_o only. This simplification will be validated at the end of this section.

One major advantage of PXM over other CSMs is its simple and fast characterization. The whole model is characterized by a single DC simulation. Moreover, no re-characterization is needed for different supply voltages.

The characterization consists of two steps; First, SPICE measurement statements are derived from the transistor netlist. Second, these measurements are executed in a DC simulation to obtain numerical values for the PXM components.

Algorithm 1 is used to derive the measurement statements for the VCCSs and the PG charges Q_{dd} and Q_{ss} of one CCB. The netlist is analyzed to identify transistors and capacitors that store charges of the PG net. At the same time, transistors that contribute to the total DC current of the PG pin are found. For CMOS cell these are source current, I_s, and bulk current, I_b. The resulting measurement statements for the inverter in Fig. 2 are

$$I_{dd} = I_s(M1) + I_b(M1) \tag{1}$$
$$Q_{dd} = C_1 V_{dd i_1} + C_3 V_{dd o_1} + Q_s(M1) + Q_b(M1) \tag{2}$$

for the pull up network and

$$I_{ss} = I_s(M2) + I_b(M2) \tag{3}$$
$$Q_{ss} = C_2 V_{ss i_1} + C_4 V_{sso_1} + Q_s(M2) + Q_b(M2) \tag{4}$$

for the pull down network. Prior to executing these measurements in SPICE, the names of linear capacitors in (1)–(4) are replaced by their numerical values. This allows to measure the charges even if the simulator removes the capacitors for a DC simulation.

Algorithm 2. Deriving Measurements for Q_i/Q_o

RT = findResistiveTree(pin, netlist);
for all Node n in RT **do**
  for all Capacitor C connected to n **do**
    $Q_{i/o}$+= $C \cdot V(C)$;
  for all Transistor M connected to n **do**
    $Q_{i/o}$+= $Q_n(M)$;

This internal view on modeling port behavior of logic cells results in two major advantages compared with existing black-box approaches. First, it enables fast characterization which needs a single DC simulation instead of a high number of transient simulations. Second, by identifying the physical sources for model components, artificial dependencies and complexity are avoided. That is, I_{ss} is independent of V_{dd} and should not be modeled using a 3D or 4D LUT. The PXM therefore models I_{ss} as $I_{ss}(V_{iss}, V_{oss})$. Also, there is no need to model output and supply currents by separate VCCSs. Instead, the output current is already described as the sum of I_{dd} and I_{ss}.

Deriving the measurement statements for Q_i and Q_o is conceptually very similar. The only difference stems from the parasitic resistors in the cell. As symbolized in Fig. 2, transistors are not directly connected to the signal pins but through trees made of resistors. There can be capacitors attached to each tree node which have to be considered. Consequently, algorithm 2 recognizes all charges at nodes of each tree and adds them to the port charge.

The resulting measurement statements for the inverter in Fig. 2 are

$$Q_i = C_1 V_{i_1 dd} + C_0 V_{i_1 o_1} + C_2 V_{i_1 ss} + Q_g(M1) + Q_g(M2) \tag{5}$$
$$Q_o = C_3 V_{o_1 dd} + C_0 V_{o_1 i_1} + C_4 V_{o_1 ss} + Q_d(M1) + Q_d(M2) \tag{6}$$

It is important to treat conducting transistors as resistors if they are in the charging path between the switching transistors and the output pin. This ensures that charges at inner nodes of transistor stacks are also recognized as part of the signal port charge.

After the automatic generation of measurement statements for the PXM model components, SPICE simulations are con-

Algorithm 3. LUT Characterization

1: Connect PG pins to nominal supply voltage and ground and attach DC voltage source V_i and V_o to signal pins
2: Set other input pins according to timing vector
3: Perform nested DC sweeps for V_i and V_o and measure I_{ss}, I_{dd}, Q_i, Q_o, Q_{dd}, and Q_{ss}
4: Calculate V_{idd}, V_{odd}, V_{iss}, and V_{oss}

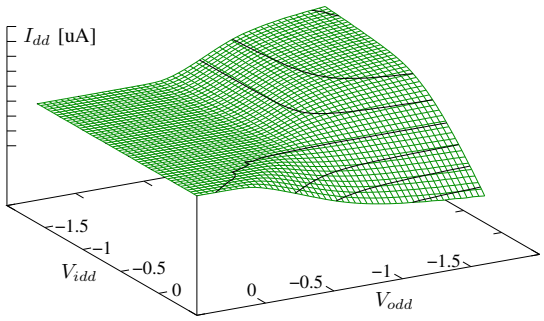

Fig. 3: Typical I_{dd} lookup table

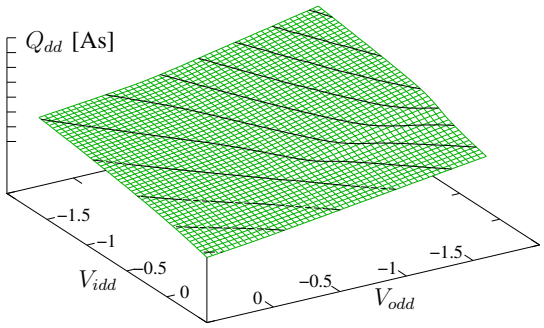

Fig. 4: Typical Q_{dd} lookup table

ducted to obtain numerical values. Algorithm 3 describes steps needed to set up the simulation for characterizing one PXM. Thereafter, the 2D LUTs are written according to their control voltages as described earlier in this section and as noted in Fig. 1. Figure 3 shows a typical I_{dd} LUT which is obviously very similar to the drain-source current of a PMOS transistor. The only difference is that the current results from multiple transistors of which some only contribute leakage currents. Figure 4 displays a typical Q_{dd} LUT which looks fairly linear due to the parasitic capacitances.

Characterizing one inverting stage on a normal desktop machine takes about 2 seconds for 50x50 LUTs. This allows to dynamically extend the PXM cell library immediately before a transient analysis. PXMs that not yet exist are generated on the fly and are then used in the normal SPICE simulator.

It is clear from (5)–(6), that the signal charges, Q_i and Q_o, physically depend on the four potentials V_i, V_o, V_{dd}, and V_{ss}. To avoid 3D or 4D LUTs in the PXM, these charges are modeled as $Q_i(V_i, V_o)$ and $Q_o(V_i, V_o)$. This, however, is only accurate if V_{dd} and V_{ss} have the same values which were used during LUT characterization. For other supply voltages the charge values are different, resulting in different dynamic currents. However, this effect is not very pronounced as the accuracy studies in Sect. IV and Fig. 5 show. In the latter, the output voltage waveforms of a cell are shown for different supply voltages. Additionally, voltage spikes of 0.3V appear in V_{dd} and V_{ss}. PXM and transistor simulation (BSIM) show identical results which validate the simplified modeling of Q_i and Q_o.

Regarding the static VCCSs, I_{dd} and I_{ss}, the PXM approach

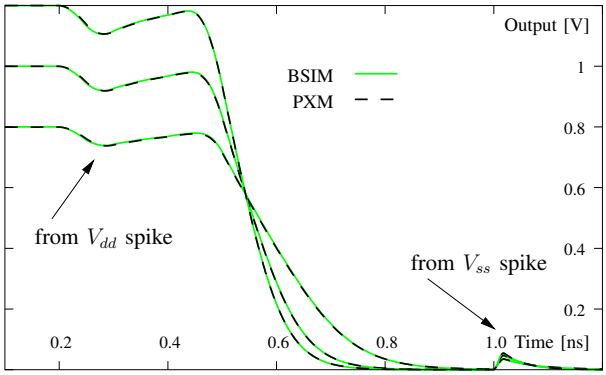

Fig. 5: Output waveform for V_{dd}=0.8/1.0/1.2V and 0.3V noise spikes on V_{dd} and V_{ss}

essentially considers PUN and PDN as a kind of macro transistors. Nonetheless, gate-source voltages of nonswitching stack transistors influence the effective current. This nonlinear dependency is efficiently modeled by scaling the DC currents I_{dd} and I_{ss}. The factors depend on the position of the active transistors in the stack and the effective voltage swing, and are automatically derived during model generation.

IV. Results

The PXM has been implemented as compiled model for a commercial SPICE simulator because many sign-off tools offer SPICE level simulation of critical paths [20]. The PXM can be used to speed up these simulations. It is also possible to use PXMs for digital blocks in a mixed signal simulation while the analog components are modeled using transistors. Bilinear interpolation is used for the LUTs.

Cell	V_{dd}	Rel. Err. [%]: Delay		Rel. Err. [%]: $\int I_{dd}dt$		Rel. Err.[%]: $\int I_{ss}dt$	
		Mean	$P_{98\%}$	Mean	$P_{98\%}$	Mean	$P_{98\%}$
INVs	1.2	0.2	1.0	0.0	0.1	0.0	0.1
	1.0	0.3	1.1	0.1	0.3	0.3	1.0
	0.8	0.4	1.1	0.3	0.6	0.5	1.4
BUFs	1.2	−0.0	1.3	0.1	1.6	−0.1	1.9
	1.0	−0.1	1.8	−0.0	0.8	−0.2	0.6
	0.8	−0.2	2.8	−0.3	0.3	−0.4	1.2
NANDs	1.2	−1.2	0.3	−0.0	0.2	0.2	0.7
	1.0	−0.4	0.5	0.1	0.5	0.4	1.8
	0.8	1.9	8.4	0.1	0.8	0.6	2.6
NORs	1.2	0.0	0.6	0.4	1.9	−0.1	0.6
	1.0	0.5	3.1	0.7	4.3	0.1	1.4
	0.8	0.9	3.5	0.8	4.7	0.1	1.8
ANDs	1.2	0.2	6.8	−0.5	0.3	−0.5	4.3
	1.0	−0.2	1.5	0.1	0.5	−0.2	0.1
	0.8	−0.6	0.9	0.2	0.6	−0.0	0.2
ORs	1.2	−0.5	0.4	0.2	5.1	−0.9	0.6
	1.0	−0.6	1.1	0.2	9.6	0.3	3.6
	0.8	−1.0	0.7	−0.3	0.1	1.1	5.1
COMPLEX	1.2	−0.5	0.5	−0.2	6.4	−0.1	5.0
	1.0	−0.3	3.5	−0.6	2.4	−0.1	4.1
	0.8	−0.1	6.9	−0.0	1.1	0.0	2.4

TABLE I: Relative errors for delay and total supply currents. Each cell is simulated individually with different values of slew, load, V_{dd}, and is compared with transistor simulation.

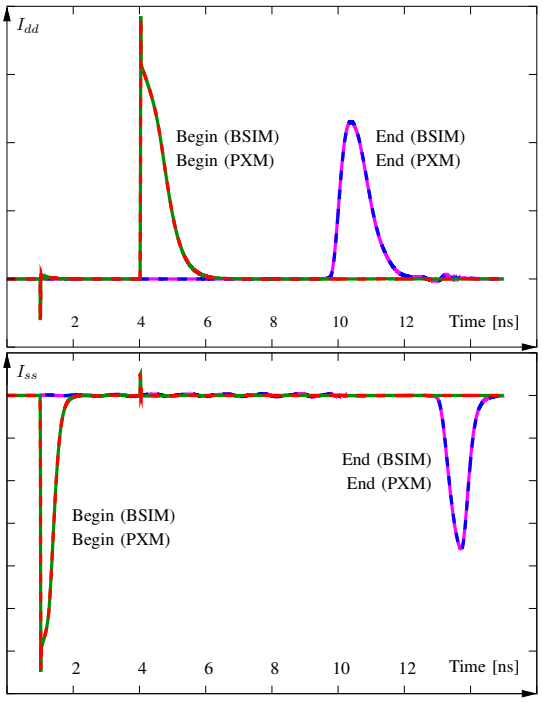

Fig. 6: Supply currents

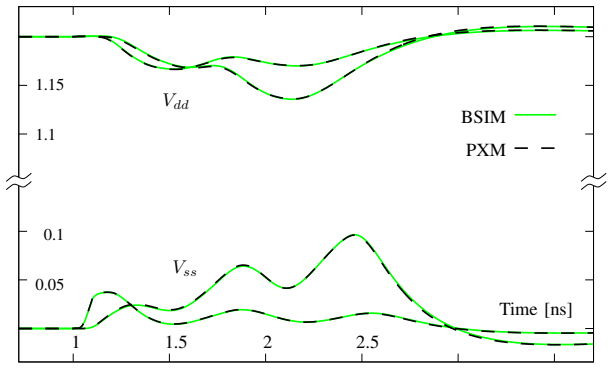

Fig. 7: Correct prediction of noise on RLC supply nets

A library of PXMs for industrial 90nm standard cells of different sizes and types has been generated with V_{dd}=1.2V and studied in a SPICE simulator. In the first test, each cell has been simulated individually with different input slew rates and output loads. Total current consumption, $\int I_{ss/dd}dt$, and cell delay have been measured and are compared with the results when using the original BSIM transistor netlist. Table I lists mean and 98 percentile of the relative errors in percent, sorted by supply voltage. Very small average and maximum errors have been observed for most simulations. Nonetheless, for a few cases delay errors are close to 10 percent. It has been noted that accuracy is lower for stacked switching transistors and very small output loads. This is due to a notable signal delay between port voltage and voltages at the switching transistors. Consequently, there are differences in voltages and currents between DC characterization and transient simulation.

In the next test, PXM accuracy and performance are analyzed for simulating generic paths. Therefore, cell chains, powered by RC chains as PG model, have been simulated and compared for delay, energy consumption, and simulation speed. The chains consist of 20 cells to cover various values of V_{dd} and V_{ss} and different signal waveforms. Figure 6 shows typical supply current waveforms for I_{dd} and I_{ss} for the first and the last cell in a chain. PXM and BSIM reference simulation overlap almost completely. It is important to note the differences in PG current waveforms between the first and the last cell. They result from IR drop along the chain. CSMs that ignore this dependency would overestimate the peak currents but underestimate the path delay. This visual PXM validation corresponds to the very small errors for delay and energy consumption which are shown in Tab. II. Depending on the gate complexity, SPICE simulations are accelerated by up to 53X, while the maximum errors in delay and energy do not exceed 1 and 3 percent, respectively. Even higher simulation performance can be achieved by approximating the LUTs as closed form expressions, which is the subject of current work.

CELL	Speedup	Err D [%]	Err E [%]
INVS	32.24	≤2.62	≤0.92
BUFS	29.20	≤1.38	≤0.75
NANDS	27.24	≤0.56	≤0.67
NORS	52.81	≤0.82	≤1.90
ANDS	14.61	≤0.08	≤0.51
ORS	23.21	≤5.34	≤0.56
COMPLEX	31.50	≤1.19	≤1.89

TABLE II: Speedup and relative errors for delay (D) and energy (E) for simulating cell chains with supply networks (different driver strengths and cell types)

Figure 7 finally shows the potentials for different nodes of V_{dd} and V_{ss} when using an RLC model for PG. Since the PXM correctly predicts supply and output currents, also the noise on supply nets is modeled with high accuracy.

V. CONCLUSION

In this paper a new CSM called PXM has been presented. It allows combined simulation of signal and supply nets with high accuracy. Compared with existing methods, it is much faster to characterize and less complex. The PXM accounts for dynamic supply voltage variations and can be used for different supply voltages without re-characterization. Used as cell model for a combined power and timing simulation, SPICE runtimes were reduced by up to 53X. The PXM is not limited to SPICE simulators but can be used in dedicated power, timing, and noise analysis tools.

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