Hierarchical Test for Today’s SOC and IoT

Yervant Zorian, SYNOPSYS

Agenda

- Trends & Challenges
- IP-Level Test Preparation
- Beyond SOC: IEEE Test Stnds
- New Topics

- Hierarchical Test Solution
- SOC-Level Test Optimization
- Life-Cycle Test & Diagnosis
- Conclusion
Data, Data, Data
*Higher Capacity, Faster Transfer, and Lower Cost*

By 2017, the annual global IP traffic will surpass the zettabyte threshold (1.4 zettabytes).

Traffic from wireless and mobile devices will exceed traffic from wired devices by 2016.

Source: Cisco Systems, VNI Global Mobile Data Traffic Forecast Update 2013

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### Mobile

Source: Business Insider, December 2013
The Emerging Scene!

- Infrastructural core
- Internet of Things
- Mobile access

What’s Moving to the Cloud

- Business Apps
- Enterprise Resource Management (ERP) Financials
- TechApps (design, eng, R&D)
- ERP HR
- Collaboration Apps
- Email
- Data analysis/mining apps
- Data Backup/archive
- Help Desk/IT Service Management
- Storage Capacity on-demand
- Application development
- IT Management (server network)
- Mobile Device management

Cloud Computing Driving Growth of Mega Data Centers

36% CAGR
Cloud 2.0 for the Internet of Things
Central Cloud for Ubiquitous Connectivity

Reducing Power in Data Centers: System Integration Enables New Micro Servers

Micro server SoCs integrate 64-bit CPU, networking, security, storage with targeted workload application acceleration & high-speed I/Os
Wireless Phone

- Voice → Voice communication with some applications
  → **Multimedia applications** with voice communication

![Wireless Phone Diagram](image)

Convergence

![Convergence Diagram](image)
**Clock Frequency Trends**

*Clock Frequencies Increase to Keep Up with Bandwidth and Functionality*

![Clock Frequency Trends Graph]

Source: 2014 Synopsys Global User Survey

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**Coping with Moore’s Law**

![Coping with Moore’s Law Graph]

Source: Pat Gelsinger
## IC Design Expensive and Difficult

<table>
<thead>
<tr>
<th></th>
<th>32/28nm node</th>
<th>22/10nm node</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fab costs</td>
<td>$3B</td>
<td>$4B – 7B</td>
</tr>
<tr>
<td>Process R&amp;D costs</td>
<td>$1.2B</td>
<td>$2.1B – 3B</td>
</tr>
<tr>
<td>Design costs</td>
<td>$50M – 90M</td>
<td>$120M – 500M</td>
</tr>
<tr>
<td>Mask costs</td>
<td>$2M – 3M</td>
<td>$5M – 8M</td>
</tr>
<tr>
<td>EDA costs</td>
<td>$400M – 500M</td>
<td>$1.2 – 1.5B</td>
</tr>
</tbody>
</table>

- Intensive customer/partner collaborative developments

Source: IBS, May 2011

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### Challenge 1: Power

**Multi-Core**

Source: Intel
Challenge 2: Productivity Gap

IP Re-Use

Source: SEMATECH

IP-based design
Enabling system companies to design chips
(Apple, Microsoft, Amazon, Google....)

- Including
  - Configurable processor core
  - Memories (RAM, ROM)
  - Special-purpose standard blocks (ASSPs)
  - Glue logic
Drivers of Hierarchical Test

- Growing volume of IP in an SOC
- Increasing design complexity with multiple levels of hierarchy
- Exploding digital logic size
- Increasing types of IP blocks to realize standard functions
- Growing use of 3rd party IP
- Increasing use of advanced technologies
- Dispersing design teams globally
- Tight time-to-volume schedules
- Improving test & debug access throughout life cycle

1. Growing Use of IP

- IP test based on direct access increases test time and cost
- Ad hoc IP test access not scalable
- Reduced pin access, flexible test scheduling & concurrent test needed
1. Ad-hoc IP/Core Test Access Can’t Scale

Rely on direct I/O access

Limited I/O access for larger designs with many IP/cores and hierarchy

Direct I/O access is feasible only for small designs

How to Access?

2. Multi-Level Hierarchical Design

- Flat DFT approaches and centralized test management are expensive in area and design time
- Hierarchical DFT access and pattern reuse/porting required
- Automated hierarchical level test sign-off required
3. Exploding Digital Logic Size

- Increased test time and power consumption during test
- Long test development time for flat designs
- Divide & conquer: design partitioning and wrapping needed

![Graph showing design size percentage over years]

3. Exploding Digital Logic Size (cont.)

- SoC not designed to handle power during full chip test
- Complex DFT and design planning
- Controllability & observability at core level needed
- Longer ATPG runtimes
4. Numerous Heterogeneous IP Types

- AMBA 2.0 AHB → AMBA 3 AXI → Network on Chip (NoC)
- AMBA APB
- GPIO
- USB controller
- Ethernet controller
- SATA controller
- PCIe controller
- DDR controller
- PCI Express (PCIe)
- DDR Phy
- DDR controller
- DDR PHY
- SD/MMC controller
- SATA Phy
- XAUI Phy
- XAUI controller
- SATA controller
- MIPI controllers
- D-PHY
- M-PHY
- Embedded Memories (SRAM, ROM, NVM)
- Datapath
- Logic Libraries
- Processor IP
- Soft IP
- Hard IP

4. Heterogeneous IP Market Segments

- Microprocessors: 41%
- Memory Cells/Blocks: 16%
- Wired and Wireless Interfaces: 19%
- Fixed Function (GPUs, Security): 14%
- Memory Controllers: 10%
- Optical PHY: 3%
- GP Analog/MS: 3%
- Other: 4%
- Embedded Logic: 3%
- Block Libraries: 1%
- Physical Library: 3%

Source: Gartner, 2013
4. Heterogeneous IP Test Challenges – Memory/AMS/Legacy IP

- SoC test integration is done manually
- BIST Engines & Debug Modes
- Uncontrollable I/O impacts test quality
- Functional I/O-only access makes it difficult to develop test

4. Heterogeneous IP Challenges – Embedded Measurement IP

- Power Management Controllers
- Temperature Sensors
- Radio Tuners
- Measurement Probes
- Clock Generators
4. Embedded Measurement IP

**Temperature Sensors**

**No standard test Interfaces**

**Uncontrollable Instruments impacts test quality**

**Functional I/O-only access makes it difficult to develop test**

5. Growth in 3rd Party IP Usage to Double

- **Escalating Design Costs**
- **Increasing Design Complexity**
- **Shorter Time Window for New Product Launch**

**Strong Growth in 3rd Party IP Usage**

<table>
<thead>
<tr>
<th>Sector</th>
<th>2012</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Consumer</td>
<td>0%</td>
<td>30%</td>
</tr>
<tr>
<td>Wireless Communication</td>
<td>5%</td>
<td>45%</td>
</tr>
<tr>
<td>Data Processing</td>
<td>7%</td>
<td>60%</td>
</tr>
<tr>
<td>Automotive</td>
<td>8%</td>
<td>75%</td>
</tr>
<tr>
<td>Industrial</td>
<td>6%</td>
<td>90%</td>
</tr>
<tr>
<td>Wired Communication</td>
<td>3%</td>
<td>15%</td>
</tr>
</tbody>
</table>

Source: Gartner, 2013
Integration

• Before 32nm, new process was introduced every other year
  ▪ Since then, a new process every year

* Source: ITRS, Samsung Electronics Co.

Innovation Enabled Technology Pipeline

IDF – Silicon Leadership

- Manufacturing & Test Quality are critical
- Modeling new types of defects (FinFET)
- Programmable test infrastructure, yield optimization and calibration techniques needed
7. Globally Dispersed Design Teams

- Ad-hoc hand-off is error prone and time consuming
- Automated sub-chip level integration and hierarchical sign-off needed

8. Shorter TTM and TTV

- Long development Time for ad-hoc bring up and silicon debug
- Uniform access and use of IEEE test standards reduce bring-up complexity and simplifies silicon debug
Yield Life Cycle Curve

Design Production Ramp-up Volume

Yield Life Cycle Curve

Design Production Ramp-up Volume

Yield Life Cycle Curve

Design Production Ramp-up Volume
Expect Many Types of “Things”

Highly Fragmented Market

- By 2016, 50% of Internet of Things solutions will originate in startups less than three years old.
  - Expect 10 billion shipments in 2020
  - Many smart versions of existing product markets
  - Key challenge: where to focus?

Source: Gartner, Preliminary, Sep 2013
Significant Growth in Sensors
Sensor Units to Grow to 30 Billion Units in 2017

Source: Semico Research, 2013

How the Billions of “Things” are Connected…

IoT Edge Devices
"Things" with sensors & actuators that monitor and control

Aggregation Layers
(Hubs/Gateways)
Connectivity & Interfaces to aggregate the edge data to send to the cloud

Remote Processing
(Cloud Based)
Applications to analyze the data and offer cloud services
The IoT Opportunity Gap

The IoT Opportunity is much larger than analysts predictions for connected devices (2020):
- 10 billion?
- 50 billion?
- 75 billion?
- 100 billion?

Market is growing rapidly, it’s been around for over 20 years.

Silos of Things

Today

Reach

Time

Functional Becomes IOT Data /Leveraging data enabled services revolution

Relationship: Users, Devices & Services

Functional

Data

drive like a girl

CAR INSURANCE
DESIGNED FOR GIRLS

17-25 year old save the most
IoT Edge Devices
A Market Segmentation

<table>
<thead>
<tr>
<th>Wearable Devices</th>
<th>Health &amp; Fitness</th>
<th>Smart Appliances</th>
<th>Safety &amp; Security</th>
<th>Smart Cities Metering</th>
<th>Commerce</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wearable Infotainment</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Machine to Machine

<table>
<thead>
<tr>
<th>Wearable Devices</th>
<th>Google Glass</th>
<th>Samsung Gear S Smart Watch</th>
<th>Samsung Gear Fit Smart Watch</th>
<th>Starkey Hearing Aid</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>570mAh Li Polymer</td>
<td>300mAh Li-Ion</td>
<td>210mAh Li Polymer</td>
<td>91 - 630mAh Zinc Air</td>
</tr>
<tr>
<td></td>
<td>1 day</td>
<td>2 days</td>
<td>4-5 days</td>
<td>3-22 days</td>
</tr>
</tbody>
</table>

source: IEEE CS & ComSoc Joseph A. Paradiso, Thad Starner 2005

Laptop Computing Technology Improvements

source: IEEE CS & ComSoc Joseph A. Paradiso, Thad Starner 2005
A Better Source Of Power
We Have Potential!

Body heat 2.4-4.8 W
Exhalation 1.0 W
Blood pressure 0.93 W
Breathing band 0.83 W
Arm motion 60 W
Finger motion 6.9-19 mW
Footfalls 67 W

source: Joseph A. Paradiso, Massachusetts Institute of Technology Media Lab, Thad Starner, Georgia Institute of Technology, GVU Center

Bodies In Motion...

Stepping in your shoes
Energy harvested 7-67 W
possible but practically around 1 W

Walking the streets
Energy harvested: 1 square generates up to 2.1 watts

source: postscape.com
Implanted Device
RF/Thermal/Piezo Powered

- Energy requirements
  - active 500 μs per minute ~ 60 μJ
- Energy content of an implantable Li-ion battery is ~200mAh (Quallion)
  - would last 1*E+5 hrs = 11.4 years!!

- Exploring MIM Cap capabilities
- MIM Cap: 38 fF / μm²
  - 4 mm x 4 mm -> C = 0.6 μF
  - Total Energy = 2.7 μJ @ 3V
- Energy requirements
  - active 500 μs per minute ~ 60 μJ
  - NOT feasible with MIM
  - BUT easy with SuperCaps
- Harvesting Piezoelectric (blood pressure) or thermal energy
  - Blood pressure @ .37W can easily sustain energy needed
Wearable Systems
Thermally Powered

• Low power embedded processors, along with innovative energy harvesting and storage technologies will make many autonomous, connected "Things" possible.

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What is the PRIMARY application of your design?
GLOBAL 2014

Internet of Things

<table>
<thead>
<tr>
<th>Category</th>
<th>2014</th>
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</thead>
<tbody>
<tr>
<td>Wearable Devices/Fitness/Portable Medical Devices</td>
<td>35%</td>
</tr>
<tr>
<td>Smart Home/Smart Appliances</td>
<td>19%</td>
</tr>
<tr>
<td>Embedded Vision/Sensor</td>
<td>13%</td>
</tr>
<tr>
<td>Smart Meter</td>
<td>11%</td>
</tr>
<tr>
<td>Machine-to-Machine</td>
<td>9%</td>
</tr>
<tr>
<td>Smart City, such as Digital Lighting</td>
<td>6%</td>
</tr>
<tr>
<td>Other</td>
<td>6%</td>
</tr>
</tbody>
</table>

Wearable Devices/Fitness/Portable Medical Devices

<table>
<thead>
<tr>
<th>Category</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>Portable Medical Devices</td>
<td>33%</td>
</tr>
<tr>
<td>Smartwatch</td>
<td>29%</td>
</tr>
<tr>
<td>Smart/Mobile Headset/Headphone</td>
<td>17%</td>
</tr>
<tr>
<td>Activity Tracker (Lifelog)</td>
<td>15%</td>
</tr>
<tr>
<td>Smartglass</td>
<td>10%</td>
</tr>
<tr>
<td>Other</td>
<td>6%</td>
</tr>
</tbody>
</table>

Synopsys Global User Survey 2014

No historical data as these are new questions starting 2014.
Problems to solve for Market Acceleration

Internet of Things
- Scale needs interoperability
- Interoperability needs Standards
- Sharing needs Trust
- Trust needs Identities & Security

Internet Of Things
- Interoperable Data and Objects
- Secure and Trustworthy
- Internet model

Today
- Silos of Things
- Everything nearly connects

Reach
- Fixed Telephony Networks
- Mobile Telephony
- M2M
- SaaS
- Internet / broadband
- Mobile internet
- Applications

IoT – The Big Picture

“Normal” Thingteractions
- Own, share, use directly

User <-> Service
- Security, privacy, ownership

Device <-> Service
- Connect
- Manage
- Application development
- Security End to End

Users

Services

Things
IoT Integration Trends

*Processor, Wireless, Power Management, Sensors…*

**High-End Integration**
High-end wireless (WiFi, Cellular, GPS), vision, audio, voice, etc.

**Low-End Microcontroller Integration**
Bluetooth Smart, 802.15.4, and ISM wireless CMOS Sensors (Cap Touch)

**Sensor Integration**
Integration of “Smarts” (Processor & NVM)

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IoT: Extremely Challenging Design Constraints

- **Time to Market**
  - Past: <3-4yr
  - Future: <1-2yr

- **Cost of end chipset**
  - Past: >> $1
  - Future: << $1

**Design Constraints**

1. Signal Chain ➔ as complicated as a cell phone
2. Cost ➔ < 1/100th of a cell phone
3. Size ➔ < 1/1000th of a cell phone
4. Power Consumption ➔ < 1/10000th of a cell phone
Automotive Electrification Drives the Use of ECUs

Rapid Growth in New Electronic Systems

- Dozens of additional ECUs per car
- Functional qualification becoming more critical for safety
- Millions of lines of software code
- Validation and test needs to start as early as possible

Automotive Electrification Drives the Use of ADAS

Advanced Driver Assistance Systems

- ADAS design requires flexible, scalable, integrated development platforms
- A complete ecosystem of software, IP and design tools yields necessary design productivity
The Connected Automobile

Variety of IP
- Ethernet QOS
- USB 2.0 / 3.0
- Floating-point and datapath
- Audio Subsystem

The Cloud:
Data services, reporting and tracking

Secure Cloud Access Gateway

Body / Comfort Systems
Chassis / Safety Systems
Infotainment Systems
Powertrain Systems
Camera (ADAS) Systems

Variety of IP
- Ethernet QOS
- USB 2.0 / 3.0
- Floating-point and datapath
- Audio Subsystem

Evolution Interface Standards
Driving IP Portfolio Evolution

New IEEE standards for Automotive Networking
### Automotive Challenges

<table>
<thead>
<tr>
<th>Category</th>
<th>Details</th>
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</thead>
<tbody>
<tr>
<td>Safety &amp; Quality</td>
<td>• ISO 26262</td>
</tr>
<tr>
<td></td>
<td>• Fault injection</td>
</tr>
<tr>
<td>Reliability</td>
<td>• Design for Six Sigma (DFSS)</td>
</tr>
<tr>
<td></td>
<td>• Traceability of system requirements</td>
</tr>
<tr>
<td>Time to Market</td>
<td>• Design iteration time</td>
</tr>
<tr>
<td></td>
<td>• IP integration</td>
</tr>
<tr>
<td>Development Costs</td>
<td>• Supply chain optimization</td>
</tr>
<tr>
<td></td>
<td>• HW/SW integration and verification</td>
</tr>
</tbody>
</table>

### Automotive Solution

**Improve Functional Safety, Robustness, Reliability and Quality of their Automotive Systems**

- System and IC Level Fault Solutions
- SW Security and Quality Semiconductor IP
- High Reliability IC and FPGA Design
- LBIST and MBIST
- Mechatronics Power Systems Wire Harness
- MCU Architecture Design
- LED Lighting Design and Simulation
- Complete Verification Environment
- Virtual IC Modeling and Simulation
- Early SW Development
9. Cradle-to-Grave Life-Cycle Approach

- What is changing in the world of hierarchical design, and how can we adapt to these changes
- How do we leverage IEEE Test Standards to design, manufacture, and take care of systems
- What standards are getting real use
- What does the “developing world” look like in terms of IEEE standards

Test Stages

- Wafer sort
- Laser repair
- Silicon debug
- Package test (final test)
- Burn-in
- Field operation
Hierarchical Test Solution
- Simple Two-Level Hierarchy: IP to SOC
- Unified Test Access
Subchip-Level Test Management

Top-Level Test Management
Communication via IEEE Test Standards

Hierarchical Design & Verification
IEEE Test Standards Projects

- 1149.1
- 1149.4
- 1149.5
- 1149.6
- 1149.7
- 1149.8.1
- 1450
- 1450.1
- 1450.2
- 1450.3
- P1450.4
- P1450.5
- 1450.6
- 1450.6.1
- P1450.6.2
- P1450.7
- P1450.8
- 1500
- 1532
- 1581
- 1687
- P1804
- P1838

Applications

- IEEE Std 1500 – Core Wrapping
- IEEE Std 1450.6 – Core Test Language

- AMS IP
- Memory BIST
- Digital Cores
- Die Stacks
- Manufacturing Test
- Field Access

- IEEE Std 1450 – STIL
- IEEE Std 1450.1 – Scan additions to STIL
- IEEE Std 1149.1 – Boundary Scan (JTAG)
- IEEE Std 1149.6 – High-speed Interconnect
- IEEE Std P1838 – 3D-IC

- IEEE Std 1687 – Instrument Access
Hierarchical Test Solution Advantages

*Accelerate SoC Testing, Improve Test QoR*

- Unified hierarchical test solution for memory, digital logic and AMS IP cores, enables reduced pin count test
- Increased design productivity and ease of use due to test resource partitioning
- Improved portability enables IP test reuse and ensures quality
- Subchip-level test closure
- Flexible test scheduling enables concurrent testing, and thus, reduced test cost
- Improved quality due to test programmability, yield and calibration

Hierarchical Test Capabilities

- Hierarchical Test Solution to allow the following
  - IP-Level Test Preparation
  - IP-Level Wrapping
  - Multi-Level Test Management
  - Pattern Porting: from IP to hierarchical-levels
  - SOC Test Integration & Scheduling
Benefits of IP/Core Wrapping

- Test Access/Isolation for IP/Cores in SoC allows
  - Test Access to core terminals
  - Higher coverage for UDL via scan test
  - Fast and easy reuse of IP Validated Test Programs providing major benefits in SoC development

- Additional BIST options allow
  - Extra savings in ATE costs through trade-off between ATE cost and silicon area
  - Major Test Program development cycle to become a simple BIST run
IEEE Std 1500: Core Wrapping

- Hardware standard for core wrapping
- Defines wrapper and test-mode control
- Mandates specification in IEEE Std 1450.6 (CTL)
- Supported by IEEE Std 1450.x (STIL) for test patterns

Wrapping
Wrapping

Each core with 100s or 1000s of I/Os

Wrapping Features

Dedicated or Shared

Maximize Register Reuse

= dedicated

= shared

= non-wrapper
IEEE Std 1500 Hardware

Wrapper Serial Port

IEEE Std 1500 Hardware

WSP

WSI
SelectWIR

WIR

WSO
IEEE 1500 Wrapper Overview

Core

test in/outputs

functional in/outputs

Functional inputs

test in/outputs

Functional outputs

Functional inputs

Wrapper

Functional inputs

1500 Wrapper General Structure

Mandatory ports, registers

Optional ports, registers
1500 Wrapper Instructions

- **Standard Instructions**
  - **Required**
    - WS_BYPASS – Allows normal (functional) mode and puts the wrapper into bypass mode.
    - WS_INTEST – Allows internal testing using a single chain configuration in the WBR.
    - WS_EXTEST – Allows external test using a single chain configuration in the WBR.
  - **Optional**
    - WP_EXTEST – Allows external test using a multiple scan chain configuration in the WBR.
    - WS_SAFE – Puts the core into a quiet mode and outputs a predefined static (safe) state from all output ports. It also puts the WBR into bypass mode.
    - WS_CLAMP – Outputs a programmable static (safe) state from all output ports. It also puts the wrapper into bypass mode.
    - WS_PRELOAD – Loads data into the single silent shift path of the WBR.
    - WP_PRELOAD – Loads data into the multiple silent shift path of the WBR.
    - WS_INTEST_SCAN – Allows internal testing by concatenation of the wrapper chain with a single internal chain.

- **Specific Instructions**
  - WS_WBR_SEL - Selects wrapper boundary registers between WSI and WSO.
  - WH_DIRECT - Configures the cells to use parallel test inputs/outputs during a test.
  - WS_MODE_SEL – Configures the configuration of the cell.
  - WS_STATIC_SEL - Selects the static register for forcing values to user pins.
  - WS_STATIC – Configures the cells to force the content of the static register to corresponding user pins.
  - WS_SCAN_SHIFT - Configures the cells to be automatically updated during shift.
  - WS_ID_SEL – Selects the unique ID of the wrapper.
  - WS_<CORE_CHAIN_ID>_SEL – Selects the core’s test chain between WSI and WSO.

Two Compliance Levels

- **IEEE 1500 Prepared**
  - Core does not have a complete IEEE 1500 wrapper function
  - Core has a complete IEEE Information Model, which accurately describes the core’s tests, as well as provide all information on the basis of which the core could be made ‘IEEE 1500 Wrapped’ (either manually or automatically by tools)

- **IEEE 1500 Wrapped**
  - Core incorporates complete IEEE 1500 wrapper function
  - Core has a complete Information Model, which accurately describes the core’s tests, as well as the wrapper and how to operate it
IP-Level Test Preparation
for IEEE 1500 Wrapping

- Core (ports)
  - core at RTL level

- Specification (standard format)
  - Specify the ports to be wrapped
  - Specify WIR width

- Outputs
  - WBR, WIR and WBY components in RTL format

IP-Level Test Preparation
IEEE 1500 Access

- Cores (ports)
  - Core at RTL level

- Specification (standard format)
  - Standard file with ports not to be wrapped
  - Specify WIR width

- Outputs
  - WIR and WBY components in RTL format
IP/Core Wrapping Specification

- **Port information** – digital, analog, clocks, resets, supplies, tie-offs, frequency, active level, direction, range, expand factor
- **Chain information** – test and DFT chains. IEEE 1500 access provided to test chains. DFT stitching script is generated for DFT chains.
- **Chain order** – physical ordering of pins included in test chains
- **Analog stimulus** – parameters of predefined analog stimulus (triangle, sin, constant)
- **Test patterns** – description of test mode, analog stimuli and input-output patterns for test chains

Memory IP Wrapping with BIST

- Advanced Self Test and Repair (STAR) engine for each group of lowest-level memory IP
- IEEE 1500 wrapper and standard interface to communicate all test, diagnosis, and repair info
AMS IP Wrapping w BIST

ADC BIST contains

- **SRAM** – for storing the code appearance numbers
- **User registers** – for input data specified by user (number of samples, ideal number of codes, etc.)
- **Internal registers** – for storing the calculated parameter values (ROFFSET, RINL, PASS, etc.)
- **Analyzer block** – parameter evaluation for PASS/FAIL report

ADC Integration with Hierarchical Test

SoC

- JTAG TAP
- Server

Embedded Memory

1500 Wrapper

Analog Mixed Signal IP

ADC

ADC BIST
Interface IP Ready for Hierarchical Test

- USB
- MIPI
- HDMI
- SATA
- PCIe
- DDR
- Ethernet

Faster test integration and re-use of IP patterns saves time and resources

AMS IP Test Preparation

- Embedded AMS/IP may be in three variants
  - "Lite": no or minimal DfT → problem for later
  - "Integrated Test": e.g. Interface IP with BIST/Loopback)
  - “Self Test and Repair”: repair features included, e.g. trimming

- Generate IEEE1500 Wrapper for AMS/IP
  - IEEE1500 compliant
  - Allows easy reuse of IP test patterns at SoC level
  - Solves SoC test access issues

- Provide AMS/IP measurement / test / diagnostics / calibration / repair libraries
  - Developed by IP providers, reused by IP users
  - Alignment of measurement and test methods
IEEE Std 1450.6 (Core Test Language)

*Broad Acceptance and Successful Use Since 2005*

- A broad language supporting test hardware definition and specification
- Supports hierarchical DFT synthesis operations
- Maps pattern data to test access mechanism (TAM)
- Supports protocol porting (up the hierarchy)

CTL Required to Support DFT Synthesis

- “Parallel” scan chains (normal scan, for example)
- Head synchronization (flop, latch)
- Head clock source
- Head clock polarity
- Head clock timing
- Tail synchronization (latch, flop)
- Tail clock source
- Tail clock polarity
- Tail clock timing
- Scan chain content and clock associations
- Scan enable pipe-lining support and enablement
- Compression
- Protocols other than “capture – shift – update”
- Clock connectivity information (e.g. OCC)
- Semantic meaning behind clock chain (control) bits
- Definition of synchronous clock domains
**IEEE Std 1450.0 and 1450.1 (STIL)**

- STIL defines pattern data
- IEEE Std 1450.0 defines simple pattern data
- IEEE Std 1450.1 defines extensions for scan
- CTL can port these patterns via protocol manipulation

---

**Hierarchical Design Flow**

```
Design  Integration  Validation  ATE  Diag

TOP -> STIL 2

1500 Core -> Core

CTL -> CTL 2
```

```
Simulation -> Pass Fail

FA
FA

Simulation
```
SoC Level Test Integration

Server is 1149.1 compliant, where:
- Wrappers are connected to Server
- WIRs are controlled by Server
- Patterns are ported from IP level to TAP level
**Multi-Hierarchy Support**

Complex hierarchies of designs with different types of IPs can be handled within the proposed infrastructure.

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**Save Development Time and Resources**

*Re-use IP/core Patterns at SoC Level*

Patterns can be ported and validated at any design hierarchy level.
IoT Nodes Block Diagram

- Small devices with minimal processing capabilities
- Four major components:
  - Sensor
  - Micro Controller
  - Radio
  - Energy Management

Variation of IoT Devices

- Very wide range of applications drive many types of IoT nodes

- Gyroscope, Accelerometer, Pressure/Temperature/Humidity/Altitude/... Sensor
- WiFi, Zigbee, GSM, GPRS, Blue Tooth....
- From sophisticated to no data processing
- Solar, EM, Vibration, Air flow, Liquid flow, ....
- AC Power, Short Burst battery, ....
- MEMS → ADC → MicroController & Base Band → Radio & FE
- Power Management / Energy Harvesting
The Market Will Demand Integration

- Most IoT nodes start with discrete components
  - Fast prototype for system and software development
  - Fast TTM and design win
- However, volume production will demand integration
  - Smaller size, footprint
  - Lower power
  - Lower cost

Example IoT SoC Architectures

Corral the Market Fragmentation

High-End Edge Device
- DDR, App Proc w/MMU, LCD/GPU, USB, Ethernet, MIPI
- 65nm → 28nm (some 40nm)
- Linux, Android
- WiFi, Bluetooth Smart Ready, 2G/3G

Low-End Edge Device
- IP: eFlash, NVM, USB, ADC
- 90nm → 55nm & 40nm
- RTOS: FreeRTOS, Contiki, MQX
- Bluetooth Smart, 802.15.4

Smart Analog Device
- IP: Power, Audio, Sensor
- 180nm some 130/110/90nm
- RTOS: None, Limited RTOS
- Bluetooth Smart, 802.15.4, etc
**Improve Test QoR**  
*Higher Test Coverage, Lower Pattern Count*

- Increased access at IP/core periphery
- Higher test quality and pattern efficiency
- Faster development of new tests with hierarchical access

---

**Reduce Test Cost**  
*Optimize Test Time and Power with Flexible Test Scheduling*

* IP/cores with same color are tested in parallel

User configurable test scheduling minimizes test time and cost
Increase Productivity
*Reduce Test Integration Time by Weeks*

- Scalable hierarchical architecture
- Standard interface for all IP/cores
- Rings minimize signal routes and congestion
- Sub-server enables efficient interface and test closure

Concurrent Test: SoC Test Scheduling

Provide optimal test time by concurrent test taking into account the SoC design/test/resource limitations.
Concurrent Test: Types of Constraints and Limitations

- Resource conflict (use of shared TAMs or BISTs)
- Precedence constraints (e.g., IP2 should be run after completing the run on IP1)
- Power and area constraints (e.g., for a BIST run there is a limit on power consumption)

Ramp-up Production Faster – TTV

*Test Patterns, Silicon Repair and Diagnostics*

- Creates tester-ready patterns
- Supports tester-based and interactive silicon debug
- Provides eFuse programming for calibration
- Compliant with 1687 for system level debug
Hierarchical Test Solution Benefits

- Address SoC test bottleneck of large designs/cores-reuse
- Provide uniform interface to users w reduced pin count
- Enable subchip level test closure
- Accelerate Time-to-Volume w ease of silicon debug
- Improve portability for both IP developers and IP users
- Reduce test cost by flexible scheduling and concurrent test
- Increase test quality by porting IP developers’ test solutions

Agenda

- Trends & Challenges
- Hierarchical Test Solution
- IP-Level Test Preparation
- SOC-Level Test Optimization
- Beyond SOC: IEEE Test Standards
- Life-Cycle Test & Diagnosis
- Conclusion
- New Topics
1149.1
Standard Test Access Port and Boundary-Scan Architecture

- Circuit architecture and protocol allowing easy board- and system-level interconnect testing to be automated and applied with limited tester access
- Very widely used test standard
- Basis for "off-shoot" standards
- Defines a BSDL
- Easy chip-level access leveraged for other things
- Recently revised

IEEE Std 1149.1

- Chip hardware and language standard
- Defines TAP (Test Access Port) of 4-5 wires with protocol for scan access
- Defines a boundary-scan register at chip top
- Defines a BSDL for board-level test
- Targeting chip and board test applications
  - Used for system-level access to many chip resources
IEEE Std 1149.1 Connectivity

- Instruction Register selects scan path
- Supports multiple serial data scan paths
- Selected scan path coupled between TDI and TDO pins
- Boundary and Bypass Data Registers are required
What is IJTAG (IEEE 1687)?

- **IEEE 1687**: Standard for Access and Control of Instrumentation Embedded Within a Semiconductor Device
- Hardware Description Language
  - Defines Status/Control registers (memory mapping)
- “Function” Description Language
  - Primitives (Read/Write) and Flow Control
- What 1687 is not:
  - NOT BIST
  - NOT a tool
  - NOT a program

IEEE 1687 Target Objective

- 1687 describes access and control of on-chip “instruments”
  - ICL describes the hardware
  - PDL describes the tests
Language Components of IEEE 1687

<table>
<thead>
<tr>
<th>Information</th>
<th>Language</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Instrument procedures</strong></td>
<td>Procedure Description Language</td>
<td>Documents the procedures to operate an instrument.</td>
</tr>
<tr>
<td><strong>Network description</strong></td>
<td>Instrument Connectivity Language</td>
<td>Documents the logical network which connects the instruments to the chip interfaces.</td>
</tr>
</tbody>
</table>

SOC Test Infrastructure Access – ATE/Board/System

SOC Test Infrastructure

- ATE
- BScan
- Diags
Benefits of 1687

- Enables REUSE of pattern/test
  - Instruments/Blocks / Sub-module / Chip / Board / System
  - ATE, BSCAN, ICT, Diagnosis

- Enables Automation
  - Verification, Test and Debug
  - Test Mapping
  - Test Data Collection

- Consistent/Complete documentation

1500 + 1149.1 = 1687

- 1500 addresses scanned and compression-based cores
- 1500 will support a 1687 application needing small amounts of test data
Signaling

IEEE Std 1500
- WRCK
- WRSTN
- CaptureWR
- ShiftWR
- UpdateWR
- WSI
- WSO
- Implied Select
- SelectWIR
  Selecting between WIR/DR

IEEE Std 1687
- TCK
- Reset
- CaptureEn
- ShiftEn
- UpdateEn
- ScanIn
- ScanOut
- Select
  Enabling access

1687 Connectivity

TDR = JTAG Test Data Register
MUX In and Out Segments

The 1687 SIB
The 1687 SIB

Instruction Register grows longer with every WIR added to scan path
1500 Connectivity

1149.1 + 1500 + SIBs = 1687
Current Language Choices

- CTL can describe the DFT architecture
  - Required for synthesis
- ICL can describe “instrument” access architecture
- New BSDL can describe “instrument” access architecture
- STIL can describe the patterns with embedded protocol
- PDL can describe the patterns with implied protocol
  - PDL is in 1687 and 1149.1

Uses for languages across life cycle

1. IC Simulation
2. IC Silicon Debug
3. IC ATE
4. PCB
5. System Level
6. Field
7. Returns/Repair
Total Hierarchical SOC Test Solution

1500
1450.6
1450

1149.1
BSDL
PDL

1497
ICL
PDL

Agenda

Trends & Challenges

Hierarchical Test Solution

IP-Level Test Preparation

SOC-Level Test Optimization

Beyond SOC: IEEE Test Stnd

Life-Cycle Test & Diagnosis

New Topics

Conclusion
• Field failure diagnosis
• What's really broken
• What's really broken
• Board?
• Package?
• Die?
Agenda

Trends & Challenges
Hierarchical Test Solution

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SOC-Level Test Optimization

Beyond SOC: IEEE Test Stnads
Life-Cycle Test & Diagnosis

New Topics
Conclusion
Reliability Faults

• Intermittent Faults:
  – unstable hardware activated by environmental changes (lower voltage, temperature)
  – often become permanent faults
  – identifying requires characterization
  – process variation – main cause of IF

• Transient Faults:
  – occur because of temporary environmental conditions
  – neutrons and $\alpha$-particles
  – power supply and interconnect noise
  – electromagnetic interference
  – electrostatic discharge

Reliability Faults (cont.)

• Infant Mortality
  – rate worsens due to transistor scaling effects and new process technology and material

• Aging Induced Hard Failures
  – performance degradation over time (burn-in shows)
  – degradation varies over chip-chip and core-core

• Soft Errors
  – Random logic still at risk
  – RAM decreasing SEU per bit

• Low Vmin increases bit failures in memories

• Transient Errors, such as timing faults, crosstalk are major signal integrity problems
Design for Reliability

- Technology
  - Leakage induced power mitigation
- Chip
  - Power mitigation
  - Redundant elements
- System
  - Memory ECC
  - Logic fault tolerance

MCU Growth Over Technology Nodes

Source: iRoC
Robustness IP for ECC

- Standard ECC architecture provides single bit repair
- RAM multi-bit upset probability depends on cell to cell distance
Advanced Transient Error Fault Tolerance

- Transient errors not just limited to space applications
- More likely at 28nm and below process technology nodes

- Highly automated flow
- Multi-bit error detection and correction
- Configurable performance versus area trade-off
- User-defined minimum distance for memory bit interleaving
- Memory banking for wide instances
- Memory correlation with write mask

The Aging Problem

- Today’s applications require large amount of embedded memories that occupy the largest ratio of SOC surface
- It is crucial to guarantee the reliability of such ICs over lifetime
- One of the most important phenomena degrading Nano-scale SRAMs reliability over time is related to Negative bias temperature instability (NBTI), which accelerates memory bit cell aging
**Hierarchical Test Solution**

*Accelerate SoC Testing, Improve Test QoR, Reduce Cost*

- **Increases Productivity**
  - Automated test integration of all IP/cores in SoC
  - Re-use of IP/core-level patterns

- **Improves Test QoR**
  - Higher test quality due to IP pattern efficiency
  - Test programmability with hierarchical access

- **Reduces Cost**
  - Reduced test time with flexible scheduling
  - Improved yield with eFuse based calibration