ACM SIGDA / EDAA PhD Forum at DATE 2014 in Dresden

The ACM SIGDA / EDAA PhD forum is part of the DATE Conference and hosted by ACM SIGDA and the European Design Automation Association (EDAA). It offers the opportunity for PhD students to present their thesis work to a broad audience in the design, automation and test community from academia and industry. During the presentation at the DATE Conference, it helps students to establish contacts. Also, representatives from industry and academia get a glance of state-of-the-art research in design, automation and test. The review process resulted in the selection of the PhD students listed below. We thank ACM SIGDA, EDAA, and DATE for making this Forum possible.

Peter Marwedel (Chair, ACM SIGDA / EDAA PhD Forum at DATE 2014)

PhD Forum Committee

Peter Marwedel (Chair), TU Dortmund, Germany
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Sander Stuijk, TU Eindhoven, Netherlands
Miroslav Velev, Aries Design Automation, Chicago, USA
Norbert Wehn, TU Kaiserslautern, Germany

Admitted Presentations

1. Agathoklis Papadopoulos (University of Cyprus, CY): Accelerating Bioinformatics and Biomedical Applications via Massively Parallel Reconfigurable Systems
2. Angeliki Kritikakou (ONERA, Toulouse, F): Scalable & Near-optimal methodologies for memory management & processing of embedded systems
3. Antonio Salazar (University of Porto, PT): Mixed-signal Test and Measurement Framework for Wearable Monitoring System
4. Anup Das (National University of Singapore, SG): Design Methodology for Reliable and Energy Efficient Multiprocessor Systems
5. Arnaldo Cruz (Kyushu University, JP): Compiler optimization space exploration using machine learning techniques
6. Benoit Vernay (University Pierre et Marie Curie, Paris, F): A Novel Method of MEMS System-Level Modeling via Multi-Domain Virtual Prototyping in SystemC-AMS
7. Daniele Bortolotti (University of Bologna, I): A Process and Environmental Variation Tolerance Scheme for ULP Shared-memory Processor Cluster
8. Danila Gorodecky (Academy of Sciences, Minsk, Belarus): Mathematical Models and Synthesis Methods of Computing Devices in Modular Arithmetic
9. Domitian Tamas-Selicean (Technical University of Denmark, DK): Design of Mixed-Criticality Applications on Distributed Real-Time Systems
10. Emad Ebeid (University of Verona, I): Modeling and Synthesis of the Network in Distributed Embedded Systems

11. Fabian Oboril (Karlsruhe Institute of Technology, D): Cross-Layer Approaches for Aging-Aware Design of Nanoscale Microprocessors
12. Fatemeh Negin Javaheri (TIMA Lab, F): Designing from Assertions: from PSL Properties to a Compliant Hardware Prototype
13. Fazal Hameed (Karlsruhe Institute of Technology, D): DRAM Aware Last Level Cache Policies for Multi-Core Systems
14. Francesco Conti (University of Bologna, I): Heterogeneity exploration in tightly-coupled clusters
15. Jai Narayan Tripathi (Indian Institute of Technology Mumbai, IN): Power Integrity Analysis and Discrete Optimization of Decoupling Capacitors
16. Karthik Chandrasekar (Delft University of Technology, NL): High-Level Power Estimation of DRAMs
17. Lars Middendorf (University of Rostock, D): Dynamic Task Mapping on Multi-Core Architectures using Stream Rewriting
18. Leonidas Kosmidis (Barcelona Supercomputing Center, ES): Enabling Caches in Probabilistic Timing Analysis
19. Luca Cassano (University of Pisa, I): Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs
20. Marco Indaco (Politecnico di Torino, I): Service Oriented Non Volatile Memories
21. Matheus Moreira (Pontifical Catholic University of Rio Grande do Sul, BR): Quasi-Delay-Insensitive Return-to-One Design
22. Mathias Soeken (University of Bremen, D): Formal Specification Level
23. Milan Pavlovic (Barcelona Supercomputing Center, ES): Data Placement in HPC Architectures with Heterogeneous Off-chip Memory
24. Mirela Alistar (Technical University of Denmark, DK): Compilation and Synthesis for Fault-Tolerant Digital Microfluidic Biochips
25. Miroslav Valka (University of Montpellier II, F): Power Aware Test and Test of Low Power Devices
26. Mohamed Bamakhrama (Leiden University, NL): On Hard Real-Time Scheduling of Cyclo-Static Dataflow and its Application in System-Level Design
27. Namita Sharma (Indian Institute of Technology Delhi, IN): Data Memory Optimizations for SPM based Baseband Processor Architectures
28. Nikola Rajovic (Barcelona Supercomputing Center, ES): High Performance Computing with Mobile SoCs: Opportunities and Challenges
29. Norma Montealegre (Heinz Nixdorf Institut, Paderborn, D): Immunorepairing of Hardware Systems
30. Ogun Turkyilmaz (CEA-LETI, Grenoble, F): Using 3D technologies to reduce power consumption of FPGAs
31. Oliver Arnold (TU Dresden, D): Dynamic Task Scheduling for heterogeneous MPSoCs
32. Pydi Bahubalindruni (University of Porto, PT): Analog/Mixed – Signal Circuits using a-GIZO TFTs
33. Robert Reicherdt (Technische Universität Berlin, D): Formal Verification of Discrete-Time MATLAB/Simulink Models using Boogie
34. Saman Kiamehr (Karlsruhe Institute of Technology, D): Cross layer resiliency modeling and optimization: A device to circuit approach
35. Samaneh Ghandali (University of Tehran, IR): High-level Synthesis and Optimization of Datapath-intensive Embedded System Designs
36. Sudip Roy (Indian Institute of Technology Kharagpur, IN): Algorithms for Design Automation of Sample Preparation on Digital Microfluidic Biochips
37. Turbo Majumder (Indian Institute of Technology Delhi, IN): On-Chip Network-Enabled Many-Core Architectures for Computational Biology Applications
38. Vito Giovanni Castellana (Politecnico di Milano, I): C-Based High Level Synthesis of Adaptive Hardware Components