Pass-XNOR Logic: A new Logic Style for P-N Junction based Graphene Circuits

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***Abstract*—In this work we introduce a new logic style for p-n junctions based digital graphene circuits: the *pass-XNOR logic style*. The latter enables the realization of compact, energy efficient circuits that better exploit the characteristics of graphene. We first show how a single p-n junction can be conceived as a *pass-XNOR gate*, i.e., a transmission gate with embedded logic functionality, the XNOR Boolean operator. Secondly, we propose a smart integration strategy in which series/parallel connections of pass-XNOR gates allow to implement AND/OR logical conjunctions, and, therefore, all possible truth tables.**

Experimental results conducted on a set of representative logic functions show the superior of pass-XNOR logic circuits w.r.t. standard CMOS circuits and graphene circuits that use p-n junctions in a complementary-like structure.

I. Introduction and Motivations

Besides its electrical superlatives (i.e., high carrier mobility and saturation velocity in particular [1]), Graphene [2] shows an indisputable limit, that is, *the leak of an energy bandgap* between conduction and valence bands. This characteristic prevents the material to implement the OFF state, also limiting its application in digital devices.

Researchers have explored various solutions to overcome this drawback; the most adopted solution consists of patterning graphene sheets into narrow stripes called graphene nanoribbons (GNRs) [3], [4]. Although even very narrow GNRs exhibit energy gaps sufficiently large for use as a semiconductor to implement Graphene-FETs [5], edge roughness alters the level of disorder of the material and results in significantly degraded device characteristics [6].

An alternative approach consists of a less aggressive strategy based on *electrostatic doping*, which can be used to implement an equivalent graphene p-n junction [7] that serves as basic switch for more complex logic circuits.

However, a graphene pn-junction behaves as a voltage-controlled passive resistor rather than an ideal switch. Therefore it can't compete with FETs if used to implement CMOS-like gates; pull-up/down networks made with passive resistors would imply excessive static power consumption. This aspect clearly imposes a departure from the "complementary" design style adopted in today's Silicon technologies.

This work introduces an alternative logic style, named *pass-XNOR logic*, which efficiently exploits the properties made available by graphene pn-junctions in order to implement more compact, yet less power hungry combinational logic circuits. As will shown later in the text, a single pn-junction intrinsically implements a *pass-XNOR gate*, namely a *transmission gate* with embedded *XNOR* logic functionality. Pass-XNOR gates connected in series/parallel implement AND/OR logic conjunctions, allowing, at a larger scale, the integration of any Boolean logic function. The main characteristic of the proposed PXL style is that, differently from complementary logic families where data are computed stage-by-stage through charges stored in parasitic capacitance, using PXL information are carried out by means of ramp signals propagating through root-to-sink resistive paths, thereby allowing dramatic reduction in the power consumptions.

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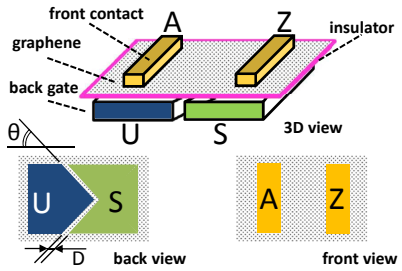


Figure 1. Graphene p-n junction.

Experimental results conducted on a representative set of logic functions show the functionality of circuits implemented with the proposed style, and, most important, their superior w.r.t. circuits built using a complementary-like style. On average we get circuit that are more compact (82% less in the count of active devices), less power hungry (90% of leakage reduction) and faster (82% of delay reduction).

II. Background

A. Graphene P-N Junction

The graphene pn-junction, shown in Figure 1, consists of *(i)* a graphene sheet, *(ii)* two front metal-to-graphene contacts, A and Z, which serve as signal input and output respectively, *(iii)* two back-gates, S and U, isolated from the graphene by *(iv)* a thick layer of oxide.

The voltages applied at the back-gates U and S implement the electrostatic doping [8], [9] of the overlapping Graphene regions: a negative voltage shifts E_F down in the valence band leading p-type doping; a positive voltage shifts E_F up in the conduction band leading n-type doping.

Different doping configurations affect the carrier transmission probability T across the junction, with T defined as the probability that a carrier injected in the junction through the input pin A is collected at the output pin Z.

When U and S are fed with concordant voltages, i.e., same logic value (U, S='00' or '11')[1], the two adjacent graphene

[1]Notice that the 1-logic value is +V_{dd} and the 0-logic value is -V_{dd}

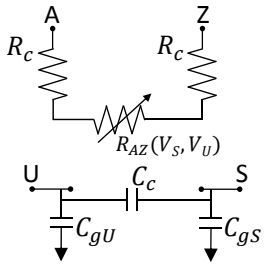


Figure 2. P-n junction electrical model.

regions show same doping profile (pp in case of '00' and nn in case of '11'). Under this configuration the transmission probability is 100%, namely, all the carriers pass through the junction. This represents the ON state.

When U and S are fed with discordant voltages, i.e., opposite logic value (U, S='01' or '10'), the two adjacent graphene regions show different doping profile (pn in case of '01' or np in case of '10'). Under this configuration the Klein tunneling effect comes into play [7] and the transmission probability T is given as:

$$T(\theta) = cos^2(\theta) e^{-\pi \mathbf{k} D \sin^2 \theta} \quad (1)$$

where θ, which is 45° by construction (see Figure 1), is the angle between the electron's wave vector $\mathbf{k}$ and the normal of the junction, D is the metal pitch between the two split back-gates (please refer to the back-view in Figure1). Under this configuration, the transmission probability reduces to a mere 0.003%. This represents the OFF state.

B. Electrical Model

Figure 2 shows a schematic of the electrical model we implemented borrowing the works of [10] and [11]. The resistor R_{AZ} is used to represent the resistive path between input A and output Z. Its value range from $R_{ON} = 300\Omega$, under pp or nn configurations, to $R_{OFF} = 10^7\Omega$, under pn or np configurations, and is analytically expressed as:

$$R_{AZ} = \frac{R_o}{N_{ch} T(\theta)} \quad (2)$$

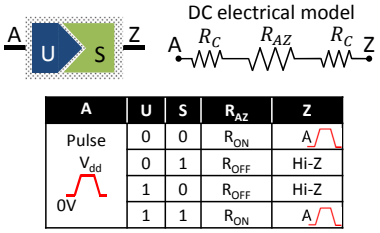
where $T(\theta)$ is given in 1, $R_0 = \frac{h}{4q^2}$ is the quantum resistance per propagation mode, and N_{ch} the number of excited propagation modes[2].

The electrical model also includes parasitics of the metal contacts. The resistors R_c at the front pins A, and Z, model the resistance of the metal-to-graphene contacts [10]. The lumped capacitance C_g at the back-gates (i.e., C_{gS} at S and C_{gU} at U) consists of the series of the oxide capacitance C_{ox} and the quantum capacitance of the graphene sheet C_q, i.e., $C_g = 1/(C_{ox}^{-1} + C_q^{-1})$.

III. Previous Works

The idea of using graphene pn-junctions for digital applications has been firstly introduced in [10], where the authors propose the use of two adjacent pn-junctions to implement a multi-function gate that can be electronically reconfigured; proper interconnections of such multiple gates with an appropriate input configurations allow to implement a full library of logic gates. The experimental results reported in [10] itself, and successively also in [13], indicate that graphene gates based on pn-junctions can outperform CMOS technologies in terms of both delay and power consumption. Only few other recent works, [11] and [12], deal with pn-junction circuits and propose some more abstract model at the gate-level. To the best of authors knowledge, the idea of pass-XNOR gates and pass-XNOR logic is presented here for the first time.

[2]A detailed discussion of the electrical model is out of the scope of this work; interested readers can refer to prior works [10], [12] for additional details.



A	U	S	R_{AZ}	Z
Pulse (V_{dd} / 0V)	0	0	R_{ON}	A
	0	1	R_{OFF}	Hi-Z
	1	0	R_{OFF}	Hi-Z
	1	1	R_{ON}	A

Figure 3. Functional behavior of the pass-XNOR logic gate.

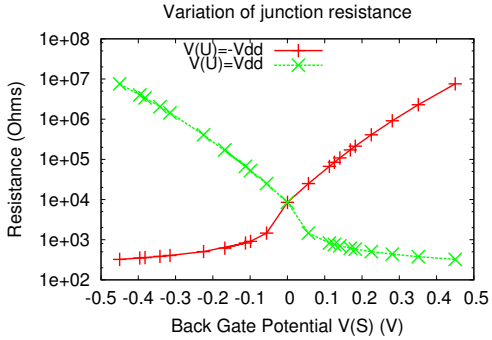


Figure 4. R_{AZ} vs. voltage at the back-gate S

IV. Pass-Xnor Logic

A. Pass-XNOR Gate

The pass-XNOR gate simply consists of a p-n junctions where the back-gates U and S are fed with the digital input signals, while the front contacts A and Z work as source and drain of a stimulus ramp pulse used to evaluate the logic function.

As shown in Figure 3, when U and S have same logic value, the equivalent in-to-out front resistance R_{AZ} is set to R_{ON} leaving the input pulse on A passes through the junction reaching Z; this represents the '1'-logic at the output. Opposite logic values, on the contrary, set the in-to-out front resistance R_{AZ} to $R_{OFF} (\gg R_{ON})$, forcing Z in a high-impedance state; this represents the '0'-logic at the output.

Notice that the transition of R_{AZ} from R_{ON} to R_{OFF} is a non-linear function of the back-gate voltages. Figure 4, obtained using the Verilog-A model discussed in Section II, plots R_{AZ} vs. the voltage at gate S when U is fed with a '0'-logic, i.e., $-V_{dd}$ (solid line), or '1'-logic, i.e., V_{dd} (dotted line). As one can observe, the larger the voltage difference between U and S, the larger the equivalent resistance.

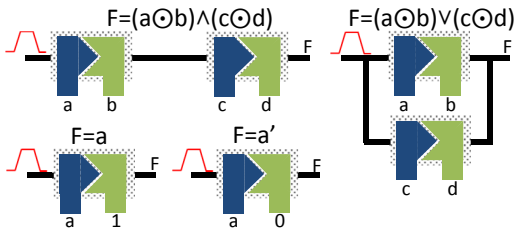


Figure 5. Basic logic functions using the pass-XNOR gate.

B. Building Complex Functions

The pass-XNOR gate shows a higher expressive power compared to the CMOS counterparts as it requires a smaller number of devices to implement XNOR/XOR-dominated logic functions. Unfortunately, the XNOR operator per se is not *functional complete* and other logic connectives are needed.

Figure 5 shows possible network topologies used to implement the *AND/OR* conjunctions, the logical *Identity* and the *Complement*. Combinations of these four basic Boolean operators allow to express all possible truth tables.

Series connections of the front contacts perform the logic AND. In the example reported in Figure 5 (topmost left), the input pulse injected in the network propagates up to the output iff *both* the pass-XNOR gates are ON, namely, when $(a \odot b) \vee (c \odot d)$. Parallel connections of the front contact, instead, perform the logic OR. In the example reported in Figure 5 (right), the input pulse injected in the network propagates up to the output when *at least one* of the pass-XNOR gates is ON, namely, when $(a \odot b) \wedge (c \odot d)$. Finally, connecting one of the back-gates to '1' or '0' allows to implement logical *identity* or *complement* respectively. In the examples reported in Figure 5 (bottom left), the input pulse propagates toward the output when $a = 1$ if the back-gate is fed with '1', and when $a = 0$ if the back-gate is fed with '0'.

C. Logical Computation through a pass-XNOR Logic Network

The logical computation consists of two distinct phases: the *configuration phase* and the *evaluation phase*. In the configuration phase the primary logic inputs, i.e., the literals composing the logic function, are fed to the back-gates of the pass-XNOR gates. At the end of this phase the doping profile of each and every device is fixed and the resistive paths of the network set up. In the evaluation phase, the input ramp pulse is injected in the network through the front input, i.e., the root of the network, and eventually propagated to the front output. A pulse detected at the front output evaluates the implemented function as TRUE.

Notice that the front input is unique, therefore, only one single front signal is shared among all the parallel branches of the network. As for the CMOS technology, multiple-output functions need distinct logic networks.

D. Preliminary Delay and Power Modeling

The total delay D_p of a pass-XNOR logic circuit can be estimated as the sum of delays due to the configuration phase D_{conf} and the evaluation phase D_{eval} ($D_p = D_{conf} + D_{eval}$). D_{conf} is the time primary logic inputs take to charge the parasitics capacitance at the back-gates, whereas D_{eval} is the propagation delay of the input pulse through the front resistive paths of the network.

Concerning the static power consumption, it is worth emphasizing that during the configuration phase and the idle periods, the front input ramp signal is quiescent, i.e., frozen at 0V. This implies a zero potential difference between front input and front output of the circuit, hence, *zero static power consumption*, which is the key strength of the proposed logic style.

The main contribution to static power is given by the tunneling current at the back-gates, similar to the gate current of MOSFETs. The analytical expression is given as $P_{static} = \sum_i^{2N} I_g$, where N is the number of pass-XNOR gates, each of them with two back-gates, and I_g as the tunneling current through a single back-gate.

Also the total dynamic power consumption can be estimated as the sum of the two contributions during the configuration P_{conf} and the evaluation phase P_{eval} ($P_{dynamic} = P_{conf} + P_{eval}$). P_{conf} is due to charging/discharging the input gate capacitance at the back-gates (similar to the input power consumed by CMOS gates); P_{eval} is the power consumed when charging/discharging the capacitive load at the front output. Since a pass-XNOR network simply reduces to an equivalent resistor R_{eq} (calculated as series/parallel connections of R_{ON} and R_{OFF} depending on the back-gates configurations) in series with the load capacitance C_l. Hence the instant power consumed across the resistor mesh can be calculated as $P_{eval}(t) = R_{eq} i^2_{C_l}(t)$, with i_{C_l} the current finally injected into C_l. The average value can be therefore obtained as:

$$P_{eval} = \frac{1}{t_{rf}} \int_0^{t_{rf}} R_{eq} i^2_{C_l}(t) dt = \frac{R_{eq} C_l}{t^2_{rf}} C_l V^2_{dd} \qquad (3)$$

where t_{rf} is rise/fall output transition time, and $i_{C_l}(t)$ is the current charging C_l. Notice that P_{eval} is consumed only for input pattern configuration which make the logic function TRUE, while it is zero otherwise. As for delay estimation, in this work we use accurate SPICE simulations to estimate R_{eq}, $i_{C_l}(t)$, and hence P_{eval}, but analytical models are part of on-going research.

V. Simulation Results

Demonstrating the superior properties of graphene pn-junctions w.r.t. standard MOS technologies is out of the scope of this work (readers can refer to pioneering works, e.g., [10], for a more accurate analysis). What is essential in this context is to prove that the proposed logic style well fits the characteristics made available by the graphene pn-junctions, thereby allowing the implementation of circuits more compact and less leaky. For this purpose, we provide a three-way analysis between *(i)* graphene circuits implemented using the pass-XNOR logic (PXL) presented in this paper, *(ii)* graphene circuits implemented using a complementary logic style (CXL) where pass-XNOR gates are used to form pull-up/down network like in CMOS gates, *(iii)* silicon circuits implemented using a standard CMOS technology and minimum sized transistors (CMOS). The analysis between PXL and CMOS aims at quantifying the area savings one can achieve using primitives with higher expressive power; whereas the analysis between PXL and CXL, which fairly use the same XNOR logic primitive, aims at quantifying the power savings obtained with the proposed logic style.

Table I. BOOLEAN FUNCTIONS WITH NO MORE THAN THREE SERIES DEVICES.

	Function		Function
F00	$\bar{a}$	F23	$a + (b \odot d) \cdot c$
F01	$a \odot b$	F24	$(a \odot d) + (b \odot d) \cdot c$
F02	$a + b$	F25	$a + (b \odot d) \cdot (c \odot d)$
F03	$a \cdot b$	F26	$(a \odot d) + ((b \odot d) \cdot (c \odot d))$
F04	$(a \odot b) + c$	F27	$(a \odot d) \cdot b \cdot c$
F05	$(a \odot b) \cdot c$	F28	$(a \odot d) \cdot (b \odot d) \cdot c$
F06	$(a \odot b) + (a \odot c)$	F29	$(a \odot d) \cdot (b \odot d) \cdot (c \odot d)$
F07	$(a \odot b) \cdot (a \odot c)$	F30	$(a \odot d) + (b \odot e) + c$
F08	$(a \odot b) + (c \odot d)$	F31	$(a \odot d) + (b \odot d) + (c \odot e)$
F09	$(a \odot b) \cdot (c \odot d)$	F32	$((a \odot d) + (b \odot e)) \cdot c$
F10	$a + b + c$	F33	$((a \odot d) + b) \cdot (c \odot e)$
F11	$(a + b) \cdot c$	F34	$((a \odot d) + (b \odot d)) \cdot (c \odot e)$
F12	$a + (b \cdot c)$	F35	$((a \odot d) + (b \odot e)) \cdot (c \odot d)$
F13	$a \cdot b \cdot c$	F36	$(a \odot d) + ((b \odot e) \cdot c)$
F14	$(a \odot d) + b + c$	F37	$a + ((b \odot d) \cdot (c \odot e))$
F15	$(a \odot d) + (b \odot d) + c$	F38	$(a \odot d) + ((b \odot e) \cdot (c \odot e))$
F16	$(a \odot d) + (b \odot d) + (c \odot d)$	F39	$(a \odot d) + ((b \odot e) \cdot (c \odot d))$
F17	$((a \odot d) + b) \cdot c$	F40	$(a \odot d) \cdot (b \odot e) \cdot c$
F18	$((a \odot d) + (b \odot d)) \cdot c$	F41	$(a \odot d) \cdot (b \odot d) \cdot (c \odot e)$
F19	$((a \odot d) + b) \cdot (c \odot d)$	F42	$(a \odot d) + (b \odot e) + (c \odot f)$
F20	$((a \odot d) + (b \odot d)) \cdot (c \odot d)$	F43	$((a \odot d) + (b \odot e)) \cdot (c \odot f)$
F21	$(a + b) \cdot (c \odot d)$	F44	$(a \odot d) + ((b \odot e) \cdot (c \odot f))$
F22	$(a \odot d) + (b \cdot c)$	F45	$(a \odot d) \cdot (b \odot e) \cdot (c \odot f)$

For this study, we limited our experiments to circuits having no more than three pass-XNOR gates in series; the obtained Boolean expressions are listed in Table I. All the simulations were run using Synopsys HSPICE. Graphene circuits have been mapped using the electrical model presented in Section II written in Verilog-A; for CMOS we resort to an industrial 40nm-MOSFET SPICE card model.

Table II gives a comprehensive resume of the collected simulation results. Detailed analysis for each benchmark has been omitted for the sake of space, but similar trends have been recognized. The table shows numbers of devices ($\#devices$), total area ($Area$), worst-case propagation delay (D_p)[3], total leakage power (P_{leak}), total dynamic power (P_{dyn}), averaged over all the 46 logic benchmarks (Table I).

Circuits implemented using the PXL style require 83% less devices w.r.t. CMOS, resulting in a total area savings of 98%. This is due to the fact that a single pass-XNOR gate can implement multiple logic functions taking a smaller amount of active layout area. Moreover, due to the intrinsic properties of graphene, PXL circuits are 83% faster than CMOS, still with a marginal increase of dynamic power consumption (only 8%). Such power overhead can be reduced by tuning the slew-rate of the input ramp (the adiabatic principle demonstrated in [14]). The reported savings are clear expression of the superiority of the pass-XNOR gates, both in terms of expressive power and electrical performance. We expect even larger savings as MOS technologies approach more scaled nodes [10].

Concerning the efficiency of the proposed logic style, one can observe how PXL circuits show 90% less leakage current w.r.t. CXL ones. Such a huge difference is mainly due to the different structure of the two networks: while for PXL circuits the leakage current is only given by tunneling currents through the back-gates, in CXL circuits leakage is induced by static currents flowing through the existing resistive path between the power supply rails. Moreover, PXL circuits are 82% faster than the CXL counterparts, still guaranteeing substantial dynamic power savings, i.e., 51%.

[3]For PXL, the D_p is measured as described in Section IV; for CXL and CMOS as typically done in standard CMOS gates.

Table II. SIMULATION RESULTS AVERAGED OVER THE 46 BENCHMARKS

	$\#devices$	$[Area]\ um^2$	$[D_p]\ ns$	$[P_{leak}]\ \mu A$	$[P_{dyn}]\ \mu W$
PXL	2.74	0.52	8.9	10.96	219.57
CXL	5.48	1.05	50.44	102.7	444.89
CMOS	16.04	22.3	53.86	9.62	204.05

VI. CONCLUSIONS AND FINAL REMARKS

We presented the *pass-XNOR logic* style, a new integration strategy that enables the implementation of compact and energy-efficient graphene digital circuits based on electrostatically controlled p-n junctions. SPICE-level simulations prove that PXL circuits are more compact, less power hungry (90% of leakage reduction) and faster (82% of delay reduction) than graphene circuits implemented using a standard complementary logic style.

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