Reconfigurable Silicon Nanowire Devices and Circuits: Opportunities and Challenges

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Abstract— **Reconfigurable fine-grain electronics target an increase in the number of integrated logic functions per chip by enhancing the functionality at the device level and by implementing a compact and technologically simple hardware platform. Here we study a promising realization approach by employing reconfigurable nanowire transistors (RFETs) as the multifunctional building-blocks to be integrated therein. RFETs merge the electrical characteristics of unipolar n- and p- type FETs into a single *universal* device. The switch comprises four terminals, where three of them act as the conventional FET electrodes and the fourth acts as an electric select signal to dynamically program the desired switch type. The transistor consists of two independent charge carrier injection valves as represented by two gated Schottky junctions integrated within an intrinsic silicon nanowire. Radial compressive strain applied to the channel is used as a scalable method to adjust n- and p- FET currents to each other, thereby enabling complementary logic circuits. Simple but relevant examples for the reconfiguration of complete gates will be given, demonstrating the potential of this technology.**

Keywords— *Reconfigurable transistor, RFET, nanowire, Schottky FET, reconfigurable circuit, inverter, doping free CMOS, symmetric FET, universal transistor*

I. INTRODUCTION

Reconfigurable nanowire electronics target an extension of the number of functions per device and logic building block, thus holding the promise of advancing computing beyond conventional Moore's scaling. Reconfigurable field effect transistors (RFETs) are the central elements responsible for delivering *fine-grain* re-programmability, i.e. a change in logic function of a circuit takes place upon the modification of the individual devices integrated therein. This is in contrast to *large-grain* reconfiguration, where information is routed to pre-arranged circuit blocks. Amongst different fine-grain approaches like memristive devices, RFETs are such four-terminal devices that deliver n- and p- FET switching characteristics from the same device as selected simply by an electric signal. Thereby, interconnected circuits built from RFETs can alter their function on the fly by selecting the inherent configuration of the building blocks.

The RFETs rely on the unique properties of nano-scale Schottky junctions in nanowires to adjust the charge carrier polarity and concentration. An important feature is that no doping is required and that the source and drain contacts are metallic. This has the potential to enable a lean technology. In addition, this could reduce variability as well as the access resistance and fringe capacitances.

In this manuscript we will review and analyze the current progress in reconfigurable nano-electronics towards the implementation of circuits considering the current challenges and opportunities that arise with this new paradigm. At first we will elucidate the electric characteristics and working principle of the nanowire RFETs. The physical working mechanism will be described in detail, through device simulations and electrical characterization. The methodologies used to successfully adjust the on-currents for p- and n- type program will be described, as this is the key requirement to implement energy efficient complementary circuits. Simple complementary demonstrator circuits will be presented. Finally, the opportunities arising from added functionality and challenging management of the increased number of control signals for digital circuit design will be discussed in the example of a compact NAND/ NOR reprogrammable circuit block. It will be shown that by combining a conventional interconnect strategy with a pseudo pass-logic implementation a strategy for REFTs can be found without comprising the functionality gained. This is a first step towards the realization of the vision of a variable structure computing [1] with RFET elements.

II. THE QUEST FOR THE UNIVERSAL CMOS SWITCH

Energy efficient complementary metal oxide semiconductor (CMOS) circuits as implemented over the last four decades have relied on integrated electron (n-type) and hole (p-type) conducting FETs with static switching functions. The different polarity of the charge carriers is decisive to alternate switching of p- and n-type FETs during a single gate-voltage swing. The overall power consumption is thus basically limited to the switching event. The recent advances in one-dimensional electronics have enabled the conception of novel FETs with n- and p-type programmable functions. This lifts the
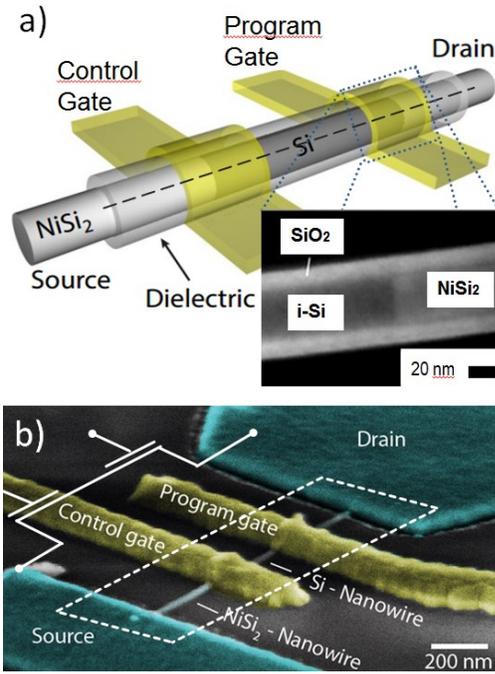
Fig. 1. The reconfigurable silicon nanowire FET with independent junction gating. a) Schematic of the device. Two independent gates are positioned on top of the source and drain junctions. Inset shows SEM of typical cross-section at the Schottky contacts, exhibiting abrupt junction with well defined area. b) SEM image of device after top gate deposition. Inset depicts device symbol.

necessity of having circuit building blocks with a pre-defined polarity at a specific location in circuits. Accordingly, novel and disruptive circuit schemes are necessary to benefit from the higher functionality and to tackle the inherent overhead of control signals present, compared to conventional CMOS.

An electronic switch that *universally* delivers n- and p- type operation upon demand has to fulfill a series of requirements to be applicable to build circuits and systems. These will be addressed in this paper and can be summarized as follows:

- Reversible configurability as n- and p- type FET
- Symmetric characteristics and p/n-FET on-currents
- Sufficient drivability strength for neighboring FETs
- Single supply voltage
- Scalability

In general, the charge carrier type that flows through conventional FETs is selected by the doping profiles, e.g. *n-p-n* / *n-i-n* for n-channel and *p-n-p* / *p-i-p* for p-channel. As device dimensions are continued to be reduced and 3-D channel structures are implemented, an accurate and reproducible control of the doping distribution and doping efficiency is of increasing difficulty [2]. In contrast to doping, the first requirement listed above involves that electrons and holes are to be injected into the intrinsic or lowly doped channel from the source and drain electrodes.

Therefore, the highly doped source and drain regions in conventional FETs are replaced by metallic contacts that ideally align their work function near the mid-energy of the

band gap. In this respect it will be shown that RFETs are an interesting technological alternative, as they do not require doping. Moreover, the first requirement demands a mechanism for selective filtering or preferential injection of charge carriers depending on the desired polarity. Different realization procedures have been presented recently and are summarized and compared in the next section. This paper will show that the nanowire RFET concept with individual source/drain gating fulfills all of the requirements listed above.

III. RECONFIGURABLE NANOWIRE FETs: DEVICE PRINCIPLES AND SYMMETRIC OPERATION

Recently, several reconfigurable transistor concepts have been reported. These have employed different nano-scaled channel materials such as carbon nanotubes (CNT) [3], intrinsic or lowly doped silicon [4-9] and graphene [10, 11]. In all cases Schottky junctions were provided at S/D and a gate potential was used to directly control band bending at the Schottky interface providing predominant charge carrier injection into the valence or conduction bands. There are basically three different implementations to provide tunable polarity. In the first approach [3, 7-9] both Schottky junctions are steered simultaneously, accumulating either holes ($V_g < 0$) or electrons ($V_g > 0$) in the channel and thus programming the device polarity. An additional gate positioned in the middle of the channel adjusts the flow of charge carriers from source to drain. In a second realization [4], the same structure can be steered differently. Sweeping the gates at the source and drain gives rise to an ambipolar characteristic, like in a regular Schottky barrier FET. The middle gate programs the device polarity by blocking the undesired carriers in the middle of the channel. In the third approach [5, 6], the Schottky source and drain junctions are gated independently from each other and no gating in the middle of the channel is needed. There, one gate can block the undesired charge carriers prior to their entrance into the channel, thus programming the device polarity. The other gate is used to tune conductance of the other charge carrier kind.

Polarity control has been achieved with all concepts, thus addressing the first requirement for a *universal* FET listed in *Section II*. The different solutions show significant differences in the device behavior and transport properties of the individual concepts. These have been compared elsewhere [12]. In the next paragraphs we will focus on describing the RFET with independent junction gating, as this device is the only one known to us, that has been brought up to the level of exhibiting symmetric characteristics and complementary operation in circuits.

Figure 1 depicts the RFET nanowire concept first introduced in our previous work [5, 6]. The transistor is composed of a core nanowire that accommodates source, channel and drain in a longitudinal metal-NiSi$_2$ / intrinsic-Si / metal-NiSi$_2$ heterostructure [13]. The nanowire heterostructure is surrounded by an electrically insulating SiO$_2$ dielectric. Characteristic elements of the RFET are the two separate gate structures that directly overlap the NiSi$_2$ to Si junctions. These

a)

b)
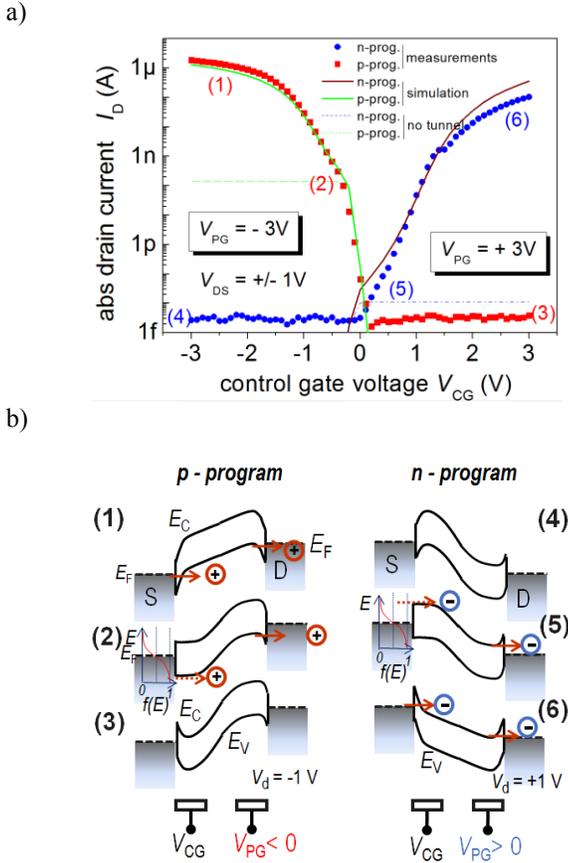
Fig. 2.   a) Subthreshold transfer characteristics of a nanowire RFET. The device can be programmed to perfom as a unipolar p- or n- type FET as set by the program gate potential V_{PG}. Characteristics from the device in [6]. Dots are measurement points, solid lines simulation results. Dashed lines show I_d neglecting barrier tunneling. b) Corresponding schematic band diagrams for different operation regions, labeled (1) – (6). The states are correlated to specific regions of the subthreshold characteristics in a).

gates are operated independently from each other enabling individual control of charge transport through each junction. The working principle of the RFET can be viewed as a Si nanowire channel with two tunable *charge injection valves* at both ends. These are the ones responsible for controlling the polarity and charge density of the REFT. The nanowire metal to semiconductor – Schottky - junctions themselves exhibit a very characteristic attribute. They can be built with a sharpness in the sub-nanometer range [13] and can ultimately reach the abruptness of an atomically sharp interface [14]. Accordingly, the junction area is well defined by the nanowire diameter. In contrast to bulk-Si / NiSi$_x$ interfaces, there are no local protrusions that could create substantial electric field variations within the junction. The nanoscopic junction introduces a Schottky barrier at the interface, energetically located near the Si midgap, see schematic band diagram in Fig. 2 b. As shown elsewhere, the Schottky barrier height determined for holes is qφ_p = 471 meV and for electrons qφ_n = 649 meV [12]. This is near to the literature values known for bulk NiSi$_2$ / Si junctions: ranging between 660 - 750 meV for electrons [15, 16]. As the nanowire channel is nominally undoped, the large majority of charge carriers are injected from the metallic NiSi$_2$ leads. Charge injection is controlled by changing the shape of

the Schottky barrier. The application of a local electric gate field bends the silicon bands at the junction. Transport through the junction is thus adjusted between thermionic emission over the barrier and quantum mechanical tunneling through the barrier (details below).   Although the geometric device structure is completely symmetric, we deliberately label the gates as *control-* and *polarity-gate* to facilitate the description of the working principle of RFETs.

Figure 2 a depicts the subthreshold transfer characteristics of a typical RFET with independent junction gating. The device is built from bottom-up synthesized intrinsic nanowires as described in [13, 17]. This is a technological vehicle that can be transferred to top-down Si processing as demonstrated in [7]. The nanowire channel has a thickness of 20 nm, 680 nm in length   and exhibits the <112> crystal direction. It is surrounded by a 10 nm thermally grown SiO$_2$ shell as the gate dielectric. The Ti/Al top metal electrodes are patterned and aligned to the Schottky junctions [6].

The RFET is programmed electrically in n- or p-FET configuration, according to the voltage applied at the polarity gate. The control gate takes the function of a regular gate electrode in a conventional FET. The corresponding schematic band diagrams for the individual operation states as labeled in the subthreshold characteristics are sketched in Fig. 2 b. For programing the p- type behavior, the program gate voltage is constantly biased at V_{PG} = -3 V and V_d= -1V. The negative program gate potential rises the conduction band edge E_c at drain increasing the barrier height for electrons well above the value of the *natural* Schottky barrier height. Thermionic emission of electrons into Si is therefore practically blocked. Note that, due the height and thickness of this barrier it becomes also practically opaque for tunneling. At the opposite side of the nanowire, the control gate is swept to adjust hole injection at the source-sided junction. For V_{CG} < 0 V the valence band edge E_v is bent upwards, substantially thinning down the E_v barrier thickness. The barrier height is basically the natural Schottky barrier height for holes with a slight decrease due to the Schottky effect [15]. For V_{CG} = -3 V quantum mechanical tunneling and thermal assisted tunneling of charge carriers from source into E_v take place. This state (state 1) corresponds to the on-state of the p-type charac-teristic. Moreover, increasing V_{CG} to the flat band condition (state 2) thickens the barrier and quenches tunneling. This readily reduces conductance by 4 orders of magnitude. Further increasing V_{CG} to +3V practically blocks thermionic emission into the valence band, shutting off the remaining hole diffusion current over the barrier by a further 3 orders of magnitude (state 3). The transfer characteristic indeed resembles that of a p-type enhancement mode FET.

To program the n-type enhancement characteristic all potentials are simply mirrored, i.e. V_{DS} = +1 V and V_{PG} is reversed and kept constant at V_{PG} = + 3 V. For V_{PG} > 0 V, E_v at drain   is lowered to block thermal emission of holes. The control gate voltage V_{CG} in turn controls the injection of electrons from source into the channel. For V_{CG} > 0 electrons tunnel through the thinned barrier at source into the Si nanowire and are consecutively injected out at drain, giving the on-state of the n-type FET (state 6). Electron tunneling from

a)

b)
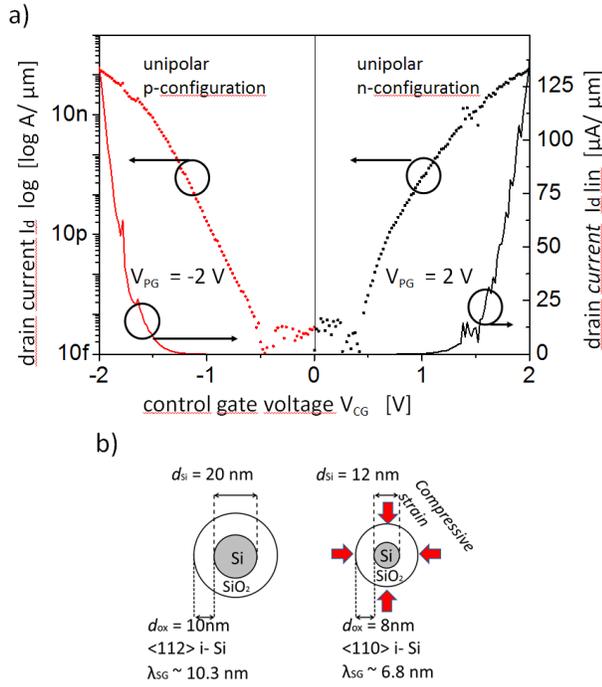
Fig. 3. Symmetric n- and p- unipolar characteristics of optimized RFET with <110> nanowire orientation, 12 nm diameter and 1.3 GPa of radial compressive strain. Device seen in Fig. 1 b. a) Adjustment of transfer characteristics by application of radial compresive strain. As a consequence, the currents for n-type and p-type from the same device are the equal. Drain currents are normalized to the nanowire diameter. b) Schematic device cross section for non-optimized device in Fig. 2 a and optimized device in Fig. 3 a.

source is practically inhibited when a lower V_{CG} sets the flat band case (state 5).The remaining thermionic emission is quenched for $V_{CG} < 0V$ (state 4). In general it can be stated that the polarity gate blocks the undesired carrier type, regardless of the applied tuning gate potential (within reasonable limits of the applied voltage). Thus V_{PG} dynamically programs the p- or n- type behavior of the device. In both cases V_{CG} controls the conductance through the nanowire in a similar manner that a conventional MOSFET does.

The total modulation for the p-program (n-program) configuration is $1x10^9$ ($6x10^7$). The maximum on current I_{on} is -1.9 µA (94 µA µm^{-1}) and 1.1 x 10^{-7} A (5.3 µA µm^{-1}) for p-type and n-type mode respectively which gives a maximum current density, J_{Dmax}, of 600 kA cm^{-2} and 34 kA cm^{-2} respectively. The scaled peak trans-conductance amounts to 6 mS µm^{-1} (p-type) and 7.5 nS µm^{-1} (n-type FET). The inverse subthreshold slope, S, reaches values as low as 90 mV dec^{-1} for the p-programmed mode. For the n-programmed mode the lowest measured S is 220 mV dec^{-1} as it is determined in the state where tunneling dominates [18].

Device simulations (Sentaurus Device) were performed to validate and interpret the measurement results. A 3D drift diffusion model is used. Tunneling currents are calculated by the Wentzel-Kramers-Brillouin (WKB) approximation. The computed $I_D - V_{CG}$ characteristics mimic the measured behavior for both p- and n- program (solid curves in Fig. 2 a). The simulations also reproduce well the characteristic *kink* in

the subthreshold region, typical to Schottky FETs. In this region, flat band conditions are found at the source electrode, i.e. the barrier height amounts to the *natural* Schottky barrier height [18]. If no tunneling is considered, I_d starts to saturate as indicated by the dashed lines. Accordingly, the on-state and the upper subthreshold region are dominated by the tunneling transmission through the barriers. This means that an additional enhancement or adjustment in currents can take place by adequately tuning the tunneling parameters.

Despite the excellent polarity control shown in Fig. 2 circuit implementation requires symmetric *I-V* characteristics. In particular the drive currents for n- and p- configurations differ almost by a factor of 10. In addition, the magnitude threshold voltages and the subthreshold slopes are unequal. These deficiencies are mainly attributed to the different barrier height for electrons and holes [15, 16]. A straightforward solution would be to implement S/D contacts that exactly align their Fermi level to the channel´s midgap energy. Nevertheless, this still leads to different n- and p- type currents given the differences in the injection efficiency and channel mobilities of electrons and holes [19]. In view of a scalable technology further variation of mobilities and differences in the tunneling transmission arising from different nanowire channel dimensions should be compensated. Although it is possible to obtain different barrier heights between NiSi$_x$ and silicon through different crystal orientations and formation temperatures [20, 21] a fine degree of tunability of the Schottky barrier heights would be necessary. At the present state of technology this could only be realized by introducing controllable dopant distributions at the junctions, either by activated dopants [15] or segregated dopants [22]. As doping control is increasingly difficult in nanometer scale dimensions [2] an alternative scalable method is required.

The relevant working region of an FET for logic applications is around the threshold voltage. The simulations of our RFETs in Fig. 2 a indicate that this region is governed by quantum mechanical tunneling through the barriers. Our approach to adjust currents for n- and p-type FETs is to fine-tune the injection of electrons and holes through the barrier by the application of radial compressive strain [23]. In our particular case the n- currents need to be enhanced. Calculations [24] have shown, that radial compressive strain lowers the electron effective masses m_n^* and thus enhances electron mobility for <110> oriented channels. At the same time hole effective masses m_p^* are increased. By tuning m_n^* to m_p^* ratio with the application of radial compressive strain, the tunneling probability through the barrier T can be adjusted according to Eq. 1:

$$T_{n,p} \propto e^{\frac{-4\sqrt{2m_{n,p}^*}\varphi_{n,p}^{3/2}}{3q\hbar E}} \quad (1).$$

Equation 1 is the WKB approximation for a triangular barrier [15] of height $q\varphi_{n,p}$ and applied field electric E across the junction, where $\hbar$ is the reduced Planck´s constant.
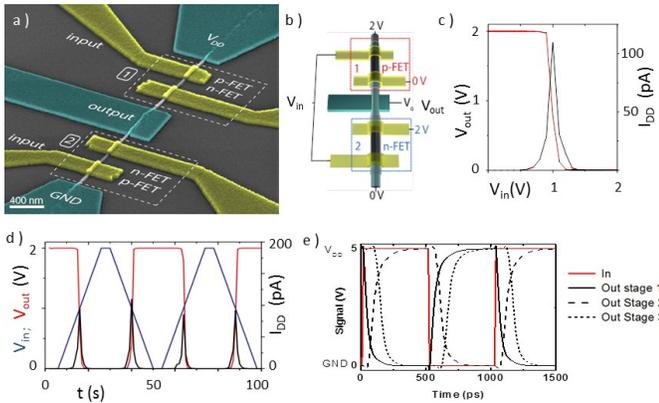
Fig. 4. Complementary inverter integrated into a single nanowire string. a) SEM image. b) One possible configuration top device: p-FET, bottom n-FET. c) Measured transfer characteristic exhibiting full-swing output and sharp transition at $V_{DD} / 2$, where cross-current flows. d) Stable V_{out} transitions in the time domain. c) Cascadability of three cascaded inverter stages as calculated by mixed-mode simulations, here $V_{DD} = 5$ V. The output of the second stage shows that RFETs built of individual nanowires principally deliver sufficient on-current to be cascadable.

To optimize our devices, we thus chose <110> oriented nanowires [17]. Radial compressive strain was introduced through self-limited oxidation of the nanowires [25]. Nanowire based devices were built with varying strain incorporation by changing the oxidation temperature and initial nanowire diameter. Symmetric transfer characteristics were obtained for devices with 1.3 GPa of radially compressive strain [23], see Fig. 3a. The nanowire channel exhibits a length of 220 nm and diameter of 12 nm. It is surrounded by a 8 nm thick SiO_2 shell. Compared to the non-optimized device (see dimensions Fig. 3b) in Fig. 2a, n-drive-currents were enhanced by almost one order of magnitude. In turn, p- currents dropped slightly as expected. The magnitude of threshold voltages V_{th-p} / $V_{th-n} = -1.41$ V / 1.42 V and subthreshold slopes 150 mV/dec are also remarkably equivalent for p- and n- configurations. Note that in addition to the adjusted effective masses, a slight shift in $q\varphi_n$ is expected, as the conduction band edge E_c is lowered by radial compressive strain [24]. This further enhances electron tunneling and also shifts the transition between Schottky emission and tunneling.

The devices obtained are the first transistors of any kind and any material known to us to provide symmetric characteristics for n- and p- from a structure with the same sizing ratio and material composition that is steered with a single supply voltage. The symmetric operation is the key enabler to leverage the value of RFETs for realizing low-power complementary circuit applications.

IV. COMPLEMENTARY CIRCUITS FROM RFETs

Having devised symmetric nanowire RFETs the path to build complementary circuits is opened. At first complementary inverter circuits have been built along single nanowires [23] as shown in Fig. 4a. One of the devices can be

programmed to perform as p-FET ($V_{CG} = 0$V) in the *pull-up* network whereas the other one performs as n-FET ($V_{CG} = 2$V = V_{DD}) in the *pull-down* network as shown in the schematic of Fig 4b. The transfer characteristic (Fig. 4c) indeed shows full signal inversion with a sharp transition at $V_{in} = V_{DD} / 2$ as a result of complementary operation. Substantial currents only flow while switching, further confirming the complementary nature of the circuit. Measured time dependent switching characteristics are shown in Fig 4 d). To study the circuit's response at shorter timescales and to investigate the driving strength of the inverter when cascaded, mixed mode calculations where performed with the *Sentaurus Device* simulator. Thereto, a 3-D drift diffusion model of the symmetric RFETs from Fig. 2 described in Ref. [19] was employed. AC small signal capacitance voltage (C-V) analysis was used to extract gate capacitances, acting as load at the output to account for the input of the next inverter stage amounting to $C_L = 30$ aF (1.2 fF / µm normalized to the gate width, here the nanowire circumference). Figure 4e shows the response of three cascaded inverters with a capacitive load of 30 aF. The circuit shows a delay of 35 ps at the first stage and 142 ps after all three stages. These performance metrics represent an initial assessment as needed to analyze their impact in circuits, however note that the device geometry has not been optimized yet with respect to capacitive coupling and length of the active region. Also note that comparable results were obtained when programming the devices alternatively: top device as n-FET ($V_{CG} = 2$V), bottom device as p-FET ($V_{CG} = 0$V) and flipping V_{dd} and GND with each other. This is an important result when designing circuits in a *pass-logic* approach where a strict separation between data paths and supply lines is lifted. It is also important to mention, that in contrast to all other reconfigurable approaches presented up-to-date these circuits are realized with the application of a single supply voltage.

V. RECONFIGURABLE LOGIC GATES

The RFET concept discussed above simplifies the technology by merging two different device technologies into a single lean one, that doesn't even require doping. Moreover, for beyond CMOS applications RFETs are promising candidates to enable novel approaches at the circuit design and system level. This can be best illustrated by the investigation of logic circuit blocks that can alter their logic function. It has already been shown by De Marchi et al. that two RFETs connected in series as in an inverter (see fig. 4b) can also perform as an XOR gate when employing the program gate as the second logic input [7]. In the latter case the input signal linked to the program gate of the *pull-up* transistor needs to be inversed. We have recently showed that a NAND circuit built from four RFET devices can be electrically reconfigured to provide a NOR function by simply switching the program gate V_{PG} signals and supply voltage between GND and V_{dd} [19].

Figure 5a shows the circuit implementation and 5b the respective complementary NAND and NOR response of the circuit. Nevertheless, this multifunctional circuit requires
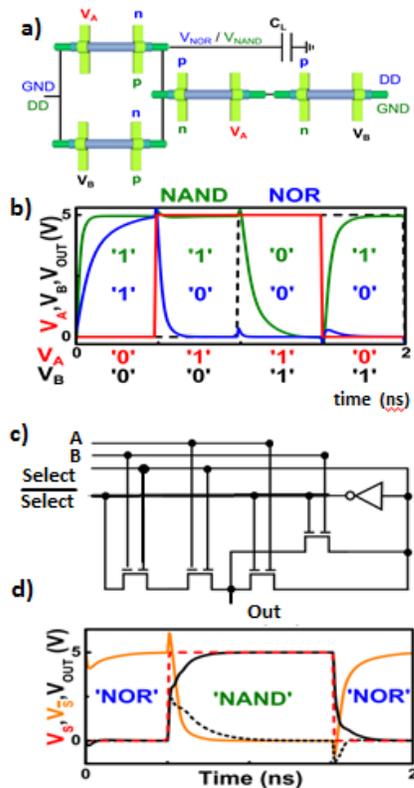
Figure 5. a) Reconfigurable NAND / NOR complementary circuit block . b) Simulations of circuit in a) with freely selectable NOR and NAND function. c) Compact six-transistor NAND/NOR cell with integrated select signal and supply voltage switch. Implementation in a pass logic-type approach, where the inverter basically acts as a de-multiplexer. d) Dynamic change of logic state as programmed by the select signal. Output responds within less than 1 ns and reaches full values despite the pass logic implementation.

switching of the supply voltage V_{DD} with GND. An elegant solution is provided by connecting an inverter as implemented in Fig. 4b at the select input. The inverter fulfills two functions, it converts the program gate voltages as needed and in addition it flips the supply voltages. The implementation resembles a pass type of logic, where supply and data paths are not separated from each-other. Figure 5d shows the mixed mode simulation results when converting the circuit from a NAND to a NOR function [19]. Importantly, it can be observed that the full output swing is reached since only a single inverter stage is used to translate a data path into a supply voltage path. This is because only one RFET on-resistance in the corresponding pull-up or pull-down network builds a voltage divider to the supply or ground voltage. With this realization a reconfigurable NAND / NOR circuit can be implemented with only 6 transistors. In contrast, an application with the same functionality as realized in conventional CMOS electronics would require 8 FETs for the individual NAND and NOR functions plus a 2 x two-to-one multiplexer to route the output signals, which requires additional FETs. More complex logic gates have been extensively studied by I. O´Connor et al. based

on CNTs [26, 27], and by P.-E. Gaillardon et al. based on Si nanowire devices [28], considering power and area consumption as well as speed.

I.   CONCLUSIONS

An electronic platform based on reconfigurable nanowire FETs has been presented. The working principles of RFETs with programmable n- and p- type polarity have been described. The adjustment of the symmetry of RFETs has been achieved by the application of radial compressive strain. It was shown, that symmetric RFETs enable complementary circuit implementation. Importantly, in the example of a NAND / NOR circuit this paper shows that complete gates can be reconfigured in a simple manner. Reconfigurable FETs have thus reached a maturity, to be used as a template to test and design future computing systems with low-power consumption making use of the individual reconfiguration at the device level.

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