Toward Ultralow-Power Computing at Exteme with Silicon Carbide (SiC) Nanoelectromechanical Logic

(*Invited Paper*)

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***Abstract*—Growing number of important application areas, including automotive and industrial applications as well as space, avionics, combustion engine, intelligent propulsion systems, and geo-thermal exploration require electronics that can work reliable at extreme conditions – in particular at a temperature > 250°C and at high radiation (1-30 Mrad), where conventional electronics fail to work reliably. Traditionally, existing wide-band-gap semiconductors, *e.g.*, silicon carbide (SiC) transistor-based electronics have been considered most viable for high temperature and high radiation applications. However, the large-size, high threshold voltage, low switching speed and high leakage current make logic design with these devices unattractive. Additionally, the leakage current markedly increases at high temperature (in the range of 10 µA for a 2-input NAND gate), which induces self-heating effect and makes power delivery at high temperature very challenging. To address these issues, in this paper we present a computing platform for low-power reliable operation at extreme environment using SiC electromechanical switches. We show that a device-circuit-architecture co-design approach can provide reliable long-term operation with virtually zero leakage power.**

Keywords—switches; nanoelectromechanical logic; computing; nanoelectromechanical systems (NEMS); silicon carbide (SiC)

I. INTRODUCTION

Rising energy costs have driven the demand for high performance, energy efficient industrial systems with reduced cost of ownership. Development of such systems has been facilitated by the availability of highly sophisticated microsystems comprising of sensors and electronics for diagnostics and control. In such applications, microsystems are required to operate in a high-temperature (T> 300°C) and extreme ambient conditions. Fig. 1a illustrates select example applications. In aerospace systems, the requirements for improved performance including fuel efficiency, reliability and operating costs has necessitated the development of a new generation of more electric aircraft (MEA) [1]. With respect to gas turbines in aircraft and space vehicle propellers, enhanced performance requirements combined with noise and emission regulations have necessitated investigation of enhanced high bandwidth engine control technologies. The electronics monitoring temperature and pressure in these applications need to be co-located very close to the combustion chamber operating at ~2000°F (1100°C) for accurate measurements. Another application of high temperature electronics (HTE) and sensors is the monitoring of conventional as well as enhanced geothermal systems (EGS) for power generation. In EGS, high pressure fluid is pumped into the well to enhance existing fractures in the rock thus creating an artificial reservoir similar to a natural hydrothermal resource [2]. The fluid, super-heated by the heat in the rock, is pumped to the surface where it is used to power turbines and generate electricity. Si-based sensors and electronics, despite being operated inside a heat shield, do not lend themselves to long term operation because of thermal budget considerations. More importantly, local electronics make it inherently easier for remote monitoring of vital parameters in healthcare and mechanical status (e.g., break wear) in automobile sector. The higher numbers of electrical/electronic components however, require novel liquid- or two-phase cooling system strategies [3]. HTEs capable of reliable, low-power operation at elevated ambient temperatures would greatly alleviate the complexities associated with cooling, weight and fuel efficiency.

Clearly there is an emerging demand for computation at high temperatures driven largely by the desire for optimal energy utilization. But HTE can also alleviate the need for expensive thermal management and heat sinking requirements of conventional CMOS electronics where increasing density has led to increasing junction temperatures. The present advancements in CMOS electronics have been able to reach operating temperatures of about 250°C [4], but this is not sufficient for the applications that we have discussed about so far. In order to attain reliable operation at high temperatures with minimum off-state leakage, we have designed and verified a silicon carbide (SiC) 3-terminal (3-T) device capable of operations above 500°C, based on SiC nanoelectromechanical systems (NEMS). SiC was chosen as the structural material for the device due to its stability and durability at harsh and extreme conditions. This aspect of the material for our purpose will be discussed in the following section. Furthermore, our NEMS 3-T unit has shown observable switching at >500°C, with minimal leakage in the range of ~10–100 pA.

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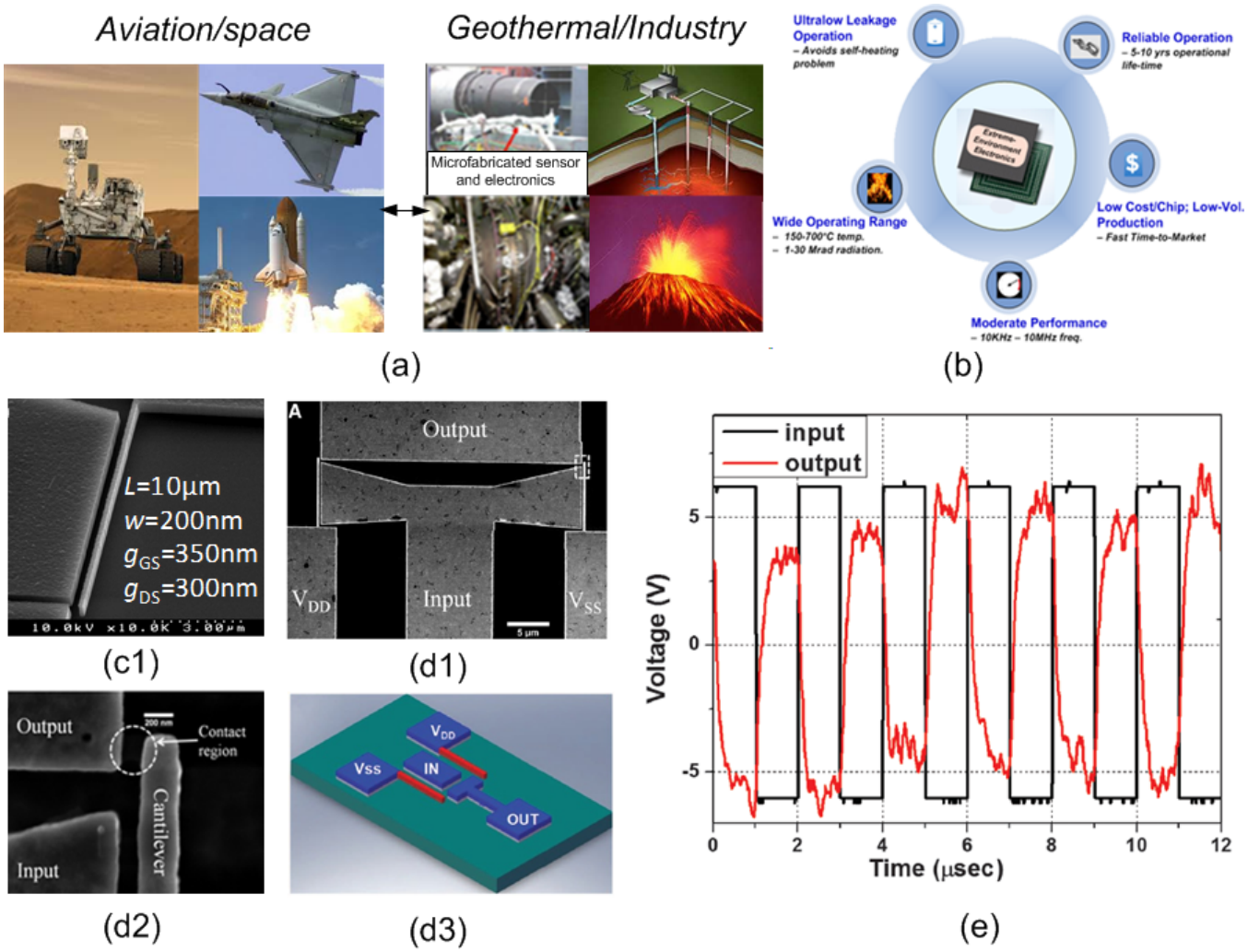


Fig. 1. Synopsis overview of SiC nanoelectromechanical logic applications and device technologies. (a) Market drivers for high temperature technology. (b) Key criteria for working at extreme conditions. (c1) Fabricated 3-T poly-SiC switch and its close-up view, scanning electron microscopy (SEM) images of the poly-SiC NEMS inverter. (d1) Top view, and (d2) Close-up view of SEM images. (d3) Schematic representation of an SiC NEMS inverter. (e) Measured input/output waveform at 500°C.

II. Choice of Material and Device

Figure1b illustrates the requirements for high temperature and extreme environment electronics. The key requirement is durability, *i.e.*, the ability not only of the electronics but also that of the contacts, interconnects and packaging to operate at elevated temperatures for thousands of hours. In the majority of the envisioned applications, moderate clock frequencies (up to 10 MHz) and higher cost/chip compared to conventional Si electronics would be acceptable. The existing Si CMOS technology has so far shown promising results with regard to performance and scaling. Despite the high performance, excessive gate leakage on scaling and p-n junction and thermionic leakage at elevated temperatures limits the operation of conventional Si metal-oxide-semiconductor field-effect transistor (MOSFET) technology to below 300°C, even when implemented with the silicon-on-insulator (SOI) approach. In addition, carrier mobility and velocity saturation also degrade with temperature. Wide bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), have much lower intrinsic carrier concentrations than Si and thus are not affected by intrinsic carrier conductivity issues or leakage currents until beyond 600°C. In particular, SiC (bandgap ~3eV) possesses excellent physical and electrical properties, including high thermal conductivity (5 W/cm°C), high elastic modulus (~400 GPa), chemical stability, high electric field breakdown (4×10^6 V/cm), and relatively high electron saturation velocity (9.7×10^7 cm/s) [5]. The material is also available in bulk wafer form. SiC technology is thus a good candidate for implementing integrated circuits for operation in high temperature. To further eliminate the issue of off-state leakage which is very common in electrical switches, we replace these switching elements in circuit with SiC cantilever-based, mechanically actuating switches. Apart from robustness at high temperature, such a mechanical switch ensures that there is no contact between the source and the drain when the switch is off. This technology is also accompanied by an overall reduction in the area and power, which will be discussed in the following sections.

III. Device Level Exploration

A. SiC NEMS 3-Terminal Switch

An image of a 3-terminal (3-T) NEMS switch, with corresponding gate (G), source (S) and drain (D) terminals, is shown in Fig. 1c. This switch is electrostatically actuated laterally (in-plane) and is realized from doped polycrystalline silicon carbide (poly-SiC). Key design considerations include appropriate choice of dimensions together with doping levels of the JFET for achieving compatible threshold voltage as well as device scaling. This phenomenon depends on several forces and factors which can be modulated to adapt it for our purpose. The main forces acting on a cantilever beam are electrostatic force (F_e) which is a result of the actuation voltage applied at the gate, mechanical restoring force (F_m), and the van der Waal's force between two surfaces in contact, which depends on the material and contact situations. Initially when actuation voltage (V_{on}) is applied at gate G1 to write the value, when $F_e > F_m$, the cantilever beam bends to touch the drain surface. On one hand, V_{on} can be determined as given in [6] using the spring-mass approximate model on the cantilever beam, $V_{on} = (8kg^3/27\varepsilon_0 wt)^{1/2}$, where k is spring constant, ε_0 is vacuum permittivity, g is actuation gap, w the gate coupling length and t the beam thickness. We can notice the clear cubic relation between actuation gap and the pull in voltage. In order to achieve smaller Von we must maintain a small g. On the other hand, the switching time may be given as,

$$t_s \approx \sqrt{27/2}\,(V_{on}/\omega_0 V_{act}) \propto (L^2/w)(V_{on}/V_{act})\sqrt{\rho/E_Y} \qquad (1)$$

where, ω_0 is the stiffness of the beam, V_{act} is the applied actuation voltage and ρ is the density of SiC. This shows that there exists a clear trade-off between threshold voltage and operating frequency of the NEMS switch. However, by moving to nanoscale dimensions and leveraging novel beam/switch structures, it is possible to realize switches with low turn-on voltages (≤ 3V) and fast switching times (≤ 1µs or well in the <100ns regime). For an 8 µm long, 150 nm wide switch with a 120 nm gap, the operating voltage was measured to be ~4.70 V. Reliable operation was demonstrated for 21+ billion cycles at 25°C and 2+ billion cycles at 500°C [7].

B. Analysis of Device Properties

In the 3-T switch design, the electrostatic force will pull the beam towards the drain irrespective of the polarity of the voltage difference between gate and the source. Thus the design can be used as a pull-up (PMOS) or pull-down (NMOS) switch by connecting the source terminal to V_{DD} or V_{SS}. Fig.1d shows the SEM image of a fabricated inverter and Fig. 1d presents a schematic of the design (Fig. 1d2 enlarged on inverter right switch). In [8] we reported successful operation of an inverter at 500°C in air with V_{DD}=6V and V_{SS} = –6V, at an operating speed of 500 kHz. The design and fabrication process mirror that of the 3-T switch. A complementary logic style is implemented to reduce noise sensitivity and enable low static-power consumption. The two beams are dimensionally identical with length, width and actuation gap corresponding to 8 µm, 200 nm and 150 nm, respectively. The logic level (Fig. 1e) is higher than that in existing Si logic devices, which operate at 3V or lower. However, the threshold voltage of the fabricated switches is compatible to other competing high-temperature electronics [9]. The active area of the demonstrated inverter is ~8 µm^2, about three orders of

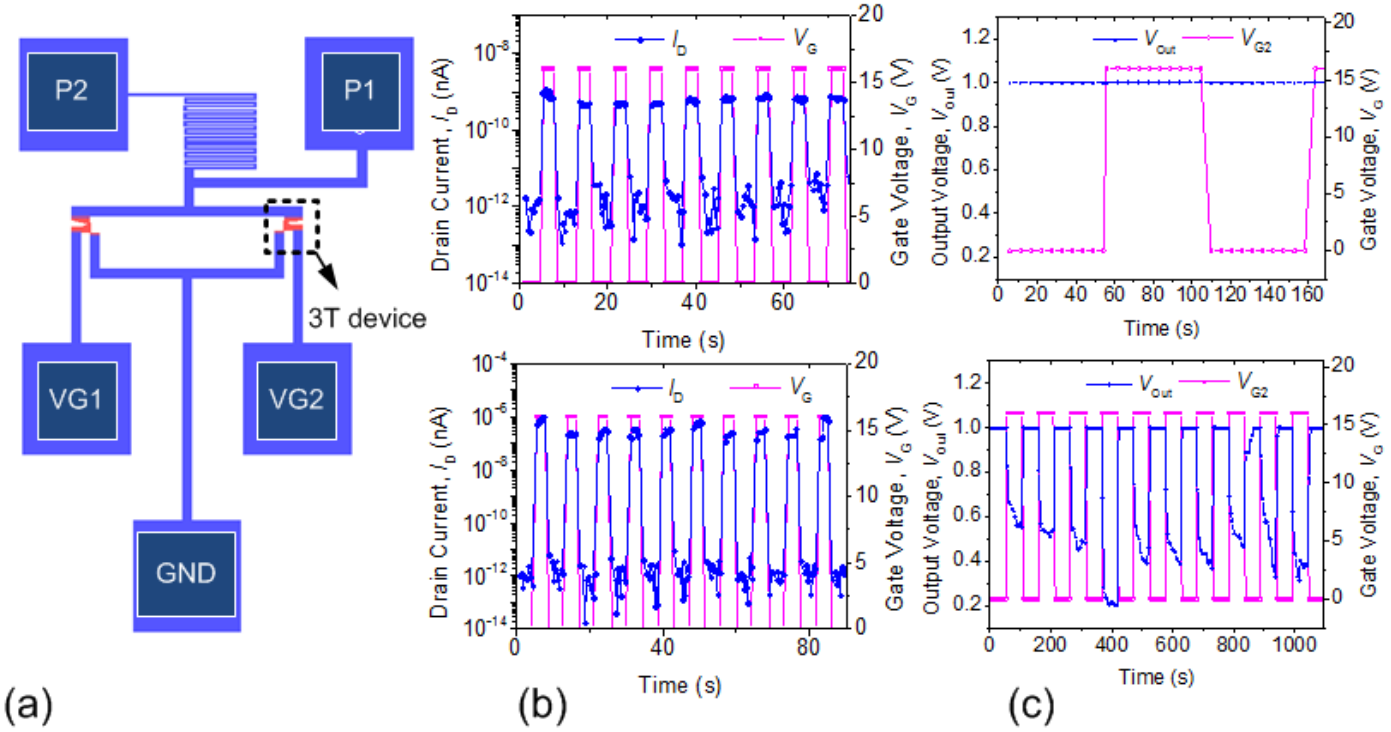


Fig. 2 Synopsis overview of SiC nanoelectromechanical logic applications and device technologies. (a) Market drivers for high temperature technology. (b) Key criteria for working at extreme conditions. (c1) Fabricated 3-T poly-SiC switch and its close-up view, scanning electron microscopy (SEM) images of the poly-SiC NEMS inverter. (d1) Top view, and (d2) Close-up view of SEM images. (d3) Schematic representation of an SiC NEMS inverter. (e) Measured input/output waveform at 500°C.

magnitude smaller than most reported high–temperature, JFET-based logic gates, which have gate lengths ranging from tens to few hundreds of microns. The measured leakage current in the off state is less than 1pA.

Using the switch unit to design a complex gate structure as shown in Fig. 2a, we have also successfully demonstrated clearly distinguishable 2-input OR and NOR operation for different input combinations. In order to implement the OR gate logic, we bias P1 terminal with V_{DD}, P2 remains unconnected and the Drain current is measured while forcing G2 to 0V and giving a pulse of 0V and 5V to G2, and vice-versa. For operation as NOR gate, we bias P2 with V_{DD} which is applied through the resistance coil, and we measure the output voltage through P1 while respectively pulsing G1or G2 as described in the OR operation. The results observed for quasi-DC testing of OR and NOR logic are depicted in the plots of Fig. 2b and Fig. 2c respectively. The NOR operation is similar to a pseudo-MOS structure, where the pull up resistance is modeled as a coiled structure in the device. Such a structure results in an effective reduction of the number of active elements (actuating beams) from 4 (conventional CMOS) to 2, and a notable reduction in die area due to the small size of the device.

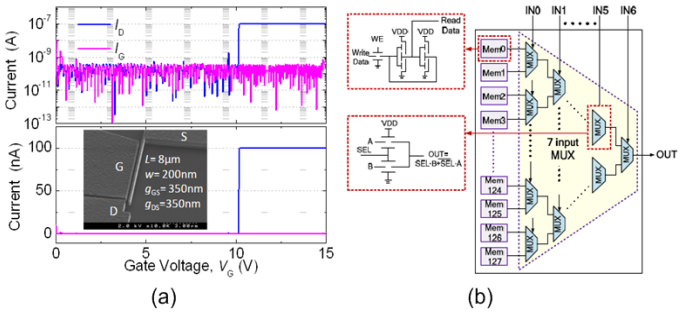


Fig. 3 (a) Measured switching characteristics of a SiC NEMS switch at high temperature (T ≈500°C) with Von≈10.2V and Ion > 100nA, and minimal gate and off-state drain leakage current. Currents plotted in (top) logarithmic and (bottom) linear scale, respectively. Inset is device SEM image, (b) 7-input LUT with NEMS based memory and the MUX tree.

C. High Temperature Operation of NEMS Switch

SiC offers compelling mechanical, thermal and chemical properties and hence a great potential for the SiC NEMS switches to work at high temperature and harsh environment. In this section we report experimental efforts on high-temperature measurements of the switch performance.

The NEMS switches are wire bonded to a ceramic package, and the high-temperature measurement setup features an infrared (IR) heater with spot size of 1cm^2, which is sufficient for heating the devices under test locally without overheating the surrounding cables. The temperature of the spot was carefully calibrated to 500°C and focused on the die of interest. We connected source terminal of the 3-T device to ground and applied a constant bias voltage to the terminal, and then swept the voltage on gate from 0V to the actuation voltage and then back to 0V, while constantly monitoring the current between drain and source and gate and source. Fig. 3a shows the measured data [10] from an 8µm-long, 200nm-wide device clearly switching at T≈500°C, in ambient air. The switch-on voltage V_{on} is about 10.2V and on-state current $I_{D,On}$ is larger than 100nA, which is comparable to those at T≈25°C. The off-state drain current $I_{D,Off}$ and gate leakage I_G are on the order of ~10^{-11}A to ~10^{-10}A. We have also demonstrated switching at high temperature from switches with multi-gated structures. To study the robust long-cycle operations in many devices in ambient air and at high temperature, we have measured their complete long-cycle evolutions, with time-domain on-current variations and other details recorded for every single cycle [10-13]. The operation of NEMS switches with tolerable off-state leakage makes it a viable element for making complex circuits, multiplexer chains, oscillators and memory.

IV. Circuit and System Level Exploration

A. Reconfigurable Computing Fabric for Extreme

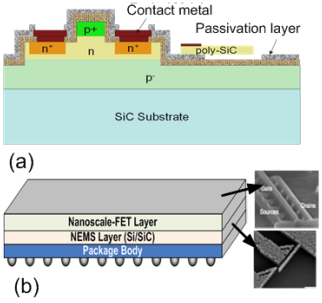
Due to the increasing demand of electronics that are capable of reliable operation at high ambient temperature (>500°C), a HT reconfigurable computing platform holds great potential. SiC NEMS switches make such a platform realizable due to its low-voltage and extremely low leakage HT operation. Previously, our group has evaluated the efficiency of an all-mechanical FPGA which is aimed to work at extreme industrial temperatures. The target here is the Configurable Logic Blocks (CLBs). Each CLB contains a 7-input lookup table (LUT), a D flip-flop as the sequential element, and a MUX, which selects between the combinational and sequential outputs. The design of a 7-input LUT with NEMS implementation is given in Fig.3b. From [14] we can see that this all-mechanical FPGA configuration has characteristic low power consumption, high performance and small area as compared to alternative implementations of several benchmark circuits. The lumped electrical models used for evaluation were obtained using measured parameters from a number of the fabricated SiC NEMS 3T switches. Simulations using this model showed that, the entire FPGA suffered from several nA (~90nA) of leakage current, which is much lower than the average mA leakage current observed in conventional CMOS FPGAs. Although their power, delay and area were inferior to that of custom ASICs, they provide an advantage of low-cost, low-volume production for targeted applications in industry.

B. SiC NEMS-JFET Integration

The most viable SiC integrated circuit (IC) device technology is currently the JFET, since Si CMOS devices face limitations due to gate leakage at nanoscale dimensions. Our team of researchers from NASA has successfully demonstrated SiC-based sensors and JFET electronics at temperatures beyond 550°C [15]. However, several issues make realization of robust digital logic circuits based on SiC JFET challenging. These include large transistor size, high threshold voltage and low switching speed. Leakage current also increases significantly at elevated temperatures. Finally, multi-level cascaded logic realization using depletion-mode negative threshold devices poses a major challenge.

NEMS switches offer an attractive alternative to realizing low-power, high-performance logic circuits. The on-off transitions of these switches can be controlled by electrostatic

actuation and the physical air/vacuum gap results in minimal off-state leakage. Thus extremely high I_{ON}/I_{OFF} ratio can be achieved even at elevated temperatures. In addition, the devices possess the operating speed, power and footprint comparable to conventional MOSFET. NEMS switches however, do not naturally provide the typical voltage/current gain observed in transistors. This affects drivability and hence realization of cascaded logic circuits. Hybrid integration of SiC NEMS with SiC JFET-based circuits is a potential solution to this. This appears feasible given that the SiC NEMS logic technology is naturally compatible with the SiC JFET-based integrated circuit technology. Such a platform has the potential to provide new opportunities for high temperature mixed-signal electronics, where the low-leakage NEMS device nearly complements the operation of the high speed JFET devices. Mainly, it addresses the high leakage power issue in JFET devices at high temperatures. Fig.4a and 4b illustrate the section view of parallel integration and stacked layer integration of NEMS and JFET.



	SiC NEMS	SiC JFET
Advantages	1. Near-zero leakage 2. Possible ultralow threshold voltage.*1 3. Robust HT operation 4. Custom structure design*2	1. High performance 2. High driving strength 3. HT compatible material
Limitations	1. Lower performance (mechanical active element) 2. Absence of gain -> limited driving strength 3. Lower switch life-time	1. High threshold voltage 2. Low speed 3. Increasing leakage at higher *Ts* 4. Less flexible for custom design

*1. Low threshold->low switching power
*2. Multiple gate and drain configuration

(c)

Fig. 4 (a) Cross-section schematic showing parallel integration of SiC NEMS-JFET on a single substrate, (b) Schematic depicting the heterogeneous stack integration of the two layers, (c) Comparison of the two complementary switching schemes in terms of major circuit parameters.

The several advantages of these fundamentally dissimilar computing layers (JFET and NEMS integration) that complement each other are given in the table in Fig. 4c. It also highlights that the NEMS device is amenable for custom design of the switch structure, by which only one such a switch can be used to demonstrate a complex gate, and each of the switches can be developed with multiple/split gates for better pull in characteristics and multiple drains for different logic values. We have so far developed multi-gate and multi drain switches for independent gate control and multi-level logic respectively. Another potential design that we have proposed is the multilayer beam structure for implementing complex structures, which is discussed in the following section.

V. Design for Reliable Ultralow Operations

A. Multilayer Swtich and Device Structure Optimization

When implementing more complex circuits like an ALU, minimization of the number of active elements, is preferable for improvements in performance and robustness as well as reduction in device area. Unlike conventional MOSFET electronic switches, NEMS switches offer unique customizability of switch structure to realize complex functions with few active elements [16,17]. Fig. 5a and Fig. 5b show conceptual drawings of a 4-T and 7-T switch respectively, using multilayer beams with separate control and S/D terminals [16]. These multilayer switches enable efficient implementation of the MUX-trees and memory elements using the NEMS switch as a basic building block. With respect to Fig. 5a, the cantilever is made of insulating poly-SiC or silicon nitride. The two conducting segments on the sidewall of the beam are made of doped SiC and electrically isolated from each other. When the voltage between G and B, $V_{GB} \geq V_{on}$, the beam moves towards G and forms a connection between S and D. By connecting B to V_{SS} or V_{DD}, we get a PMOS or NMOS pass transistor-like cell. The 7-T switch operation is similar to that of the 4-T switch. The availability of two sets of connection for this switch, however, makes it behave like a 2×1 MUX. Since in digital logic, the G voltage can only be logic low or high, the cantilever gets pulled in towards one side only. The corresponding S value will get transmitted to D, which realizes the function of a MUX.

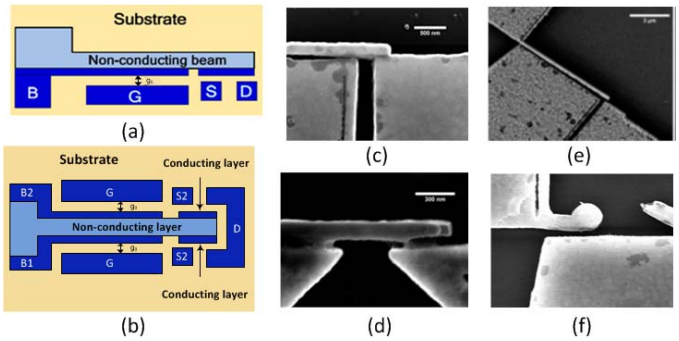


Fig. 5 Designs of multiple-terminal NEMS switches for logic. (a) 4-T multi-layer beam switch, and (b) 7-T multi-layer switch, for efficient implementation of 2x1 multiplexer. Typical switch failure mechanisms observed in our experiments, (c) Stiction with beam touching drain and gate, (d) Incomplete delineation of beam during lithography/etching, (e) Effects of stress in device layer, and (f) cantilever fracture during fabrication or release.

B. Failure Modes and Reliability Improvement Options

Failure mechanisms we have so far observed include the following: (1) Stiction, with the beam touching drain and/or gate (Fig. 5c); (2) Incomplete pattern delineation at the e-beam lithography process step or due to material re-deposition in the actuation gap during etching of the device layer, a result of aggressive feature scaling (Fig. 5d); (3) Cantilever deflection caused by localized stress leading to higher than designed actuation voltages or no actuation at all (Fig. 5e); and (4) Mechanical fracture near the anchor of the beam (Fig. 5f).

Process-based approaches to mitigating these issues include: (1) optimizing process conditions of the film deposition step for appropriate stress and stress gradient, (2) polishing the poly-SiC film for improved feature resolution during patterning and etching, (3) optimization of the electron-beam lithography step to reduce trade-off between resolution and edge roughness and (4) optimization of the etch process to reduce etch lag and re-deposition.

Design-based approaches include varying beam cross-section near the base or a curved beam design. The drain contact may also be positioned closer to the beam than the gate. Other options include tapering the gate electrode at the end closer to drain electrode or replacing the cantilever design

with a doubly-clamped beam and repositioning of the gate and drain to avoid simultaneous contact while also reducing actuation voltage.

C. Swtich Conductance Improvement

In the SiC NEMS devices we have fabricated and tested, the contact resistances are often in the MΩ ranges. The contact resistances of the switches are generally dominated at low actuation voltages by the native oxide formed on the switch contacting surfaces. At higher applied voltages, the calculated contact resistance values using Sharvin's model fit the measured values well [2]. To improve its conductivity, graphitized SiC surface is an attractive solution since the electrical conductivity of the resultant graphite/graphene surface is exceptional. The requisite processing does not alter the key dimensions of the device given that only a few atomic layers of materials are affected. However, conducting the experiment under UHV and at a temperature >1200°C requires an expensive vacuum chamber, pumping system, and heating tool. We have attempted an alternative approach – graphitize the SiC surface by using laser energy. We have gathered some interesting and encouraging preliminary results based on this attempt [2]. We believe this could possibly lead to a highly innovative approach toward new generations of high-performance SiC NEMS switches.

The graphitization process involves XeCl laser treatment of the SiC surface, to convert the SiC surface into a carbon-rich, more conductive layer. Subsequent TEM and XPS studies indicate that a few to ~10nm-thick nanographite structure has been obtained, repeatedly, from such a process. The measured resistivity of such surface layers is as low as 0.004 Ω·cm.

VI. Summary and Future Work

In this paper we have described a computing at extreme paradigm using SiC nanomechanical switches. We have followed a co-design paradigm that combines device level design space exploration with circuit-system level analysis and vice versa. We have demonstrated the operation of our SiC based 3-T switch structure in room temperature and the measured values for HT operation are also presented. Owing to its robust characteristics at high temperature, SiC was chosen as the substrate material for building our device. The unique adaptability of the NEMS structure is observed from the ability of a single fabricated device structure to operate as OR and NOR logic. The corresponding results have also been reported in this paper. We have also presented a comparison of conventional CMOS logic-based FPGA with an all-mechanical NEMS reconfigurable platform. The results have shown that NEMS FPGA provides better performance, robustness and low off-state leakage during HT operation. We have proposed a novel idea of integrating JFET and NEMS for developing a hybrid computing framework, where the two different elements complement the drawbacks of each other. Our design of a multilayer switch structure for implementing complex logic such as MUX and ALU in the design of a reconfigurable platform was also discussed. In the final sections we have enlisted the design challenges encountered in these nanoscale structures, observations made from testing numerous switches, and the methods for overcoming the challenges.

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