Complementary Resistive Switch Based Stateful Logic Operations Using Material Implication

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***Abstract*—Memristor based logic and memories are increasingly becoming one of the fundamental building blocks for future system design. Hence, it is important to explore various methodologies for implementing these blocks. In this paper, we present a novel Complementary Resistive Switching (CRS) based stateful logic operations using material implication. The proposed solution benefits from exponential reduction in sneak path current in crossbar implemented logic. We validated the effectiveness of our solution through SPICE simulations on a number of logic circuits. It has been shown that only 4 steps are required for implementing N input NAND gate whereas memristor based stateful logic needs N+1 steps.**

I. Introduction

Implication based stateful logic using memristors has recently been proposed as a design paradigm that allows to implement any boolean logic using memristors. Further, memristor based resistive-variable memory devices have recently emerged as a promising technology to overcome the limitations of traditional CMOS based memories [1] [2] [3]. These devices can be fabricated with finer layouts using non-lithographic methods like imprint lithography to produce high density memory with short access latencies. Moreover, they exhibit non-volatile state retention characteristics, which are particularly suitable for stable data storage. Hence, memristor based efficient memory design and implementation is currently of high interest both in academia and industry. Memristive devices can also be programmed for several different resistance states that features a multilevel RRAM [4].

Over the years various memristor array based memory architectures have been reported. For example, passive crossbar arrays of memristive elements were reported as possible non-volatile random access memories (RAMs) in [5]. However, passive crossbar arrays have the general issue with sneak-path currents due to interference from the neighbouring cells when selecting a designated cell within the arrays. To avoid sneak-path currents, recently complementary resistive switches (CRS) were proposed [2], which consist of two anti-serial memristive elements. These elements, including a high resistance state and a low resistance state, are used to encode either logic 0, 1, ON or OFF (See Fig 1). The transitions between these states depend on the applied biasing voltage across the CRS, controlled by SET and RESET threshold voltages [2].

Stateful logic operation based on material implication (IMP) was first proposed by HP Laboratories [7]. The basic structure of the material implication proposed by HP Laboratories is discussed in the next section. There are many proposals that can intrinsically enable logic in memory architectures, for which the non-volatile memory elements are used as the main devices for logic computations [7], In [6] authors proposed a circuit structure that performed logic operation on memristor memory based on nanocrossbar. Here the authors assumed basic memristor module, however in such a large array sneak path could be a problem.

In this paper we propose a CRS based stateful logic operations using material implication. To the best of our knowledge, no prior work exists implementing CRS based stateful implication logic. The proposed solution benefits from exponential reduction in sneak path current in crossbar implemented logic. Further, it has been shown that only 4 steps are required for implementing N input NAND gate whereas memristor based stateful logic needs N+1 steps. The rest of the paper is organized as follows. Section II introduces preliminary concepts related to this paper, Section III describes the proposed CRS stateful logic and NAND operation. Experimental results and crossbar sneak path analysis are presented in Section IV. Finally, Section V concludes this paper.

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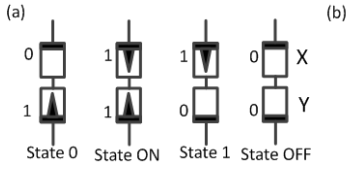


(b)

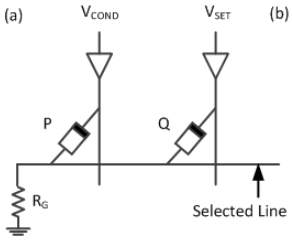
CRS State	State of Memristors X	State of Memristors Y	Resistance
0	0	1	R_{CRS}
1	1	0	R_{CRS}
ON	1	1	R_{CRSON}
OFF	0	0	R_{CRSOFF}

Fig. 1. (a)Four states of CRS. (b)Functional chacteristics of CRS

II. Background and Motivation

A. Memristor IMP Operation

Memristor is a two terminal device which has two states, 1 for low resistance state (R_{ON}) and 0 for high resistance state (R_{OFF}) [1], [7]. The transitions between these states depend on the applied biasing voltage across the memristor, controlled by SET and RESET threshold voltages. In [7], it is shown that memristor can be used for stateful logic operation. The memristor IMP operation is shown in Fig. 2. As Fig. 2(a) shown, two memristors are connected with a nanowire (the selected line). One terminal of those memristors will be connected together with a load resistor R_G. Voltages V_{COND} will be applied across P memristor and V_{SET} will be applied to Q memristor. After that, the state of Q memristor is the IMP operation result. The truth table for memristor IMP operation is shown in Fig. 2(b). To perform the IMP operation, the following Eqn. $R_{ON} < R_G < R_{OFF}$ needs to be satisfied [7]. V_{SET} is the positive voltage which can shift memristor to state 1. V_{COND} is the positive voltage less than V_{SET}, thus cannot change the state of memristor. When P memristor is in high resistance state 0, most of V_{COND} is dropped across P memristor. Therefore voltage across Q memristor is equal to V_{SET}, the state of memristor Q changes or stays on state 1. On the other hand, if memristor P is in state 1, the voltage on selected line is equal to V_{COND}, the voltage across memristor Q is not enough to switch, it will remain its state 0.



(b) $Q' = \overline{P} + Q$

P	Q	Q′
0	0	1
0	1	1
1	0	0
1	1	1

Fig. 2. (a)IMP operation of memristor cell. (b)Truth table of IMP

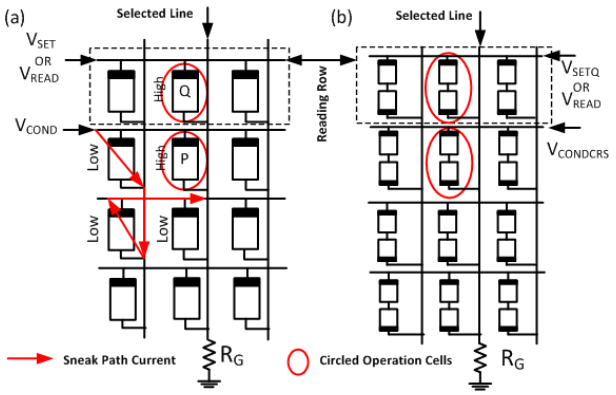


Fig. 3. (a)Memristor based crossbar logic circuit. (b)CRS based crossbar logic circuit

B. Memristor Memory Logic

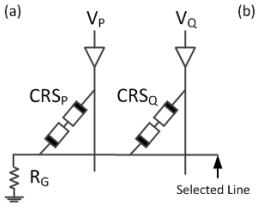
Fig. 3(a) shows a stateful logic mapped to crossbar structure, voltage V_{SET} and V_{COND} should be applied to the memristor P and Q in logic operation stage. Logic will be performed between those two memristors and output will be stored in memristor Q. R_G is used as a pull-down resistor in logic operation stage. To read the output result in crossbar structure, a read scheme [8] is proposed. A voltage V_{READ} is applied to the reading row, R_G in read stage will act as a load resistor, voltage on R_G will be sensed and compared with V_{REF}. One of problems in this scheme is sneak path current that exists during the stateful logic operation. In Fig. 3(a), the red line with arrow shows the sneak path current. This sneak current can pass the non-operational memristors and inject the current to the selected line pulling up the voltage and this could corrupt the output results. For example, if the two red circled operation cells are in high resistance state. Apply V_{SET} to Q memristor can switch it to 1 (low resistance state). However, due to sneak path current, the voltage in selected line will be pulled up, so the voltage for Q memristor will be much less than V_{SET}. As a result, memristor Q remains in its state, and an error is induced. To address this issue, a design using CRS is presented in [2] to reduce the sneak path current.

III. CRS Stateful Logic

A. CRS IMP Operation

As explained in Section I, CRS has four different states as shown in Fig. 1. Note that state 0 and state 1 have the same resistance state (R_{CRS}) as one of memristors X and Y is in R_{OFF} and the other is in R_{ON} state. When both of those memristors are in R_{ON} states, the CRS is in state ON (the lowest resistance). When both of them are in R_{OFF} state, CRS is in OFF state and this state is not used in stateful logic.

To perform CRS IMP operation, consider the Fig. 4. Fig. 4(a) shows the basic structure. This structure contains two CRS cells CRS_P and CRS_Q, result will be latched in CRS_Q. By applying voltage V_P, V_Q to CRS_P and CRS_Q respectively, the circuit can perform IMP operation $CRS_Q''' \leftarrow CRS_P$ *IMP* CRS_Q. Fig. 4(b) shows the truth table of CRS IMP. Three states $1, ON, 0$ are used in CRS IMP. Fig. 4(c) shows the number of steps to perform the CRS IMP operations and applied voltages for each step. During IMP operation, $V_{ONCRS-1}$, $V_{CONDCRS-1}$ and V_{CLEARP} (these are defined in Fig 5) are applied to CRS_P, and V_{SETQ} is applied to CRS_Q. In memristor stateful logic, if the applied voltage is not sufficient to switch the state to its opposite state, memristor will remain in its current state. However in CRS IMP operation, the state of CRS may be changed to state ON. During stateful logic operation,



(b)

		Step-1		Step-2		Step-3	
CRS_P	CRS_Q	CRS_P'	CRS_Q'	CRS_P''	CRS_Q''	CRS_P'''	CRS_Q'''
0	0	0	0	0	1	0	1
0	1	0	1	0	1	0	1
1	0	ON	0	ON	0	0	0
1	1	ON	1	ON	1	0	1

(c)

	V_P	V_Q	Function
Step-1	$V_{ONCRS-1}$		Operation
Step-2	$V_{CONDCRS-1}$	V_{SETQ}	Operation
Step-3	V_{CLEARP}		Reset

Fig. 4. (a)Basic CRS IMP operation. (b)Truth table of CRS IMP (c)Apply voltages and steps for IMP operation.

CRS may be either state 0, 1 or ON are shown in Fig. 4(b). To mitigate this problem, we use one step $Step-1$ (Fig. 4(b)) to switch CRS to state ON first, thereby achieving IMP operation similar to memristor IMP. To achieve CRS IMP operation, two types of CRS cells (CRS_P and CRS_Q) are required. Their I-V characteristics are shown in Fig. 5 and note that, CRS threshold voltage V_{Pth1} is larger than V_{Qth1}, and V_{Pth3} is less than V_{Qth3}. It is important to note that when a positive voltage is applied to CRS_Q which is greater than V_{Qth1}, less than V_{Qth2}, CRS_Q will change the cell from state 0 to state ON or remain in state 1. If the applied voltage is greater than V_{Qth2}, the CRS cell will be switched to state 1 irrespective of its original state. For negative voltage, when applied voltage decreases from V_{Qth3} to V_{Qth4}, assuming the initial state is state 1, the CRS cell will be turned to state ON then state 0. The similar behavior is assumed for CRS_P when corresponding voltages are applied. V_{SETQ} will turn CRS_Q from state 0 to 1, it can be equal to V_{Qth2}. Voltage $V_{CONDCRS-1}$ is a key requirement for CRS IMP operation, it should be less than V_{Pth1}, so that CRS_P will be stable under $V_{CONDCRS-1}$. Meanwhile if voltage for CRS_Q is equal to $V_{SETQ} - V_{CONDCRS-1}$, to make CRS_Q stable, this voltage should be smaller than V_{Qth1}. Voltage $V_{ONCRS-1}$ is applied to switch CRS_P from state 1 to ON. V_{CLEARP} can shift CRS_P to state 0. The relationships between various threshold voltages and operation voltages are given in Eqns. (1) to (6) and also shown in Fig. 5. For successful CRS IMP operation, the value of R_G

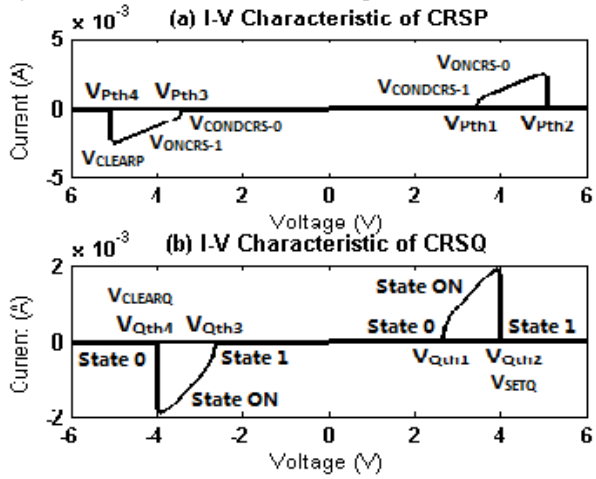


Fig. 5. (a)I-V Characteristic of CRS_P. (b)I-V Characteristic of CRS_Q

should be carefully selected as per Eqn (7). When CRS_Q shifts from 0 to 1, it comes to state ON first, so if R_G is larger than the resistance value of CRS_Q state ON (R_{CRSONQ}), most of V_{SETQ} will be dropped across R_G and there is not enough voltage to switch

CRS_Q from state ON. Also, if R_G is smaller than CRS_P state ON (R_{CRSONP}), $V_{CONDCRS-1}$ will be blocked by CRS_P and the voltage at the selected line will be low. To solve those issues, select $R_G < R_{CRSONQ}$ and greater than R_{CRSONP}. The variation of R_G will effect the successful CRS IMP operation. Increasing the value of R_{CRSONQ} and decreasing R_{CRSONP} can make the circuit has a high tolerance of the variation. In equation (7), R_{CRS} is the resistance value for state 0 and 1 of one CRS.

$$V_{Pth1} > V_{Qth1}, V_{Pth2} > V_{Qth2} \quad (1)$$

$$V_{Pth3} < V_{Qth4}, V_{Pth4} < V_{Qth4} \quad (2)$$

$$V_{ONCRS-1} < V_{Pth3} \quad (3)$$

$$V_{Qth2} - V_{Qth1} < V_{CONDCRS-1} < V_{Pth1} \quad (4)$$

$$V_{CLEARP} < V_{Pth4} \quad (5)$$

$$V_{SETQ} > V_{Qth2} \quad (6)$$

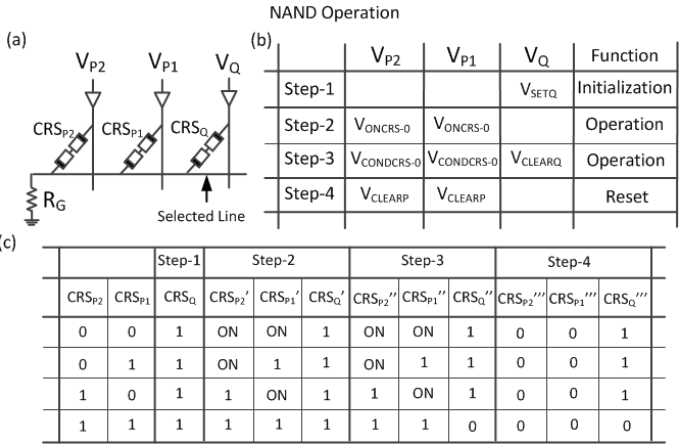
$$R_{CRSONP} < R_G < R_{CRSONQ} << R_{CRS} \quad (7)$$

Fig. 4(c) shows the steps for CRS IMP operation. First, CRS_P and CRS_Q are configured to their initial states. Then in $Step-1$, only voltage $V_{ONCRS-1}$ is applied to CRS_P to shift it to state ON if it is in state 1. The operation in $Step-2$ is like memristor IMP, voltages $V_{CONDCRS-1}$ and V_{SETQ} are applied simultaneously, if CRS_P is in state ON, the voltage on selected line will be pulled to $V_{CONDCRS-1}$, thus for CRS_Q, the voltage dropped across it is less than V_{SETQ} and the CRS cell keeps stable, otherwise, if CRS_P is in state 0, it blocks V_P, voltage across CRS_Q is equal to V_{SETQ}, CRS_Q will be shifted to state 1. After operation steps, CRS_P may come into state ON (low resistance state). So it induces sneak path current into crossbar structure. To address this issue, one extra reset step $Step-3$ is performed after operation steps. In this step, CRS_P will be reset to state 0. The CRS crossbar logic is shown in Fig. 3(b). From this figure, memristors are replaced by CRS cells and CRS_Q are always in the reading row.

B. CRS NAND Operation

According to [7], any logic can be implemented using NAND gates. So the following section will illustrate the details of NAND CRS operations. The two input NAND operation needs three CRS cells, CRS_{P1}, CRS_{P2} (NAND inputs) and CRS_Q which will get the result after NAND operation. To perform NAND operation, CRS_Q is set to state 1 under voltage V_{SETQ} in $Step$-1 (see Fig. 6(b)). In $Step$-2, $V_{ONCRS-0}$ is applied to CRS_{P1} and CRS_{P2} to switch them to state ON if they are in state 0. $Step-3$ is the most important part of NAND operation, voltage $V_{CONDCRS-0}$ and V_{CLEARQ} are applied to all operation CRS cells simultaneously. If both CRS_{P1} and CRS_{P2} are in state 1, CRS_Q will be shifted to stat 0. Otherwise, CRS_Q will stay in state 1, because most of voltage $V_{CONDCRS-0}$ is dropped across R_G and make CRS_G has no enough switch voltage. From Fig. 6(c), it can be seen that if either CRS_{P1} or CRS_{P2} is in state 0, CRS_Q remains in state 1, otherwise it is changed to state 0 which matches the NAND truth table. Finally, one reset step for CRS_{P1} and CRS_{P2} is required (See Fig. 6(c)).

To perform N inputs CRS NAND operation, it only needs four steps, however $N+1$ CRS cells are required. CRS_Q will be initialized to state 1 in $Step-1$, then all N input CRS_P cells will be performed NAND operation simultaneously under voltage $V_{ONCRS-0}$ and result will be latched in CRS_Q. Further, one reset step is followed. For memristor NAND operation, in previous approach, it needs to perform N times IMP, so N inputs memristor NAND logic requires $N+1$ steps (N IMP steps plus one step initialization). The number of steps required for multi input NAND operation is shown in Table I.



		Step-1	Step-2			Step-3			Step-4		
CRS_{P2}	CRS_{P1}	CRS_Q	CRS_{P2}'	CRS_{P1}'	CRS_Q'	CRS_{P2}''	CRS_{P1}''	CRS_Q''	CRS_{P2}'''	CRS_{P1}'''	CRS_Q'''
0	0	1	ON	ON	1	ON	ON	1	0	0	1
0	1	1	ON	1	1	ON	1	1	0	0	1
1	0	1	1	ON	1	1	ON	1	0	0	1
1	1	1	1	1	1	1	1	0	0	0	0

Fig. 6. (a)Basic circuit of NAND operation. (b)Apply voltages and steps for NAND operation. (c)Truth table of NAND operation.

TABLE I
N INPUTS NAND OPERATION USING IMPLY

Steps	Implementation Steps	
	CRS proposed method	Memristor [7] [10]
IMP	3	1
2 inputs NAND	4	3
3 inputs NAND	4	4
4 inputs NAND	4	5
N inputs NAND	4	N+1

IV. Simulation Results and Analysis

A. Simulation Results

The following explains the simulation results performed for various stateful logic in CRS using Cadence-Spectre simulation tool. To perform the CRS stateful logic operation, the parameters of CRS cells and R_G should follow the equations (1)-(7). Here, we choose $R_{CRSONP} = 200\Omega$ for state ON of CRS_P and $R_{CRSONQ} = 2k\Omega$ for state ON of CRS_Q. The value of R_G should between R_{CRSONP} and R_{CRSONQ}. $R_G = 1k\Omega$. Adding R_G will increase the V_{Pth2} and V_{Qth2} [9], we used $5.3V$ for V_{SETQ}, $-5.6V$ for V_{CLEARQ}. According to apply voltages definition in equations (3), (4) and (6), $V_{ONCRS-1}$ is given the value $-5.5V$. $V_{ONCRS-0}$ is $5.5V$. $V_{CONDCRS-1} = 3.6V$, $V_{CONDCRS-0} = -4.2V$. The reset voltage $V_{CLEARP} = -5.7V$.

Fig. 7 shows the CRS IMP and NAND simulation results. Fig. 7(a), (c) are the applied voltages for CRS IMP and NAND operation. In Fig. 7(b), (d), the state of CRS_Q and CRS_P is represented by two memristors called $stateQX$, $statePX$ (the top red memristor) and $stateQY$, $statePY$, (the bottom black dashed memristor) respectively. The x-axes in Fig.7(b), (d) represent the doping length of the memristor in nanometer (nm). When the doping length is $3nm$, memristor is in state 1 and when the doping length is $0nm$, memristor is in state 0 [11]. So if CRS_Q is in state 0, $stateQX$, the top memristor should be $0nm$, the bottom memristor $stateQY$ should be $3nm$ (See Fig. 7(b)). Comparison between Fig. 7, Fig. 4 and Fig. 6 proves that the simulation results are matched with the expected output discussed in Section. III.

B. Sneak Path Analysis

In this section, first we derive sneak path voltage equations for memristor followed by CRS. Here we assume the worst case for the crossbar logic operation. The selected operating memristors P and Q in crossbar array are in state 0 (high resistance), all other memristors are in state 1 (low resistance), and voltage V_{COND}

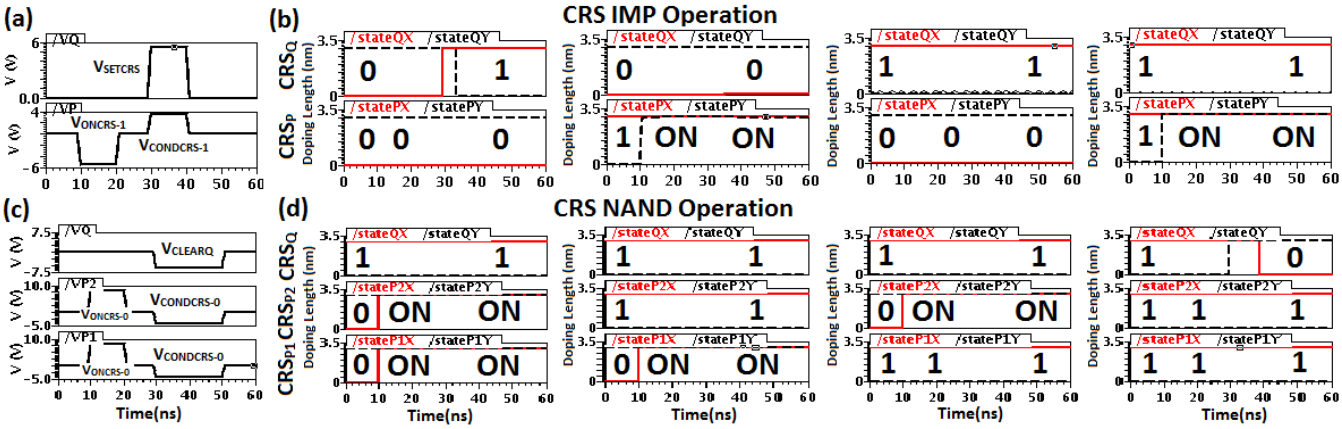


Fig. 7. (a)Voltages for CRS IMP Operation. (b)CRS IMP operation. (c)Voltages for CRS NAND operation. (d)CRS NAND operation.

applies to the selected P memristor (See Fig. 3(a)). The sneak path voltage V_{Msneak} in the selected line (affected by sneak path current) is expressed in (8).

$$V_{Msneak} = \frac{V_{COND} * R_G}{\frac{2*m-1}{(m-1)^2} * R_{ON}} \tag{8}$$

For CRS based crossbar logic, every CRS cell is in state 1 or state 0. So they have the same resistance values $R_{State0} = R_{State1} \approx R_{CRS}$. Assume the cells in crossbar first row are CRS_Q, and CRS_P has $m \times m$ matrix as Fig. 3(b) shows. Both operation CRS cells are in state 0. Other cells are in state 1. The sneak path voltage V_{Csneak} affected by sneak path current in CRS crossbar is shown in equation (9).

$$V_{Csneak} = \frac{V_{CONDCRS-1} * R_G}{\frac{2*m-1}{(m-1)^2} * R_{CRS}} \tag{9}$$

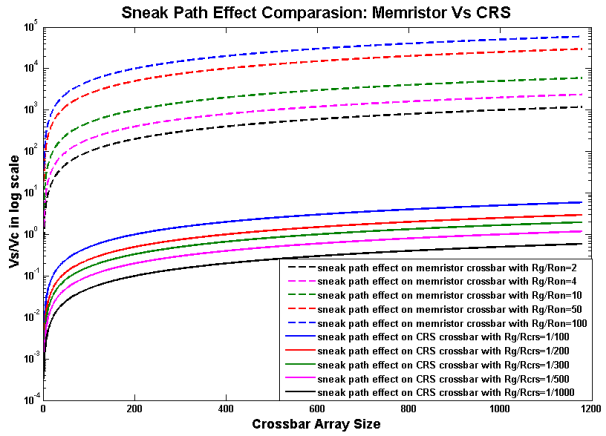


Fig. 8. Sneak path worst case comparison

Fig. 8 shows the worst case sneak path comparison between memristor and CRS. In this figure, y-axis is V_S/V_C in log scale. V_S represents V_{Msneak} for memristor crossbar array and V_{Csneak} for CRS. Vc is V_{COND} for memristor crossbar and $V_{CONDCRS-1}$ for CRS. The result of V_S/V_C expresses the impact of sneak path in crossbar array, x-axis is the crossbar array size. From this figure, the ratio of R_G with R_{ON} and R_{CRS} plays a key role in sneak path voltage calculation. When the ratio of V_S/V_C gets smaller, the sneak path effect is reduced. Due to R_{ON} for memristor worst case calculation, memristor crossbar logic has a worse sneak path current issue. Increasing the value of R_{ON} can reduce the sneak path current effectively. However when R_{ON} is equal to or larger than R_G, this can make the memristor stateful logic operation unsuccessful. For CRS crossbar logic, R_{CRS} is much larger than R_G which makes the sneak path effect minor. Increasing the value of R_{CRS} can improve the performance.

V. Conclusions

CRS can effectively reduce the sneak path in CRS arrays like crossbar structure. CRS based crossbar is more suitable than memristor based arrays for stateful logic operation. In this paper, a CRS stateful logic scheme is explored. IMP operation can be performed with two different types of CRS cells. We have demonstrated CRS IMP and NAND operation. One additional step is required compared to memristor IMP operation. Using basic NAND operation, all logic function can be implemented. Furthermore, only 4 steps are required for implementing N input NAND gate whereas memristor based stateful logic needs N+1 steps. The most important feature of our proposed NAND CRS logic is its reduction in sneak path current and constant computational steps, which will be very useful for logic design compared to memristor implication which requires variable number of steps depending on the number of inputs.

Acknowledgments

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