A Hybrid Non-Volatile SRAM Cell with Concurrent SEU Detection and Correction

Pilin Junsangsri and Fabrizio Lombardi
Electrical and Computer Engineering
Northeastern University
Boston, MA, USA
junsangsri.p@husky.neu.edu, lombardi@ece.neu.edu

Jie Han
Electrical and Computer Engineering
University of Alberta
Edmonton, Canada
jhan8@ualberta.ca

***Abstract*—This paper presents a hybrid non-volatile (NV) SRAM cell with a new scheme for SEU tolerance. The proposed NVSRAM cell consists of a 6T SRAM core and a Resistive RAM (RRAM), made of a 1T and a Programmable Metallization Cell (PMC). The proposed cell has concurrent error detection (CED) and correction capabilities; CED is accomplished using a dual-rail checker, while correction is accomplished by utilizing the restore operation; data from the non-volatile memory element is copied back to the SRAM core. The dual-rail checker utilizes two XOR gates each made of 2 inverters and 2 ambipolar transistors, hence, it has a hybrid nature. Extensive simulation results are provided. The simulation results show that the proposed scheme is very efficient in terms of numerous figures of merit such as delay and circuit complexity and thus applicable to integrated circuits such as FPGAs requiring secure on-chip non-volatile storage (i.e. LUTs) for multi-context configurability.**

Keywords— Memory Cell, Programmable Metallization Cell (PMC), SEU, Detection, Correction, Emerging Technology

I. INTRODUCTION

Scaling of CMOS has been made possible by improved fabrication/manufacturing as well as design techniques. So-called *emerging technologies* have been widely reported to supersede or complement CMOS. Integration of significantly different emerging technologies with CMOS has gained attention, thus creating new possibilities for designing circuits and systems. This type of design style is commonly referred to as "hybrid" [1], because it exploits different characteristics of emerging technologies. One of the emerging technology-driven paradigms in memory systems is represented by the so-called *non-volatile* resistive RAM (RRAM) [2]. Different non-volatile SRAM (NVSRAM) cells have been proposed in the technical literature. The volatile data held in the SRAM core is replaced with the data held in the non-volatile storage when a restore operation on power-up is performed. Non-volatile elements based on resistive switching such as memristor have been recently proposed for NVSRAM implementation [3]. Security constraints as well as multi-context configurability (i.e. the capability to store and operate under multiple sets of configuration data) require non-volatile operation in programmable chips such as FPGAs; hence non-volatile elements have been proposed as an addition to SRAMs in FPGAs [4]. Despite these advances, the reliable operation at nanometric feature sizes remains of significant concern [5]. The amount of charge stored on a circuit node is becoming smaller due to the lower supply voltage and the smaller node capacitance. This makes circuits more susceptible to spurious voltage and charge variations caused by *externally induced phenomena,* such as cosmic ray neutrons and α-particles [6]. In a memory circuit, the transient voltage changes that is generated by a heavy ion strike, may directly lead to a *Single Event Upset* (SEU) as a state change of the memory cell [6]. A SEU is said to occur when the collected charge Q at a particular node is greater than the critical charge, Q_{crit}, i.e. Q_{crit} is the *minimum charge* that needs to be deposited at the sensitive node of a storage cell to flip (change) the stored bit (data). Usually for a 6T SRAM core, Q_{crit} is found at one of the storage nodes, i.e. DN or D. H*ardening* has been utilized for designs to tolerate a single SEU in storage elements such as memories and latches. An example of a hardening approach in memory design is known as DICE [7] and uses twice the number of transistors of a standard storage cell (i.e. 12T vs. 6T). A different hardened memory design requiring 11 transistors (i.e. 11T) has been proposed in [4].

This paper proposes a PMC-based NVSRAM cell with a new scheme for SEU tolerance. It considers the node of least charge (i.e. the critical charge) for mitigating a SEU by accomplishing both detection and correction. Simulation results show that the proposed scheme is very efficient in terms of numerous figures of merit.

II. PROPOSED NVSRAM CELL

In this section, the operational principles of the proposed NVSRAM cell are presented. This NVSRAM cell consists of two parts: a volatile (6T) SRAM core and a RRAM circuitry (consisting of a 1T and a 1X, where X denotes the type of resistive element). The proposed cell (7T1P; X=P as it uses a PMC as non-volatile storage element) is shown in Fig. 1.

A. Write (Store) operation: (Both SRAM and PMC)

Write '0' Operation: To write '0', the value of the voltage at D must be at GND, while the value of the PMC resistance must be R_{OFF} (high resistance). Data is written in the SRAM by setting the voltages at BL and BLB to GND and V_{DD} respectively and the voltage at WL of the selected cell to V_{DD}.

978-3-9815370-2-4/DATE14/©2014 EDAA

Fig. 1. Proposed non-volatile SRAM (7T1P) cell

Transistor M7 is turned ON to write data into a PMC, because the changing rate of the PMC resistance is related to the voltage difference across it (by increasing the supply voltage and the voltage at Ctrl1 to the threshol voltage of the PMC V_{dh} during the write operation); so the PMC is written with the data corresponding to the voltages at D and Ctrl2. As the voltage at node D is at GND and the voltage at Ctrl2 is at V_{dh}, then a negative voltage is dropped across the PMC and its resistance is set to the OFF state (R_{OFF}).

Write '1' Operation: In this case, the voltage at node D must be at V_{DD} while the PMC resistance must be placed in the ON state (low resistance). So, the voltage at WL must be at V_{DD} for selecting the memory cell, while the voltages at BL and BLB are at V_{DD} and GND respectively. The voltage at D is increased by increasing the supply voltage of the 7T1P cell to V_{dh}. M7 must be ON to generate the voltage difference across the PMC. So, the voltage at Ctrl1 is V_{dh}, while the voltage at Ctrl2 is at GND. A voltage difference across the PMC exists and the write '1' operation is executed.

The write operation of the 7T1P requires one clock cycle and stores data in both the SRAM and the PMC.

B. Restore Operation

The restore operation transfers (copies) the data stored in the PMC to the SRAM cell, i.e. at node D. The data stored in the PMC is read by setting the voltages at Ctrl1 and Ctrl2 to GND and V_{DD} respectively. If a '0' ('1') is stored in the PMC, the voltage at DP is at GND (V_{DD}). For the restore operation, V_{WL} is set at V_{DD}, while voltages at BL and BLB are varied depending on the stored data, i.e. for a '0' ('1') in the PMC, the voltages at BL and BLB are given by GND and V_{DD} (V_{DD} and GND) respectively and the voltage at D is at GND (V_{DD}).

C. Instant-On Operation

When the supply voltage is lost, the voltage at D is also lost due to the volatile nature of the SRAM core. The instant-on operation is employed to bring back the value stored in the resistive element to the SRAM core. M7 is turned ON by setting the voltages at Ctrl1 and Ctrl2 at values larger than V_{DD}; the voltage at D varies depending on the value of the PMC resistance. Due to the high value of the PMC resistance in state '0', an uncertainty may exist due to a discharging node between D and DN. However, the ON state resistances of M1 and M7 are less than the resistance of the PMC; so, the voltage at D is at 0V. If a '1' is stored in the PMC (with a low value of resistance), the voltage at D is at V_{DD} while the voltage at DN is discharged through M3. Therefore, the data in the PMC is correctly restored to D.

III. Concurrent Error Detection

To detect a difference in values between the data stored in the SRAM and the PMC, Concurrent Error Detection (CED) is employed; a dual-rail checker is utilized by connecting two XOR gates in parallel as shown in Fig. 2a.

Fig. 2. a) Dual-rail checker for CED b) Proposed XOR gate using ambipolar transistors c) Model of ambipolar transistor

The proposed design is hybrid in nature, because it utilizes ambipolar transistors in the XOR gates for the dual-rail checker. Two ambipolar transistors and two inverters are used (Fig. 2b). The two input signals are given by IN1 and IN2, while the output of the XOR gate is Out. The following cases are possible in the operation of the XOR gate.

(1) *Both IN1 and IN2 are '0':* Since node IN2 is connected to the polarity gate of the ambipolar transistors, both ambipolar transistors behave as NMOS when IN2 is set to GND. So, the ambipolar transistors operate based on the voltage at IN1. IN1 is at GND, so the ambipolar transistors AMB1 and AMB2 are ON and OFF respectively. The voltage at O1 is given by the difference between the supply voltage and the threshold voltage drop across AMB1 (V_{DD}–V_{th}). Therefore, the output voltage (V_{Out}) is at GND. (2) *IN1 and IN2 are '0' and '1' respectively.* In this case, both ambipolar transistors behave as PMOS; AMB1 is OFF, while AMB2 is ON. The voltage at O1 of the proposed XOR gate is given by the threshold voltage of the ambipolar transistor (V_{th}), so the output voltage is given by V_{DD}. (3) *IN1 is '1' and IN2 is '0'.* In this case, both ambipolar transistors behave as NMOS; AMB1 is OFF, while AMB2 is ON. The voltage at O1 is at GND, so the voltage at Out is at V_{DD}. (4) *IN1 and IN2 are '1'.* Both ambipolar transistors behave as PMOS. AMB1 is ON, while AMB2 is OFF. The voltage at O1 is at V_{DD} and its output voltage is at GND. Hence, the circuit of Fig. 2b correctly operates as an XOR gate.

A two-input CMOS XOR gate employs at least 8 transistors, while two more inverters are needed to generate the reverse input logic. The total number of transistors is increased to 12. The utilization of ambipolar transistors reduces the number of transistors and improves power dissipation [8].

Consider the operation of the dual-rail checker in the absence of an SEU; the copies of the data stored in the SRAM at D and in the RRAM at DP are the same. Two comparisons between the node pairs D and DP and DN and DP are executed to establish the CED feature. The dual-rail checker is connected to the proposed NVSRAM cell (Fig. 1); for CED, M7 is turned OFF, while the voltage at Ctrl2 is at V_{DD}, the voltages at the three nodes are provided as inputs to the two XOR gates.

Since both the RRAM and the SRAM are written during the write operation, then they are monitored by the dual-rail checker. If either an SEU does not cause a logic inversion in the SRAM or there is no SEU, then $V_{DP} = V_D$. However If a SEU causes a logic inversion in the SRAM, then $V_{DP} = V_{DN}$. The outputs of the dual-rail checker ensure that a single fault occurring in one of the XOR gates will be detected as generating an invalid code at the output, i.e. this circuit is self-checking too. When $V_{ER1}=V_{DD}$ and $V_{ER2}=0$, the restore operation is required. As described previously, the restore operation permits the data stored in the PMC to be written back in the SRAM core, thus correcting the SEU.

IV. SIMULATION RESULTS

In this section, the proposed NVSRAM cell is evaluated by simulation. HSPICE is utilized as the simulation tool, while the model of [9] is employed for simulating the PMC; the resistance range of the PMC is given by 30kΩ – 100MΩ [9]. The largest values for the CF height (L) and CF radius (R) of the PMC are given by 1.5nm and 25.2nm respectively, while the threshold CF height (h_{th}) and the radius (r_{th}) of the PMC [9] are selected at the values of 1.45nm and 0.225 nm respectively. The macroscopic model of Fig. 2c is utilized for an ambipolar transistor; the transistor sizes are adjusted to generate the symmetric conduction between the PMOS and NMOS behaviors at 32nm CMOS feature size.

A. Ambipolar-based XOR gate

In Fig. 2b, two inverters and two ambipolar transistors are needed in the proposed XOR gate. The delay, power dissipation and PDP of the proposed XOR gate are assessed at 32nm. As shown in Table 1, the proposed XOR gate encounters a larger delay when the voltage at IN1 is at GND due to the threshold voltage drop across the ambipolar transistor. The worst cases (bold entries) for the power dissipation and the power delay product (PDP) of the proposed XOR occur when one of the inputs is at 1.

TABLE 1 DELAY, POWER DISSIPATION, AND POWER DELAY PRODUCT (PDP) OF THE PROPOSED XOR GATE

State			*Delay (ps)*	*Power Dissipation (µW)*	*PDP ($*10^{-15}J$)*
IN1	*IN2*	*OUT*			
0	0	0	324.2	5.1496	1.6695
0	1	1	**338.3**	14.1325	**4.781**
1	0	1	7.9	**105.353**	0.8323
1	1	0	36.5	27.4792	1.003

B. Critical charge

A Single Event Upset (SEU) in a SRAM cell occurs when a charged particle strikes the most sensitive node and flips the state of the SRAM cell, causing a change in stored data. The sensitivity of SRAM to radiation is quantified by the critical charge parameter, Q_{crit}, as the least amount of charge required to change the state of the cell [7]. Table 2 shows the critical charge of the 7T1P cell for the three nodes D, DN and DP for ‘0’ and ‘1’ as data stored in the cell. The critical charge is given by the bold entries and occurs always at node DN. Table 2 confirms that the node at the resistive element has a very high charge and the data stored in the resistive element is not connected to the node of critical charge, i.e. unlikely to be affected by a SEU. The charge at DP is larger than the critical charge; this is caused by the resistance value and the voltage across the PMC.

TABLE 2. CHARGE OF NODES D, DN, AND DP OF THE PROPOSED 7T1P CELL

Node	*Charge for Stored Data Value (C)*	
	'0'	*'1'*
D	$6.1504*10^{-16}$	$6.1802*10^{-16}$
DN	**$5.9049*10^{-16}$**	**$5.9536*10^{-16}$**
DP	$9.5062*10^{-15}$	$9.3147*10^{-9}$

C. Write and Read operations of NVSRAM:

To write to the 7T1P cell, data must be written to D and the PMC. As mentioned previously, the supply voltage and the voltage at Ctrl1 must be increased to V_{dh}, while the voltage at Ctrl2 must have an opposite value of the data to be stored. V_{dh} is related to the voltage difference across the PMC, in this paper, V_{dh} is 3.5V.

TABLE 3. DELAY, POWER DISSIPATION, AND PDP FOR WRITE, READ, AND RESTORE OPERATIONS OF THE PROPOSED PMC-BASED NVSRAM CELL (PMC RESISTANCE IS 100MΩ AND 70KΩ);

Operation	*Write*		*Read*		*Restore*	
	'0'	*'1'*	*'0'*	*'1'*	*'0'*	*'1'*
Delay (ps)	0.023	**3.827**	7.81	**8.61**	18.90	**22.56**
Power dissipation (µW)	**871.2**	795.271	**9.684**	9.389	**25.862**	21.32
PDP ($*10^{-15}J$)	0.020038	**3.044**	0.0756	**0.081**	0.4678	**0.481**

Table 3 shows the delay, power dissipation and power delay product (PDP) of the proposed 7T1P cell for both cases of the write and the read operations. The write '0' operation is faster than the write '1' operation; during the write '1' operation, the PMC resistance is reduced and the voltage difference across the PMC also decreases, thus the switching time of the PMC is slower. The power dissipation (PDP) of the write '0' operation is higher (lower) than the write '1' operation for the same reasons. The write operation of DICE takes 5.011ps at 32nm feature size; despite the presence of the RRAM, the proposed cell has better performance than DICE because the SRAM core in the NVSRAM utilizes the 6T configuration rather than the feedback arrangement of [7].

The read operation involves both the SRAM and the RRAM. The process of precharging the bitline voltages (BL and BLB) to V_{DD} is initiated prior to the read operation; the word line voltage (V_{WL}) of the selected memory cell is then at V_{DD}, such that the voltage stored in the SRAM cell is made available at both BL and BLN. The read ‘0’ operation has the least delay, and the least power dissipation (but the highest PDP) is accounted for the read ‘1’ operation (Table 3). For comparison purposes, the read operation of DICE takes 10.041ps at 32nm, again higher than the proposed scheme.

For reading the RRAM, the PMC resistance is monitored as the voltage at node DP. The data stored in the PMC is found by having the voltage of node Ctrl1 at GND (to turn OFF transistor M7 and separate D and DP); also the voltage of Ctrl2 must be at V_{DD}. If a '0' is stored in the RRAM (i.e. the PMC resistance is very large), the voltage at DP is very small; if a '1' is stored in the RRAM (so the PMC resistance is very small), when the voltage at Ctrl2 is at V_{DD}, the voltage at DP

increases to V_{DD}. So by measuring the voltage at DP during the read operation, its delay is 1.923ps, smaller than the delay for reading the SRAM core.

D. Dual-rail checker:

TABLE 4. VOLTAGES AT D, DN, DP OF 7T1P CELL AND OUTPUT VOLTAGE, DELAY TIME, POWER DISSIPATION AND PDP OF PROPOSED DUAL-RAIL CHECKER

Input (V)			Output (V)		Delay	Power	PDP	Status
V_D	V_{DN}	V_{DP}	V_{ER1}	V_{ER2}	(ps)	Dissipation (µW)	($*10^{-15}J$)	
0	V_{DD}	0	0	V_{DD}	**365.4**	5.43125	**1.98458**	NO SEU
0	V_{DD}	V_{DD}	V_{DD}	0	321.6	4.03484	1.2976	SEU
V_{DD}	0	0	V_{DD}	0	364.5	4.19548	1.52925	SUE
V_{DD}	0	V_{DD}	0	V_{DD}	301.4	**5.77171**	1.73959	NO SEU

Next, performance of the dual-rail checker is established. By using the proposed XOR gate (Fig. 2b) and connecting the voltage at DP to both the polarity gates of the ambipolar transistors, Table 4 shows the delay, power dissipation and power delay product (PDP).

The worst case for the delay and the PDP occurs when a '0' is stored at both D and DP (this corresponds to one of the fault free cases); the other fault free case (i.e. for '1' at both D and DP) accounts for the worst power dissipation. For comparison purpose, consider a CMOS implementation of a dual-rail checker. The CMOS XOR gate of [10] is used in place of the proposed ambipolar-based XOR gate. This CMOS gate requires 12 transistors, so the total number of transistors in a CMOS-based implementation of a dual-rail checker is 24. The delay, power dissipation and PDP of a CMOS-based dual-rail checker are shown in Table 5.

TABLE 5. VOLTAGES AT D, DN, AND DP OF A 7T1P CELL AND OUTPUT VOLTAGE, DELAY TIME, POWER DISSIPATION AND PDP OF A DUAL-RAIL CHECKER IMPLEMENTED IN CMOS

Input (V)			Output (V)		Delay	Power	PDP
V_D	V_{DN}	V_{DP}	V_{ER1}	V_{ER2}	(ps)	Dissipation (µW)	($*10^{-15}J$)
0	V_{DD}	0	0	V_{DD}	**58.46**	22.4873	**1.31461**
0	V_{DD}	V_{DD}	V_{DD}	0	51.12	15.6201	0.798497
V_{DD}	0	0	V_{DD}	0	57.92	**22.6245**	1.31041
V_{DD}	0	V_{DD}	0	V_{DD}	52.82	15.3855	0.812661

This circuit is faster and has a better PDP, however it incurs in a larger power dissipation and requires a larger number of transistors compared with the proposed ambipolar-based implementation.

E. Restore operation:

Data correction occurs when a SEU has affected the SRAM core and its occurrence is detected by the dual-rail checker. So following the detection for the two faulty cases (i.e. DN=DP), a restore operation takes place to copy back the value of the data stored in the RRAM to the SRAM core. The voltage at WL is at V_{DD}, while V_{BL} and V_{BLB} are selected depending on the value to be restored, i.e. the voltage at D is made the same as the voltage at DP. The simulation results in Table 3 show that the worst values (bold entries) for the delay and PDP (power dissipation) are encountered when a '1' ('0') is restored.

It should be noted that as commonly found in coding circuits, a dual-rail checker is used for the word output of a memory; in this arrangement, error detection and correction are evoked once a read operation is executed and the voltages at D, DN and DP are checked. The correction of the SEU requires more time to be corrected using the proposed scheme than by hardening [7][11] due to delay in the CED circuitry.

V. CONCLUSION

This paper has presented a novel approach to concurrent error detection and correction of a SEU in a new memory cell. The proposed memory cell is hybrid in nature because it utilizes a 6T SRAM core, a RRAM consisting of a 1T and a Programmable Metallization Cell (PMC) as non-volatile resistive element, two XOR gates in a dual-rail checker scheme (in which each XOR gate consists of a two ambipolar-based implementation). Different from other SEU tolerant cells [7][11], the proposed memory cell is non-volatile and utilizes a dual-rail checker for concurrent error detection and the so-called restore operation for correction. In the absence of a SEU, the proposed cell has faster read and write times compared with designs using hardening [7][11]; however, the utilization of the restore operation accounts for a higher delay in SEU correction. The utilization of a PMC results in a very large resistive range, low hardware overhead (due to the bridging nature of this type of resistive element), fast switching. This suggests that the proposed cell is best suited for memories requiring non-volatile operation with very frequent read operations (but infrequent write).

REFERENCES

[1] P. Junsangsri and F. Lombardi "Design of a Hybrid Memory Cell Using Memristance and Ambipolarity," *IEEE Transactions on Nanotechnology*, vol. 12, no. 1, pp. 71-80, 2013

[2] H. Akinaga, H. Shima, "Resistive Random Access Memory (ReRAM) Based on Metal Oxides," *Proc. of the IEEE*, pp. 2237-2251, 2010

[3] M. F. Chang, C. H. Chuang, M. P. Chen, L.-F. Chen, H. Yamauchi, P.-F. Chiu, S.-S. Sheu, "Endurance-Aware Circuit Designs of Nonvolatile Logic and Nonvolatile SRAM Using Resistive Memory (Memristor) Device", *2012 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 329-334, 2012

[4] X. Xue, W. Jian, Y. Xie, Q. Dong, R. Yuan, Y. Lin, "Novel RRAM Programming Technology for Instant-on and High-security FPGAs," *2011 IEEE 9th International Conference on ASIC (ASICON)*, pp. 291-294, 2011

[5] S. Lin, Y.B. Kim and F. Lombardi, "Soft-Error Hardening Designs of Nanoscale CMOS Latches," *Proc. IEEE VTS* 2009, pp. 41 - 46, 2009

[6] P.E. Dodd and L.W. Massengill, "Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics," *IEEE Transactions on Nuclear Science*, pp. 583 - 602, June 2003

[7] T. Calin, M. Nicolaidis, R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology," *IEEE Transactions on Nuclear Science*, Volume 43, Issue 6, Part 1, pp. 2874 - 2878, Dec. 1996

[8] M. H. B. Jamaa, K. Mohanram, G. D. Micheli "An Efficient Gate Library for Ambipolar CNTFET Logic" *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems,* Vol. 30, No.2, Feb 2011

[9] P. Junsangsri, J. Han and F. Lombardi, "Macromodeling a Phase Charge Memory (PCM) Cell by HSPICE," *Proc. IEEE/ACM Int. Symposium on Nanoarchitectures,* pp. 77-84, Amsterdam, July 2012.

[10] R. J. Baker "CMOS Circuit Design, Layout, and Simulation" *Wiley-IEEE Press,* Revised 2nd Edition, 2011

[11] S. Lin, Y.B. Kim and F. Lombardi, "A 11-Transistor Nanoscale CMOS Memory Cell for Hardening to Soft Errors", *IEEE Transactions on VLSI Systems*, Volume 19, Issue 5, pp. 900 - 904, May. 2011