System Integration - The Bridge between More than Moore and More Moore

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***Abstract*—System Integration using 3D technology is a very promising way to cope with current and future requirements for electronic systems. Since the pure shrinking of devices (known as "More Moore") will come to an end due to physical and economic restrictions, the integration of systems (e.g. by stacking dies, or by adding sensor functions) shows a way to maintain the growth in complexity as well as in diversity which is necessary for future applications. This so called "More than Moore" approach complements the conventional SoC product engineering. This paper gives insights in System Integration design challenges from different perspectives, ranging from design technology over MEMS product engineering and 3D interconnect to automotive cyber physical systems.**

Keywords—System Integration; NoC (Networks on Chip); Design Space Exploration; Packaging; MEMS

I. INTRODUCTION

The multitude of new integration technologies opens many new possibilities for building electronic systems in a confined space and with high efficiency in terms of power dissipation and performance. In particular, the use of the third dimension in the backend/package allows combining products from different semiconductor as well as MEMS technologies. Thus, these advanced integration technologies link the requirements for high performance (More Moore) with the demand for functional and technological diversity (More than Moore).

High-end applications that require high data throughput, such as systems with the new Wide I/O memory cannot be realized by conventional PCB technologies. They benefit notably from advanced system integration processes. A second application field is the implementation of heterogeneous systems where memory, processors, analog and RF modules (see Fig.1 for an example) are built with sensors in a confined space that could not, or only with great effort, be integrated as SoC. Additional advantages are short signal paths and consequently lower power consumption of the integrated systems.

Already, advanced packaging technologies, such as embedded wafer level ball grid arrays (eWLB), are in use in series production. They allow the combination of several dies and some passive components in a common housing. Another solution is the use of interposer (2.5D system integration). In the future, 3D-Integration will be the most effective kind of integration. But the introduction of this 3D integration requires additional new manufacturing technologies, such as Through Silicon Vias (TSVs) and handling of thinned wafers. After more than ten years of technology development in this area, a sharp increase in the number of TSV-based products is expected in the coming years.

The development of 3D integrated systems also imposes high and in particular new demands on the design process, which can be covered only partially by the current 2D design software. Special requirements also arise in the test development, both for the individual component or die and for the entire integrated system.

In this paper current research results are presented for the design automation of integrated systems. The main focus is on set on MEMS as well as 3D systems. After this introduction the paper is structured as follows:

The next section addresses the design methods and how to navigate through the design space. After a brief insight in packaging, section 3 covers the topic of technology design for MEMS as well as 3D stacking processes. The challenges for inter and intra chip communication using networks on chips (NoC) in three-dimensional IC stacks are described in section 4. The paper terminates with insights to industrial application in section 5 followed by a conclusion.

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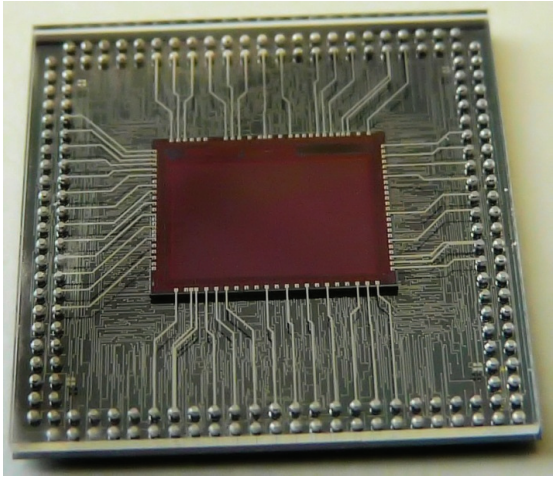

Fig. 1. Example for a heterogeneous integrated 3D-system

II. DESIGN TECHNOLOGY FOR 3D INTEGRATED SYSTEMS

Future 3D integration technologies offer many different possibilities to combine dies into a system. Such integration technologies are for example the well-known and industrially used System in Package (SIP) integration. A complex demonstration example is shown in Fig. 2. In this 3D integration scheme the dies can be arranged stacked or side by side onto a silicon or organic substrate. The connections between two dies or a die and the substrate are established by wire bonds or by balls and flip-chip mounting of the dies.

Another integration technology uses very thin contacts from the front side to the back side of the silicon carrier – called through silicon vias (TSVs). If the silicon carrier is an active die then the scheme is called 3D integration, otherwise if the silicon carrier is an interposer it is termed 2.5D integration. An example is presented in Fig. 3. Both technologies have the advantage of very high density interconnect integration compared for example to the SIP approach.

But not in all cases such high density integration is needed. For example, in heterogeneous systems with analog sensors and actors and digital control, the analog parts are mostly connected with only some interconnects. For these parts of the systems older and cheaper integration technologies like bond wires are enough.

With the availability of these new integration technologies a multitude of new alternatives for the realization of a specific system come up. The system designer must decide for example:

- how many dies should be used
- which semiconductor technologies should be used for each of the dies (different technologies are possible)
- the arrangement of the dies (stacked or side by side or a combination of both or another special technology like eWLB)
- the assembly technology like balling od bond wires

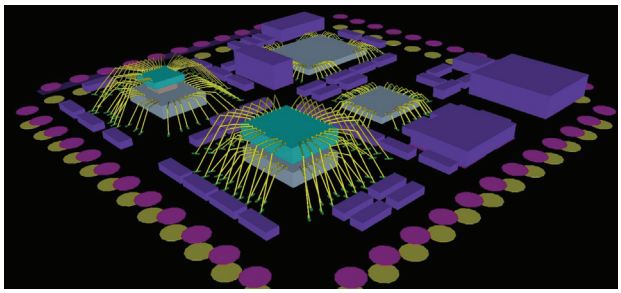

Fig. 2. A complex System in Package (SIP) example

The system designer must also consider the congestion in the different metal layers and in the connection layers. The connection layers (balls, bond wires, etc.) of 3D-integreated systems are critical because these parts have high area requirements. Interconnects are critical because their width is significantly different depending on their location in the system. Within chips the widths are in the range of some hundreds of nanometers whereas on the interposer level or on the redistribution layer of the eWLB they are in the order of some micrometers. The largest dimensions are necessary on the PCB level where dimensions of more than 100 µm are reached. Accurate estimates of the congestion in the metal and congestion on these structures are essential for a successful design space exploration (DSE). In the literature [15], [16] different estimation methods are proposed, for example simple table or stochastic based ones. But both methods are limited to nearly similar dimensions of the interconnects and/or to nearly similar topologies of the 3D-Systems. For our work we use a novel method – a multigrid, multilevel fast routing estimation. With these methods we can estimate the congestion on a coarse level and so we are able to compare different implementation variants of the 3D-system.

With such congestion estimation method as an inner loop a stochastic based DSE can be developed, which is shown in Fig. 4, where routing simulation results are shown: green boxes indicate low congestion, red boxes high congestion.

The main optimization goal of the DSE is the manufacturing cost of the whole 3D-system. For this reason we have created a manufacturing cost function (similar to [17], [18]), which consists of two parts. Part one is a generic, company independent function and the second part is used to set company dependent parameters for the first part and also includes some new functions. The functions consider geometry parameters of available 3D systems like size of the die, number of balls etc., which can be combined with all well-known arithmetic operations. Some constraints for the optimization

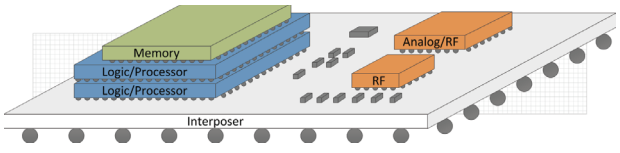

Fig. 3. A complex system build up by a combination of 2.5D and 3D integration

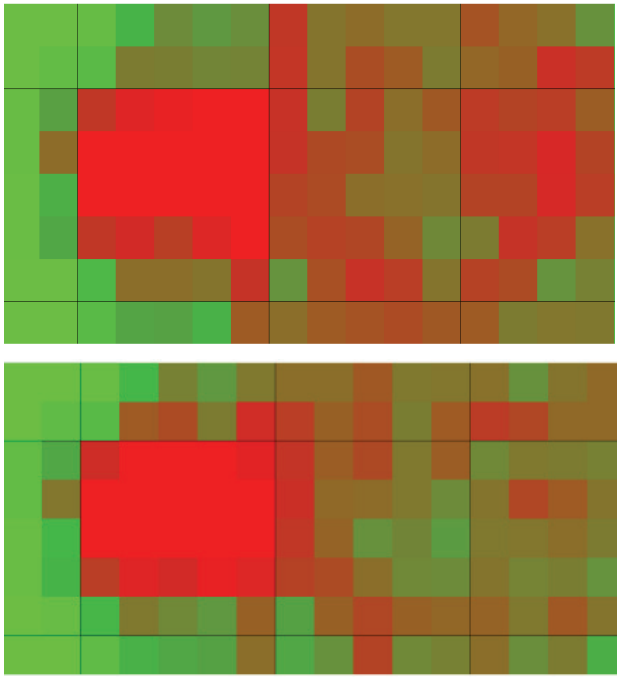

Fig. 4. Results from the multigrid, multilevel fast routing method (for one selected metal layer) for two different 3D-system configurations.

are also needed, for example for the maximum temperature. Such constraints can be modeled also as costs extending the manufacturing cost function. The input of the DSE is a so called module graph, which describes the modules of the system and there dependencies. This module graph can be derived from different abstraction levels in the design e.g. from high level behavior modelling languages like SystemC or from the register transfer level (RTL) and the languages like Verilog or VHDL. Also a technology database is used to describe possible chip, assembly and stacking technologies. This data base and the resulting 3D-system of the DSE is checked for manufacturing aspects by technology check like the one described in Section III.

A. Wafer Level Packaging

For a successful system the housing of the integrated individual dies is a decisive factor. Different market segments from mobile communication and consumer to automotive see the increasing need to focus on system integration on less space instead of single components or functional groups. This drives advanced semiconductor packaging to diversify and become fairly more complex, but at the same time an integrated functional part of the system. The demand for more and more diversified functionality on same or even less space drives the development of "More-than-Moore" (MtM) solutions in the packaging world. The keyword is again "System-in-Package" (SiP). Chip-Package-Board Co-Design and Co-Development are essential key for success. It can be shown on some real product examples where system integration in the package saved up to 4X space on the board for the same functionality with even more performance. While today the majority of SiP is still realized using laminated organic substrate interposers, the need to close the gap to System-on-Chip (SoC) performance is driving closer distances of the single functional elements to each other. This can be realized by Fan-Out Wafer Level Packaging (FO-WLP) technologies, like eWLB (embedded Wafer Level Ball Grid Array), which overcomes Fan-In Wafer Level Packaging (FI-WLP) limitations especially in terms of system integration, keeping the advantages of scalability and cost efficient batch processing. For stacked 3D-systems with their small footprint the results of the DSE (see Section II) shows problems coming from the limited number of balls between the stack and the PCB. Such problems can be solved by an additional interposer layer or by a redistribution layer (RDL) realized in an additional eWLB step at the bottom of the stack. Such eWLB steps are very cost effective and can help to reduce the total cost of stacked 3D-systems.

III. MEMS PRODUCT ENGINEERING- TECHNOLOGY DESIGN FOR SYSTEM INTEGRATION

Taking into account the diversity of technologies from die manufacturing to packaging (as shown in the previous section) it becomes clear that for product engineering of integrated systems such as MEMS or stacked 3D circuits the constraints and inter-dependencies of design and manufacturing are of special interest. The configuration of these technologies is strongly application specific and design methods differ completely from the approach known from the development of conventional two dimensional ICs.

A. Process Design

Product engineering in the area of microelectronics stresses the aspect of managing complexity since hundreds of millions of devices selected from a set of only few basic components (transistors, diodes etc.) can realize almost any electronic system [3]. For MEMS as well as 3D system integration, managing diversity is much more important. The diversity is manifold and obvious as far as application areas, engineering domains (micro-electrical but also micromechanical or micro-optical etc. regarding e.g. sensors), and manufacturing technologies. This is expressed in the MEMS law stating that every device needs an individually tailored manufacturing process.

The clear separation of manufacturing processes and design in

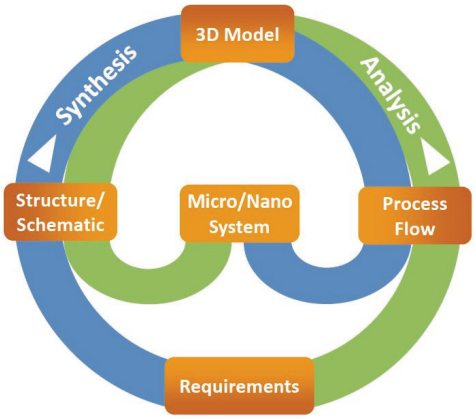

Fig. 5. Pretzel model for MEMS design [4]

terms of a fixed PDK (process design kit) consisting mainly in geometrical and electrical design rules, cannot be adhered in our case. Design and manufacturing are not independent. The design task for MEMS (and with some modifications also for 3D integrated circuits) comprises the structural design as well as the process design which have to be carried out concurrently. For MEMS with micromechanical sensors it is clear that the manufacturing process steps define the third dimension, the height of the structures. Their 3D sizes and material properties etc. are application specific and as crucial for the function of the die as the lateral design. This is expressed in the pretzel model (see Fig. 5).

B. Technology design tools for MEMS

Technology design for MEMS product engineering means to configure an appropriate product specific manufacturing environment. The development of new manufacturing recipes is challenged by a variety of different external and internal requirements and constraints. To cope with this growing complexity in fabrication process development new approaches for adequate process design automation are necessary to cover the design of new process sequences from the very first ideas to the final handover to mass production.

Many properties and parameters have to be taken into account in order to configure a feasible manufacturing process for MEMS. Electronic Design Automation (EDA) methods and software are necessary for structural design but also for the technology design branch. In earlier projects a process design execution system (PDES) was developed. XperiDesk is commercially available and covers most of the requirements for MEMS process design [5]. Fig. 6 gives a screenshot of the process editor of XperiDesk.

New process sequences often are based on previous design approaches. Therefore, knowledge management as part of a PDES can provide means to access structured results from earlier developments. The software can facilitate the assembly and storage of new sequences. A designer can use building

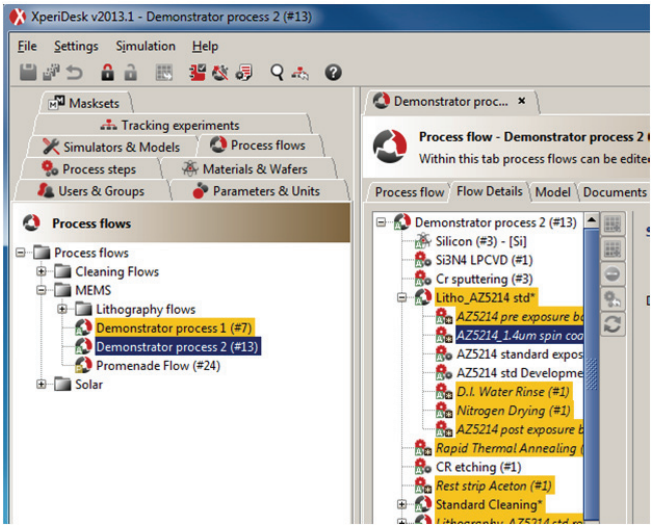

Fig. 6. Process Design Execution System XperiDesk [5]

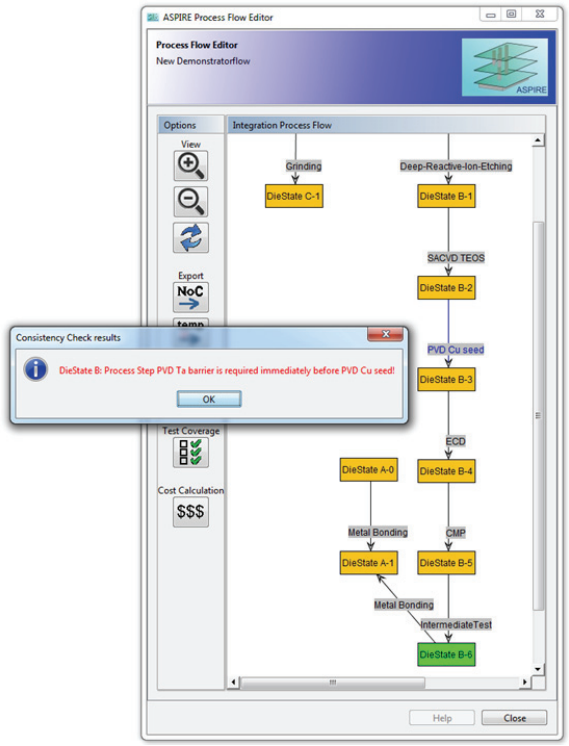

Fig. 7. Process Flow Editor and Consistency Check in ASPIRE.

blocks or modules from previously assembled process sequences within new sequences.

Real benefits are obvious in the process verification phase, where automated consistency checks based on process rules are performed. Most of the rules used can be expressed in a computer-readable way (e.g. do not exceed 160 °C as long as a polymer for lithography is deposited on the wafer).

These checks cannot confirm the functionality or even the structure of the produced device. Technology Computer-Aided Design (TCAD) will have to be used to simulate the process steps and give a sketch of the structure. The PDES supports these ”virtual fabrication” abilities by managing simulation models of different abstraction levels for all process steps (e.g. deposition, etching, and lithography).

C. Process planning for 3D Systems

When system integration is performed in a three-dimensional way, which means the vertical stacking of integrated circuits, to MEMS development comparable mutual dependencies between design and technology exist. The development of 3D systems is a highly complex procedure with a huge variation of possibilities on how to vertically integrate two or more dies. Suitable technology and interconnect structures have to be selected according to the desired application, since product specific constraints affect the selection of process steps. For instance require different kind of applications different sizes of the so-called TSV (through-silicon-vias) that are the commonly used interconnect structures between two dies. In return it is not possible to manufacture all different sizes with the same technology.

3D-Integration technology implies TSV formation, wafer thinning and wafer bonding [1]. In industry different approaches exist for the chronology of these processes. Depending on the time, when the fabrication of TSVs takes place regarding to the IC-processes and the other integration process steps, the integration schemes are often named “via-first”, “via-middle” or “via-last”. In addition different process steps are available to perform e.g. the TSV formation or the wafer thinning. Between these processes several dependencies exist, and the choice of processes is influenced by different die technologies or types of TSVs. In order to support the process engineer in finding an adequate process flow, a process graph model has been developed and implemented in a software prototype [2].

The process flow modelling of a 3D system involves the treatment of two or more dies, so that a plain sequence of process steps is not sufficient. In contrast the process steps of several dies need to be modelled, as well as a merging of different process strands has to be possible. The process graph model (PGM) described in [2] fulfills these requirements. In the PGM an edge represents an integration process step (IPS) and a node represents the current “production state” of a die. Each time an IPS (e.g. an etch process for via formation) is performed, the production state of the die changes, and another node in the graph is reached. This model has been implemented in the Process Flow Editor of the software prototype ASPIRE (Application Specific Integration Flow Evolution). An example of such a process graph is shown in the editor window in Fig. 7. Next to developing a process flow it is possible to validate the flow by checking various constraints, e.g. process conditions or the thermal budget of a die. In the given example the process step “PVD Ta barrier” is missing before the process step “PVD Cu seed” and therefore remarked by the consistency check. With this it is possible to get a manufacturable process flow.

The data needed for the developed process flow is retrieved from an integration technology database, which is part of the ASPIRE software. The database holds information about the materials, process steps, dies, TSVs, process sequences and process flows as well as their respective parameters.

IV. 3D-TSV-HUB: POTENTIALS AND CHALLENGES FOR VERTICAL INTERCONNECTS IN NETWORKS-ON-CHIPS

In System-On-Chip designs, manufactured using stacked die technology, TSVs are best practice to realize inter-die connections like vertical NoC links. However, TSVs are cost intensive under several aspects. Compared to planar metal layer interconnect, area consumption is high due to large TSV diameters and keep out areas. Furthermore, mechanical induced stress can lead to runtime failures and a low overall system yield. On the other hand, TSVs are short and can be operated at a high clock frequency, allowing a high-speed narrow interface using serialization and multiplexing [6-8]. Therefore, in order to ensure that a minimum number of TSVs are performance and cost efficiently operated to their full capacity, a 3D-TSV-Hub has been proposed [8]. It supports virtualizing TSVs, enables a smart mapping of communication flows onto TSVs and provides mechanisms to handle production and runtime failures.

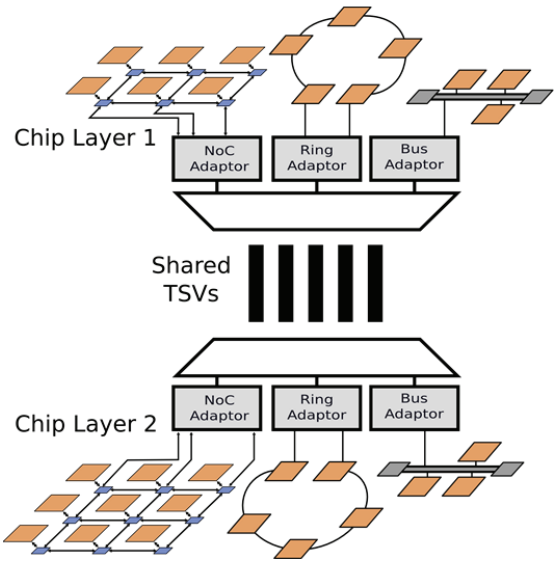

Fig. 8. TSV-Hub concept

For heterogeneous SoC designs, an efficient and cost effective communication subsystem can be realized as an application specific NoC, where the individual links are tailored to the requirements of the communication flows between the IP-Cores. In addition to NoC routers, the TSV-Hub serves as a further building block for creating application specific NoCs. However, generating an application specific NoC is a complex task and usually not feasible manually [14]. Therefore, the instantiation and configuration of TSV-Hubs is part of a NoC synthesis process. From a system design perspective, aspects like compliance to thermal requirements and manufacturing process requirements influence the optimization. In order to consider such factors, NoC synthesis is intertwined with design space exploration and 3D floorplanning. A 3D design flow covering these aspects has been proposed in [19].

A. TSV Hub architecture

The TSV-Hub provides a scalable and flexible module to virtualize a set of physical TSVs connecting two dies. A virtual link layer provides a transportation service for a configurable number of generic virtual links via the same TSV array. The termination of each virtual link can be tailored to the specific needs of the protocol that is transported and to the properties of the design, like the clock distribution and level of synchronicity of different synchronous islands.

The virtual link terminations provide three functionalities:

- Serialization/ deserialization of the incoming/outgoing data stream to adjust it to the number of TSVs provided by the physical TSV array.
- Temporal buffering of a specific number of data words.

- Synchronization between interconnect and TSV clock domain.

The virtual link is configurable regarding several aspects, like the data word size of the link, number of physical data bits (number of data TSVs), relation of the read and write clocks (synchronous, mesochronous, asynchronous), the quality-of-service level (guaranteed service or best effort), the buffer depth of the link at both input and output side type of serializer.

A virtual link can be regarded as a service that provides a certain capacity and can be used by a protocol adaptor to build an inter-die connection. A protocol adaptor might only use one virtual link (e.g. to realize a point-to-point connection) or multiples (e.g. NoC-Link with multiple virtual channels, AXI interface) depending on the properties of the transported protocol.

A built-in scheduler performs dynamic TDMA scheduling considering the bandwidth requirements and QoS level of each of the configured virtual links. Statistical Multiplexing is exploited when best effort links are present. This means the scheduler distributes the available TSV-Hub bandwidth to the virtual links according to their service level and bandwidth requirements. Virtual links requiring guaranteed bandwidth are always served according to their demands. The remaining part is shared among the best effort links. At design time, also the level of serialization is set according to the hub's virtual link setup and the maximal possible TSV clock. Fig. 8 shows an example of the basic concept as a virtualizing wrapper around a physical TSV array, stretching multiple interconnect protocols over two chip layers.

B. Fault Tolerance and Redundancy

One of the major difficulties in building 3D-ICs with high-bandwidth inter-die-connectivity is the low reliability of TSVs. The number of TSVs is reduced by using serialization and multiplexing, thus the overall yield is already improved. However, if no mechanism is applied to handle faulty inter-die connections, the 3D-IC will fail as soon as only one TSV fails. In many works redundancy is introduced by placing spare TSVs that can replace faulty ones [9-11]. We achieve fault tolerance as well by introducing additional TSVs but have a more abstract view. We see a TSV-Hub as a module that provides a certain overall inter-die link capacity. As soon as TSVs fail this capacity is reduced. In order to still provide the nominal bandwidth when faulty TSVs are present, an over dimensioned hub w.r.t. bandwidth is created. If all TSVs are functional this hub provides a higher capacity than specified.

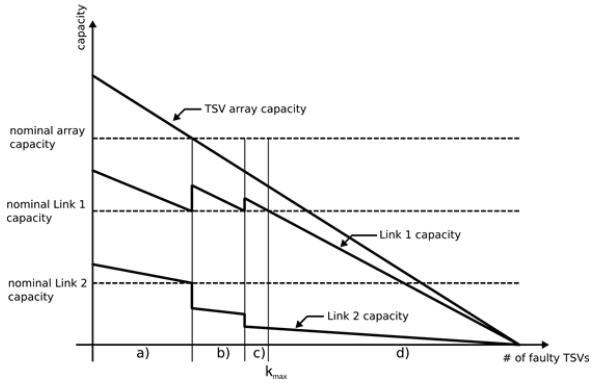

Fig. 9. TSV-Hub Performance w.r.t. number of TSV defects

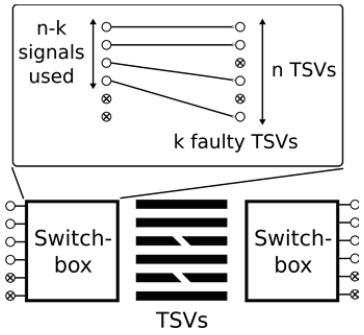

Fig. 10. Switchbox for remapping signals to functional TSVs

Fig. 9 shows qualitatively the impact of faulty TSVs on the bandwidth assignment by the hub's dynamic scheduler for an example with one guaranteed service link (link 1) and one best effort link (link 2). In region a) a higher, than the nominal array capacity is provided. The throughput of both links is reduced with the number of faulty TSVs increasing. As soon as total bandwidth falls below the nominal array bandwidth, the system would have to be considered faulty if the scheduling was not adapted. In the example of Fig. 9, the scheduling is changed such that link 1 gets an additional time slot that is taken from link 2 (b). Thus, we can still maintain the required bandwidth of link 1. This can be repeated when further defects occur (c). In section (d) the hub is considered as non-functional as more TSVs than the maximum tolerable number (k_{max}) fail.

On the logic level the handling of faulty TSVs is enabled by introducing Switchboxes in the data path that perform a dynamic distribution and remapping of the input signals on functional TSVs, excluding the faulty ones. The principle is shown in Fig. 10. The area and complexity of such a switchbox significantly depends on the number of allowed faulty TSVs (k_{max}), hence the maximal number of positions a signal can be shifted if TSV defects occur. K_{max} is a designer's choice that forms a trade-off between logic overhead and level of fault tolerance.

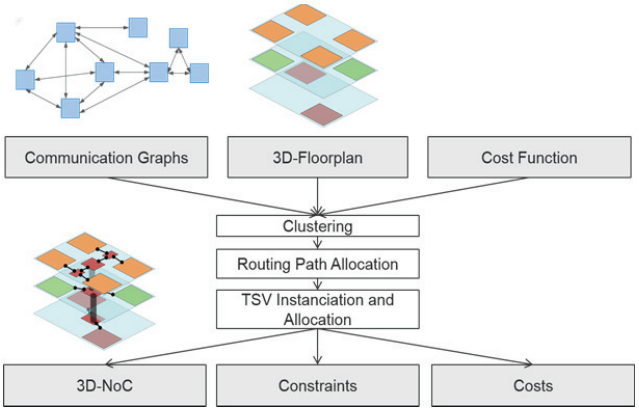

Fig. 11. Steps to generate NoC

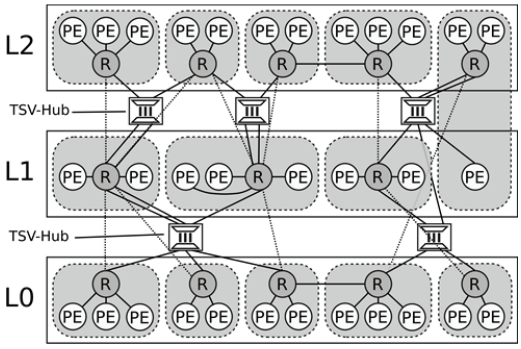

Fig. 12. 3D NoC synthesis result

C. NoC Synthesis

Although, homogeneous 3D mesh NoCs can also benefit from using multiplexing and serialization, the TSV hub is, due to its scalable embodiment, mainly intended for being used in an application specific communication subsystem. In such a system each instance of a hub receives different configuration parameters and is tailored to the needs of the traffic flows that are transported by the hub.

The requirements to the NoC are initially formulated in a Communication Graph that contains the system's IP-Cores as nodes and the communication requirements (flows) as edges. In addition, each flow is part of a use case. Use cases are different application scenarios in which the system can operate. Next to the communication demand an initial 3D floorplan that is obtained from a 3D floorplanner but yet lacks the communication subsystem is considered. Fig. 11 gives an overview on the steps that are subsequently carried out to generate the NoC.

The first phase is an initial clustering where Spectral Clustering [12] is used to obtain a partition of clusters of IP-Cores connected to one router each. Spectral clustering approaches a global optimum such that the affinities in each cluster are maximized and those between the clusters are minimized. The affinities are measures calculated from the bandwidth demands and vertical and horizontal distances. After clustering Routing Path Allocation (RPA) is performed where the links between the routers are created and the flows are mapped on a sequence of links. The mapping of flows is performed in a greedy manner [13], such that additional cost for each mapping is minimized. In a final step inter-die connections are combined using correlation information off the traffic flows in order to maximize the gain when applying statistical multiplexing. For each cluster of vertical links a TSV-Hub is inserted and configured. The synthesis tool is available as a C++ implementation. An XML format is used to describe communication requirement, floorplan and cost information as well as synthesis parameters.

Fig. 12 shows an example for a final outcome of the 3D NoC synthesis process. After NoC synthesis, link costs are calculated for each traffic flow and are further broken down into 2D interconnect costs, 3D interconnect costs and router costs. This allows an exploration tool to evaluate the created

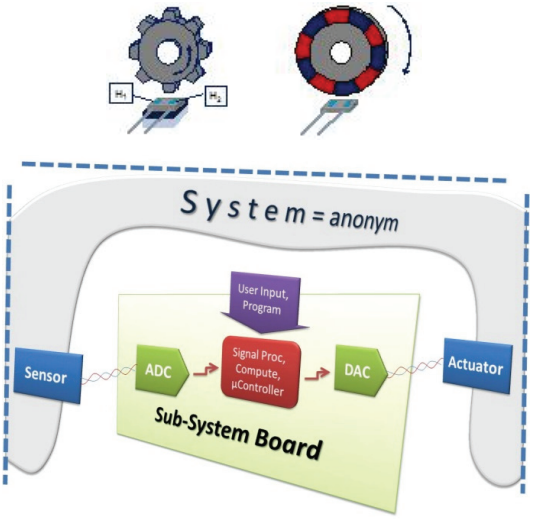

Fig. 13. This figure shows the typical, well known basic concept

NoC and improve the system w.r.t. communication (e.g. changing placement of cores).

V. Automotive Cyber Physical Systems as Example for 3D Integrated Systems

Cyber Physical Systems (CPS) – this new name for systems which consist of collaborating computational, sensing and actuating elements- are perfect examples for the engineering domain addressed here. Sub-Systems for the controlling of physical (or chemical, biological, or other) entities always need some sensor elements and an adequate interface to the computing system: Impedance Adapter, Amplifier, Analog to Digital Converter, wireless or wired signal/data communication /transmission and others. On the other side (the output of the digital units) the electrical digital control signal has to be converted into the physical (or again chemical, biological, or other) domain via DAC (Digital to Analog Converter) and related interfacing components like Buffers, Drivers, Level Shifters to generate the input for the actuator elements (Motors, Pumps, or others).

The development of products based on this concept can be, and is mainly still done by isolated experts or teams for the Sensors, the Analog and the Mixed Signal Components (ADC, DAC) the Microcontroller Chips and the Actuators. The components mentioned are packaged separately and assembled on a PCB – again, the PCB design is done by another expert (team). In the last 5 years design methodology and tooling had been improved a lot to enable so called Chip-Package-Board Co-Design, but the important step to cover a full sub-system including the sensor/actuator topics is still asking for many manual, error prone design tasks. In conjunction with the introduction of the innovative 3D packaging technologies, the design challenges for error free, efficient (mainly measured as NRE-Cost and Time to Market) get a new dimension. It is not only the functionality (according to customer requirements) but also formerly called 2nd order criteria like reliability, testability, safety, manufacturability are becoming most significant to create or keep an outstanding market success. Those challenges ask for a full blown "Multi Physics" design

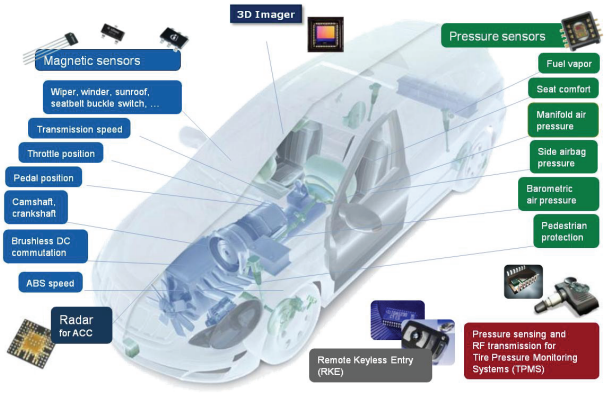

Fig. 14. Sensor portfolio in the automotive domain (Source: Infineon)

environment. Full blown means, that the whole design process is consistently closed. Starting with the requirement management, covering all simulation aspects (models, patter, simulator, data management, parameters including parameter fluctuations), the flow continues with design implementation (layout, 3D mechanical design, etc.) design verification, rule checking, ending with specification compliant validation. The extreme reliability related challenges ask for totally new methodologies and tools driven by the rapidly increasing integration density enabled by 3D technologies. Last but not least all aspects of DtC (Design to Cost) have to be addressed with a high level of cost planning accuracy. This demand on cost planning accuracy comes from the fact, that 3D integration technologies offer a totally new design space. Many different implementation concepts have to be evaluated and compared to get a most competitive solution at the end.

Up to now, only the integration of the Sub-System (Sensor – ADC - µC – DAC Actuator) has been discussed here. But this is only a small part of the upcoming 3D complexity situation. Many of the parameters mentioned above are strongly depended on effects of the next system level.

It becomes clear, that another engineering community has to join the project team. Detailed know how on e.g. car system requirements and behavior is needed. The challenge here is not only to bring the people into a collaborative working style – the tools and the design process (methodology) have to be aligned/linked or even better merged.

The example of the System Car and the Sub-System ABS-Break demonstrates clearly that even this is not the real final request. The breaking conditions for a car strongly depend on the environmental conditions – which means the road, the climate, and finally also the mental situation of the driver. As a result, many more sensor signals have to be collected and evaluated to get a high performance breaking system. Therefore the complete scenario – environment – road – car – driver – and the beak has to be taken into account. At this level there is definitely no methodology and no tool-chain available today: much room for improvement.

Taking these considerations into account device manufacturers will benefit from CPS and 3D technologies especially in the sensor area. Fig. 14 demonstrates a typical sensors portfolio for the automotive market

VI. CONCLUSION

System Integration is a manifold challenge comprising very different design tasks. Design space exploration, application specific technology design, networks on three-dimensional chips and specific packaging approaches are highlighted in this paper. There are certainly more areas that could not be covered here. In any case, these tasks are highly interdependent and therefore have to be executed in an intertwined way. An obvious conclusion regarding the various technologies and application areas seems to be that design and manufacturing of integrated systems have to be supported by appropriate methods and cooperative tools. Procedures and software environments used in the context of conventional IC design must be complemented at least or have to be newly developed to meet System Integration requirements. Beyond the automotive domain other application areas will also profit from the heterogeneous 3D integration, which is an enabler for new economic opportunities.

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