Approximating the Age of RF/Analog Circuits through Re-characterization and Statistical Estimation

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***Abstract*—Counterfeit ICs have become an issue for semiconductor manufacturers due to impacts on their reputation and lost revenue. Counterfeit ICs are either products that are intentionally mislabeled or legitimate products that are extracted from electronic waste. The former is easier to detect whereas the latter is harder since they are identical to new devices but display degraded performance due to environmental and use stress conditions. Detecting counterfeit ICs that are extracted from electronic waste requires an approach that can approximate the age of manufactured devices based on their parameters. In this paper, we present a methodology that uses information on both fresh and aged ICs and tries to distinguish between the fresh and aged population based on an estimate of the age. Since analog devices age mainly due to their bias stress, input signals play less of a role. Hence, it is possible to use simulation models to approximate the aging process, which would give us access to a large population of aged devices. Using this information, we can construct a statistical model that approximates the age of a given circuit. We use a Low noise amplifier (LNA) and an NMOS LC oscillator to demonstrate that individual aged devices can be accurately classified using the proposed method.**

I. INTRODUCTION

As electronic supply chain grows rapidly and more widely, IC devices can be provided from many different suppliers all over the world. However, in some cases, suppliers provide recycled components from used or defective systems. Although these devices may be operating according to specifications at the initial time, they can malfunction much sooner than expected due to various stress and wearout mechanisms. In case of critical applications such as automotive electronics, military systems, and medical devices, counterfeit ICs can result in catastrophic events. A recent study has determined that about 10 percent of the technology products sold worldwide are counterfeit [1], resulting in more than $100 billion of global revenue loss every year.

In effect, counterfeit ICs behave as if they were never tested and quality controlled. Counterfeit ICs that reach the end user are much more expensive to identify compared with earlier detection. Therefore, it is necessary to develop efficient, quick, and low-cost solutions to identify counterfeit ICs prior to their integration into systems. Over the past decade, this problem has been addressed from multiple angles. In [2], an odometer based technique to estimate age was proposed to monitor the reliability of ICs for the future. The same odometer can be used to effectively gauge the age of the devices, hence leading to the identification of recycled components. However, this requires upfront thinking at design time; thus, this method is not applicable to devices that are currently in the market. In [3][4], the authors suggest using physical tests through part authentication tools, visual inspection, and X-ray. However, these kinds of methods require time consuming and high cost processes. In addition, since many applications depend on designs that have been manufactured years ago, distinguishing whether an existing device belongs to an unused or used (counterfeit) IC population is not possible through such authentication methods.

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While there are many ways ICs are stressed in distinct use conditions, extensive research on semiconductor reliability can be used to develop models and tools to estimate how the aging process degrades the performance of the devices that are used in the field [5]-[14]. For digital circuits, aging effects are a function of the environment, as well as the use patterns [15][16]. For analog circuits, which mainly operate in the small signal domain, aging is mainly a function of the bias conditions, which makes it more or less independent of input patterns. Thus, the aging process can be approximated with respect to temperature, humidity, and other environmental conditions [17][18]. Two classes of solutions can be envisioned for the counterfeit IC detection problem. One class of solutions relies on the information from fresh ICs and tries to categorize devices according to whether they belong to the fresh IC population. Another class of approaches uses the information on both fresh and aged ICs and tries to distinguish between the fresh and aged population based on an estimate of the age.

Reliability models and aging mechanisms have been used to enable detection of counterfeit ICs in recent years [19][20]. In [19], path delay information is used as a fingerprint to distinguish aged devices from fresh ones for digital circuits. In [20], the authors present a comprehensive parametric technique for the identification of aged devices using a one-class identifier. One class identifiers are statistical tools that can determine whether a given sample belongs to a certain population, which in this case is the fresh device population. The motivation behind using a one-class identifier is that extensive information exists on the fresh device population whereas the aged device population may present with many different parametric distributions.

In this paper, we present a statistical parametric methodology that takes advantage of aging models and information, and tries to estimate the age of a given device. In this sense, our methodology belongs to the second class of parametric counterfeit detection techniques. We develop and use a simulation framework based on aging models that can estimate the degradation profiles of a large number of samples with process variations, variations/mismatch in aging parameters, and environmental stress (e.g. temperature). We treat the age of a device as an independent parameter. Using a neural network model, we map parametric measurements from the device under test (DUT) to its age. We use two circuits, an LNA and an oscillator [7] as experimental venues. Our experiments show that the age of the devices can be approximated to a degree that it allows identification of counterfeit devices (aged more than 2 years) whereas identifying most fresh devices as such.

II. AGING MECHANISMS IN CMOS TECHNOLOGY

As CMOS technology scales, reliability is considered as one of the most important design challenges for nanometer CMOS technologies. In order to properly describe the counterfeit IC detection, it is required to understand the aging mechanisms in CMOS technology. Aging mechanisms, such as

hot carrier injection (HCI) [5]-[7], and negative bias temperature instability (NBTI) [10]-[12], will cause a change in transistor parameters as a function of time, resulting in continuous performance degradation over time. Even aging mechanisms that are thought to cause sudden and immediate failure in digital circuits may cause parametric degradation in analog circuits.

Parametric variations present the most difficulty in determining the age of a given device. Variations exist both in classical process parameters, such as threshold voltage, and in parameters included in the degradation model, such as the trap generation energy. Hence, it is imperative to take process variations into account. Process variations are classified as die-to-die variations and within-die mismatch variations [15][16].

Hot Carrier injection (HCI) is one of transistor wear-out effects mainly considered for N-type MOSFETs. During hot carrier stress caused by high electric field near the drain region, a carrier at the end of the drain junction gains sufficient kinetic energy, and then it is injected toward the oxide silicon surface. These injected hot-carriers can cause both interface state generation and charge traps which increase the leakage substrate current and decrease drain current. After hot carrier stress, the transistor characteristics, such as threshold voltage and the channel mobility, may shift, changing the characteristics of the device. The threshold voltage degradation under HCI has been derived in [5][10].

III. Simulation Framework for Aging

In order to analyze the effect of the aging mechanisms, degradation models of transistors are used in conjunction with circuit parameters (i.e. voltage, current) to develop a simulation framework. Combined effects of time-dependent aging with both process variations and variations in degradation parameters are modeled to enable aging simulation. We use HSPICE as the circuit simulator and use additional circuit components to model the drift in transistor parameters, such as the threshold voltage [21]. As the transistor ages, it is possible to observe the degradation profiles of circuit specifications gradually over time. In a similar vein, in [12][17], the degradation-based reliability simulation methods are presented with the simulation tools and failure equivalent circuits. However, in prior work, all transistors are assumed to have the same degradation model parameters, which are subject to variations similar to the variations in physical process parameters.

Our simulation framework starts with the fresh device. At this point, devices are sampled from a statistical distribution, including variations in process and degradation parameters. DC simulations are used to calculate the electrical parameters. These circuit parameters are then used to update the circuit degradation models. Since this update results in a parametric change in the overall circuit, the bias conditions will change. Hence, it is necessary to periodically repeat the DC simulations and update the degradation circuit parameters.

The equivalent circuit model of a transistor with threshold voltage shift due to HCI and NBTI is shown in Fig. 1. The

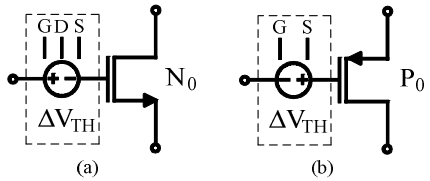


Fig. 1. Circuit-level models of (a) HCI and (b) NBTI threshold voltage shift

controlling node voltages are input variables of the aging model and connected to gate, drain, and source of the device, respectively. These node voltages are updated after each time step in order to obtain more accurate actual responses. In this work, the aging model is calibrated to 65nm technology. This aging model is used in circuit-level simulation with analytical computation of the threshold degradation. The performance of RF circuits with various levels of stress can be predicted using this model to obtain the degradation profiles.

IV. Proposed Methodology for Aging Estimation

In [20], the authors present a parametric method to detect counterfeit ICs using a one-class identifier, a support vector machine (SVM). Since the proposed method is based on a similar concept, it would be useful to review this existing work before explaining our methodology. SVM is a popular machine learning method for classification, regression, and other learning tasks [20][22]. In a one-class SVM, only the data from the target population is needed for training. After training, the machine classifies whether incoming samples belong to the target population. Using a one-class identifier eliminates the need to know the aging profiles. The goal in [20] is to identify whether a number of ICs received in one batch are fresh or aged. In this sense, rather than relying on individual classification, the authors propose to use a voting mechanism to determine the classification of the entire batch.

As mentioned earlier, aging mechanisms result in mostly bias dependent degradation for analog circuits, which makes it easier to obtain aging profiles for a large class of process and degradation parameters. Having this information, the classification can be made more accurate both for fresh and aged devices. This would enable us to test a few representative samples from the batch. Since each tested device contributes to the cost at the customer end, reducing the number of ICs that need to undergo aging detection can reduce the overall cost.

The degradation in circuit parameters follows highly non-linear behavior for distinct devices. Hence, analytical modeling of these profiles as a function of time is rather difficult. We take a novel approach to approximating the age of a given device. We consider the age as another parameter of the device under test (DUT). As such, a device instance sampled from a population is spawned as multiple devices, at each time checkpoint. Hence, for N time steps and K devices, we have $N \times K$ device instances to model. Each device instance has its performance parameters plus the age as an additional

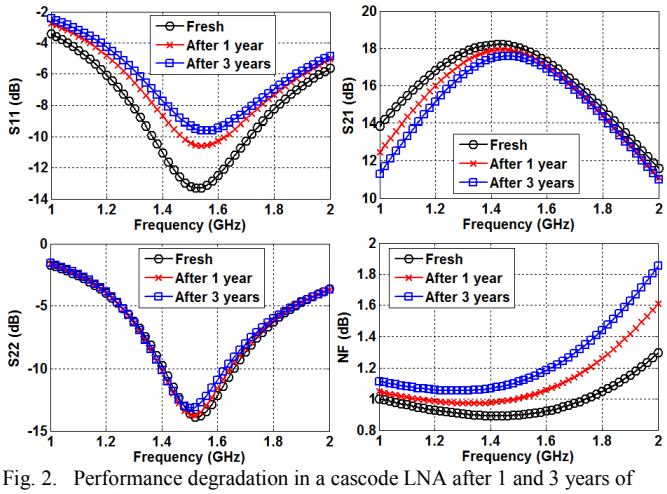


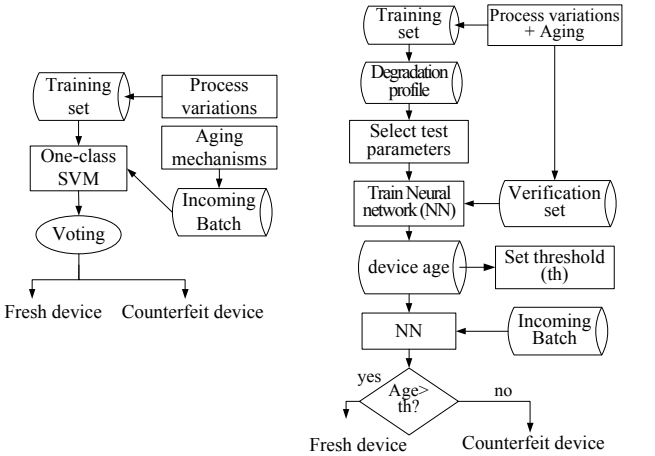
Fig. 2. Performance degradation in a cascode LNA after 1 and 3 years of operation at the room temperature

parameter. We use an Artificial Neural Network (ANN), which is a generic statistical modeling tool. ANNs have been used in analog/RF test for reducing the number of tested parameters, which is a similar problem [23][24].

Our objective is to identify a used or defective (counterfeit) device provided from suspicious supplier. When the transfer function of the network is determined using the training set (device measurements), the validation test set is applied to the network in order to estimate the target values (age) for ANN prediction. We establish a threshold criterion for identifying a fresh/counterfeit device by using the predicted age. This threshold provides us a tuning parameter to ensure that fresh devices are not misclassified since such misclassification may often lead to drastic measures. Hence, we have the flexibility to set the threshold with the goals of (a) identifying aged devices beyond a certain time (e.g. two years), and (b) identifying almost all fresh devices as such.

Fig. 2 shows an example of the simulation results for an LNA instance sampled from the process distribution for four performance parameters. As this figure shows, even after 1 year of nominal use (room temperature), there is noticeable degradation in three of the performance parameters, namely S11, S21, and noise figure (NF), whereas one performance parameter does not display much movement. Hence, it is beneficial to use the three affected parameters in the statistical model since the inclusion of S22 will result in more uncertainty in the results. Fig. 2 also shows that degradation is more severe in same frequency which may be different than the intended frequency of operation. Hence, measurement of these parameters can be conducted at different frequencies. We use a simple selection methodology to determine which parameters (and which frequencies) need to be included in the statistical model.

Fig. 3 (b) shows the flow of the proposed methodology. We start with a training set of devices. This training set can be obtained using aging simulations and/or accelerated aging studies. We use the degradation profiles from the training set to first select the tests to be included in the statistical model and to establish the statistical model. A number of samples are also reserved as verification set to establish the necessary age threshold to deem a device fresh or aged. Once the statistical model is established, incoming circuits can be re-characterized with respect to the selected measurements and the results can be used to predict the age. The predicted value is compared with the established threshold to decide if the individual device is fresh or counterfeit. Fig. 3 also compares the proposed methodology with the state of the art [20]. The major differences are (a) single device characterization (proposed) versus batch characterization ([20]), (b) using statistical information on fresh and aged devices (proposed) versus using information on only fresh devices ([20]), and (c) age prediction by treating age as a device parameter (proposed) versus classification only ([20]).



(a) SVM-based detection [20] (b) Proposed detection method using age as a parameter

Fig. 3. Flow of the proposed counterfeit detection method and comparison with existing work

V. RESULTS

The proposed classification test method is applied to a RF low-noise amplifier (LNA) and LC oscillator (OSC) circuits shown in Fig. 4. The time-varying threshold voltage shift is modeled as a dependent voltage source, as explained in Section III. This model is updated after each time step. Time steps are chosen uniformly for these experiments although they can be made adaptive with respect to perceived shifts in monitored parameters.

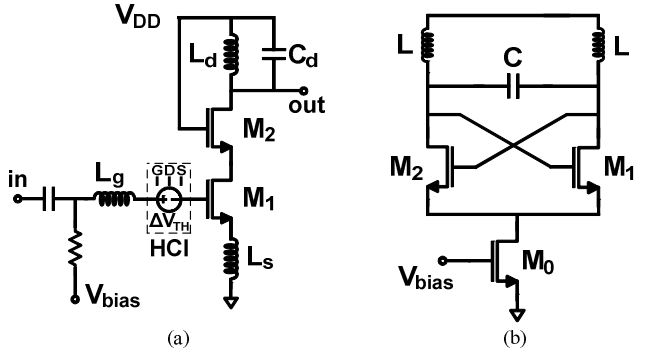
In order to generate the device population, Monte-Carlo (MC) simulation is used. Both die-to-die and within die variations in process parameters as well as degradation parameters are taken into account. For process parameters, we vary the length and threshold voltage (V_{th0}) of transistors according to Table I. Five parameters of the LNA, namely S-parameters, noise figure and DC current are evaluated. The important parameters for LC oscillator are phase noise at various frequency offsets from the center and output amplitude. 1000 Monte-Carlo devices of LNA and oscillator are generated and simulated for up to 3 years.

TABLE I. PROCESS VARIATION TABLE

	Length (3σ)	*V_{th0} (3σ)*	*R (3σ)*	*L (3σ)*	*C (3σ)*
DD	20 %	20 %	20 %	20 %	20 %
MM	2 %	2 %	2 %	2 %	2 %

The proposed method is applied to the two experimental circuits. One thousand device instances are generated using Monte-Carlo sampling. 900 of these instances are selected at 6 different aging points to from 0 to 36 months. The remaining 100 devices are used to evaluate the accuracy. In order to avoid the dependence of test quality on the training sample set, evaluation is performed several times and average classification rates are reported. Once an age threshold is selected to distinguish between fresh and aged devices, the classification rates at each time step can be calculated.

Based on the above-mentioned parameters, the classification rate for the LNA circuit using our proposed method is shown in Table II. 93% of fresh devices are correctly



(a) (b)

Fig. 4. Experimental RF Circuits: (a) Cascode LNA and (b) NMOS LC oscillator

TABLE II. CLASSIFICATION RATE FOR LNA/OSC WITH PROPOSED METHOD

Baseline			t_0	t_1	t_2(2y)	t_3	t_4	t_5
LNA	1m	New	**53**	0	0	0	0	0
		Used	47	**100**	**100**	**100**	**100**	**100**
	8m	New	**93**	36	6	1	0	0
		Used	7	**64**	**94**	**99**	**100**	**100**
OSC	1m	New	**16**	0	0	0	0	0
		Used	84	**100**	**100**	**100**	**100**	**100**
	9m	New	**92**	54	8	2	0	0
		Used	8	**46**	**92**	**98**	**100**	**100**

identified whereas 94% of devices aged by t_2 (two years) are correctly identified. Identification rates of devices at higher ages are nearly 100%. Table II also shows the identification rate for the LC oscillator circuit. We obtain 92% correct identification for fresh devices and 92% correct identification for devices aged at t_2 (two years). For devices aged 2.5 years or more, the correct identification rate is 100%. It is important to note that our proposed technique identifies individual devices randomly selected from an aged batch.

In order to compare the proposed technique with the one-class identifier proposed in [20], we have implemented the SVM based on the parameters described in [20]. As mentioned earlier, only fresh devices are used for the training process. Hence, the identical 900 devices are used for training the SVM. Again, the process is repeated 10 times and average identification rates are evaluated. Classification results of SVM classifier method for both LNA and LC oscillator are shown in Table III. In comparison to the results of the proposed technique, the one-class SVM cannot provide the desired accuracy for correctly classifying single devices, particularly for fresh devices. For both the LNA and the oscillator, the classification accuracy is around 50% for fresh devices. The authors in [20] hence suggested testing devices in batches and relying on a voting mechanism.

TABLE III. CLASSIFICATION RATE USING ONE-CLASS SVM CLASSIFIER

RF circuits		t_0	t_1	t_2 (2y)	t_3	t_4	t_5
LNA	New	**50**	23	12	2	0	0
	Used	50	**76**	**88**	**98**	**100**	**100**
OSC	New	**47**	38	33	30	24	25
	Used	53	**62**	**67**	**70**	**76**	**75**

VI. CONCLUSION

In this paper, we present a technique for successful identification of used (counterfeit) devices among existing unknown devices by employing a neural network model. The proposed method requires relevant information such as aging degradation profiles of the devices including process variations and aging mechanisms. This information can be obtained using either accelerated aging data or reliability simulations. Our simulation framework for aging is based on experimentally proven reliability models and a novel circuit/device level hybrid simulation methodology that can take process variations as well as variations and mismatches in aging degradation parameters. We present a novel modeling technique where the device age becomes a parameter and map the performance parameters measured from the device to its age. We set an age threshold to classify devices as fresh or aged. This aging threshold can be adjusted with respect to the goals. Our goals have been to identify most of fresh devices as such and most of used devices (beyond two years) as aged. Experimental results using an LNA circuit and an LC oscillator circuit and based on simulation data show that the proposed technique can achieve identification accuracy of above 92% for both fresh and aged devices. The identification results are compared with those of the one-class SVM classifier method [20] for single device identification. The proposed method achieves better classification accuracy for single devices both for fresh and aged devices. This reduces the burden of re-characterization since it can be done for a small number of samples out of a batch of received devices.

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