An Embedded Offset and Gain Instrument for OpAmp IPs

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***Abstract*—Analog and mixed-signal IPs are increasingly required to use digital fabrication technologies and are deeply embedded into system-on-chips (SoC). These developments append more requirements and challenges on analog testing methodologies. Traditional analog testing methods suffer from less accessibility and control with regard to these embedded analog circuits in SoCs. As an alternative, an embedded instrument for analog OpAmp IP tests is proposed in this paper. It can provide the exact gain and offset values of OpAmps instead of only pass/fail result. What's more, it is an non-invasive monitor and can work online without isolating the DUT Opamp from its surrounding feedback networks. Nor does it require accurate test stimulations. In addition, the monitor can remove its own offsets without additional complex self-calibration circuits. All self-calibrations are completed in the digital domain after each measurement in real time. Therefore it is also suitable for aging-sensitive applications, in which the monitor may suffer from aging mechanisms and has additional offset drifts as well. The monitor measurement range for offset is from 0.2mV to 70mV, and for gain it is from 0dB to 40dB. The error for offset measurements can be 10% of the measurement value with plus/minus 0.1mV, and -2.5dB for gain measurements.**

I. Introduction

Analog IPs are usually tested with automated test equipments (ATE), which are complicated and expensive instruments. The analog IP under test needs to be isolated from other IPs, and must be fully accessible to the ATE. However, in the case of IPs which deeply embedded in SoCs, it is difficult to access them due to the limited number of pins in the package. Even with sufficient pins, the routing of analog signals are easily polluted by the surrounding digital IPs, and isolating an IP is not always possible in SoCs as well.

An existing solution for those test requirements mentioned above is using the embedded-instrument (EI) concept [1]. They provide on-chip test IPs which are connected through standard buses and protocols (IEEE P1687) [1]. These on-chip EIs are supposed to test basic physical parameters like voltages, currents, temperatures, as well as performance parameters of analog/mixed-signal IPs. The embedded instruments are primarily used during function tests. Now they are there and can be used as aging monitors during SoCs life time as well. The aging effects in the nano-meter CMOS technologies (<90nm), like negative bias temperature instability (NBTI), could influence gains and offsets of analog OpAmps [2]. These influences need to be monitored regularly during the life-time, which are beyond the capability of traditional ATEs.

In this paper, an embedded offset and gain monitor for OpAmp IPs is proposed. It can test the gain and offset of the OpAmp IP online without isolating it from surrounding feedback networks as well as connected IPs. No accurate stimulation sources are required either. It provides a self-calibration method to remove the resident offsets as well as aging-induced offsets inside the monitor. The paper is organized as follows. Section II will explain the new offset and gain monitor theory as well as self-calibration method. Section III will show the designed EI in system level. Section IV describes the circuit simulation results. The conclusions are provided in Section V.

II. Offset Gain Monitor And Self-Calibrations

The exact offset value of an OpAmp IP can be measured by unit-gain feedback-loop method [3] or calibration source methods [4]. These methods are either configuring the OpAmp into a unit-gain feedback system or applying extra calibration sources to the OpAmp and comparing its output. They are both invasive and require isolating the OpAmp from surrounding feedback networks. They need to add switches into the original signal paths, which is not preferred by designers considering the noise and mismatch influence. In addition, they will either need an accurate ADC or an accurate stimulation source as the key element, which increases both the complexity and difficulty of the EI design. Self-calibrations to keep the accuracy of the ADC or the stimulation source add an extra problem as well. To overcome the above problems, a new offset monitor theory is proposed.

A. The New Offset Monitor Theory

The basic idea is simple. The output of the OpAmp device-under-test (DUT) has an offset. If the same output without any offset can be generated, the offset voltage can be measured by comparing these two output signals. This ideal output signal seems difficult to generate. However, with the block diagram shown in Fig. 1, the goal is achieved successfully. Fig. 1 shows the DUT OpAmp with an input offset voltage V_{off}. The output of the DUT is compared with a signal from a gain-controlled amplifier. This amplifier has the same input as the DUT. Its gain is controlled by both the digital programmed number K and the compared result V_c. The analog multiplier in Fig. 1 is introduced to realize such gain control mechanism.

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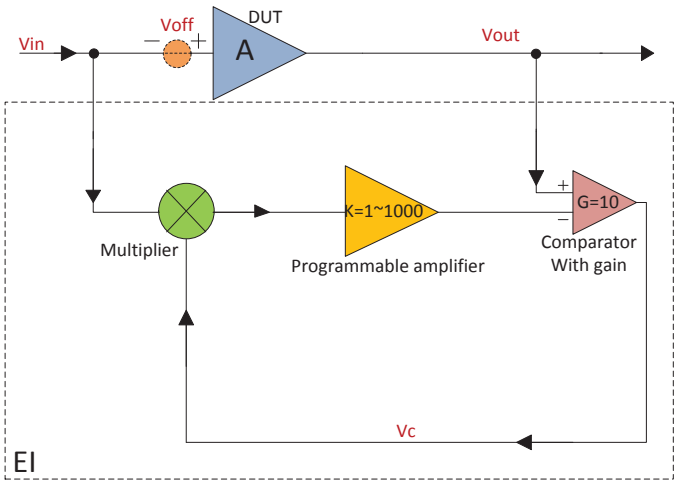

Fig. 1. Block diagram for the new monitor theory.

From Fig. 1, V_c can be expressed as (1).

$$V_c = \frac{(V_{in} + V_{off}) \cdot AG}{1 + V_{in} \cdot KG} \tag{1}$$

In (1), V_{in} is the original input signal of the DUT OpAmp. It means that the DUT can be online when doing measurements. V_{off} is the DUT input offset voltage, which is to be measured. A is the gain of the DUT. G and K are gains of the comparison gain stage and the digitally programmable amplifier in the monitor respectively. With different program settings, K can be changed from 1 to 1000. V_c is the output signal from the comparison gain stage. All these symbols are shown in Fig. 1 on their respective locations.

As shown by (1), V_c depends on the input signal V_{in} in most cases of K settings. However, there is a special K value for which V_c is independent on the DUT input signal V_{in}. This special K value can be expressed in (2).

$$K_{spc} = \frac{1}{V_{off} \cdot G} \tag{2}$$

Substitute (2) into (1). V_c in this situation can be calculated as:

$$V_c|_{K=K_{spc}} = V_{off} \cdot A \cdot G \tag{3}$$

Lets reexamine the monitor shown in Fig. 1 and the expression for V_c in (1). Basically, there is a feedback loop in the monitor which includes the multiplier, the programmable amplifier K and the comparator G. The input signal V_{in} not only controls the loop gain, but also determines whether it is a negative feedback or a positive feedback. If the loop gain $V_{in} \cdot K \cdot G$ approaches -1, V_c will be driven to positive infinity or negative infinity, depending on which direction the loop gain approaches -1. For example, if K is larger than K_{spc}, it can be expressed as (4).

$$K = \frac{1}{(V_{off} - \triangle)\, G} \tag{4}$$

In (4), $\triangle$ is a positive value which is smaller than V_{off} to make sure that the sign of K is not changed. Substitution of (4) into (1) results in:

$$V_C = \frac{(V_{in} + V_{off}) \cdot AG \cdot (V_{off} - \triangle)}{V_{in} + V_{off} - \triangle} \tag{5}$$

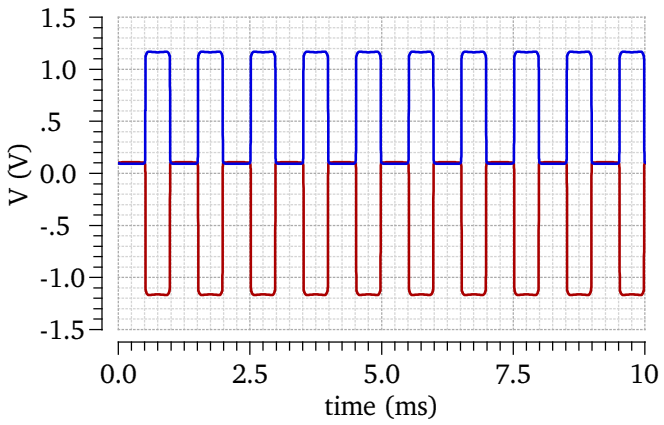

Fig. 2. The simulation for V_c vs. time under two adjacent programmable K values.

As the denominator of (5) approaches zero, the numerator is still positive. Hence V_c will be driven to positive infinite. Following the same reasoning, it can be concluded that V_c will be driven to negative infinite if K is smaller than K_{spc}. It mean that V_c will change dramatically when the programmable K value is scanned across the K_{spc}. Fig. 2 shows this dramatic change in V_c for two adjacent K programmable values, between which the K_{spc} value shown in (2) occurs. It shows that for all K values larger than the K_{spc}, V_c reaches the top rail (the blue line reach $1.2V$). While for all K values smaller than the K_{spc}, V_c reaches the bottom rail (the red line reach $-1.2V$ in a full differential system). Now one can find the K_{spc} value with a simple comparator as will be shown in Section III. Moreover, it makes the quick binary searching possible as well because the V_c result contains the information whether the current K is larger or smaller than the K_{spc}. Finally, to obtain the above mentioned dramatic change, the input voltage V_{in} should have an AC component and approach V_{off} during its variations. In other words, the input signal of the DUT OpAmp should have an AC component and the amplitude of the AC component should be larger than its offset. Fortunately, this is the normal case in both functional tests and lifetime operations of OpAmps.

B. Self-Calibration for Resident Offsets

Actually, every component inside the monitor has resident offsets. Moreover, aging effect like NBTI will introduce extra offsets during the lifetime. These offsets can have such a significant influence which can turn the measurement result totally useless. Using offset minimization technique for each component, such as auto-zero or chopper-stabilization, is possible but too expensive. The same holds for adopting on-chip accurate calibration sources. Here, a simple technique is proposed to accomplish the self-calibration in the digital domain.

Fig. 3 shows the monitor with resident offsets in each component. These offsets can be resident offsets from non-perfect matching or aging induced offsets from NBTI. V_{o1} and V_{o3} indicate offsets at two input ports of the multiplier. V_{o4} stands for the offset at the output of the multiplier in combination with the offset of the programmable amplifier. The offset of the comparator gain stage is shown as V_{o2}. Two

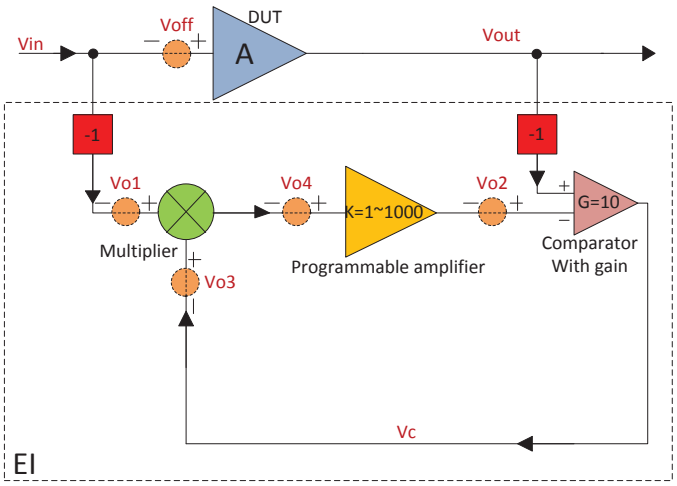

Fig. 3. Self-calibration for resident offsets inside the monitor.

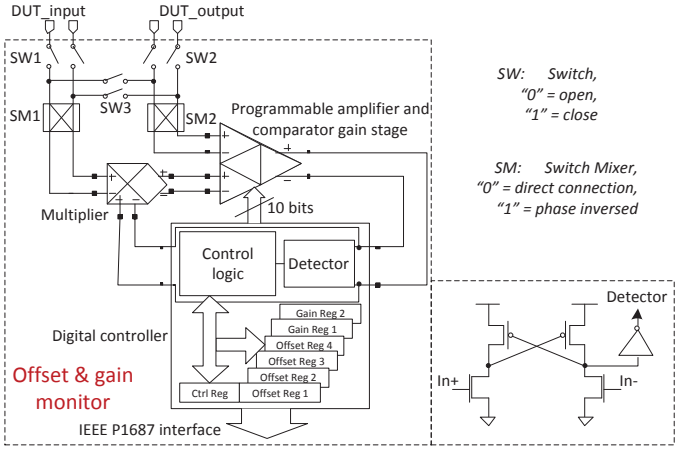

Fig. 4. System level plot of the designed embedded offset and gain instrument as well as the detector used in the EI.

"-1" red blocks are inserted into the two inputs paths of the monitor, which indicate phase inversion (multiplying by -1). They are used in the self-calibration procedure and can be easily implemented by switching the sequence of two signal lines in a full differential system.

If both V_{in} and V_{out} are directly injected into the monitor without phase inversion, the expression for K_{spc} in (2), which takes resident offsets into account, can be written as (6).

$$K_{00} = \frac{1}{G \cdot \left(V_{off} - V_{o1} - \frac{V_{o2}}{A} + \frac{V_{o3}}{AG} - \frac{V_{o4}}{A} K_{00}\right)} \tag{6}$$

In (6), K_{00} means the specific K_{spc} value with both V_{in} and V_{out} are not inverted. If both V_{in} and V_{out} are inverted, the expression can be found as (7), in which K_{11} means the specific K_{spc} value with both V_{in} and V_{out} are inverted.

$$K_{11} = \frac{1}{G \cdot \left(-V_{off} - V_{o1} - \frac{V_{o2}}{A} + \frac{V_{o3}}{AG} - \frac{V_{o4}}{A} K_{11}\right)} \tag{7}$$

In fact, (6) and (7) are both second order equations of K. Each of them will have two solutions. If these solutions can be written as K_{00a}, K_{00b}, K_{11a} and K_{11b}, their relationships with DUT offset V_{off} and gain A can be expressed in (8) and (9).

$$A = V_{o4} G \cdot K_{00a} K_{00b} = V_{o4} G \cdot K_{11a} K_{11b} \tag{8}$$

$$V_{off} = \left(\frac{1}{K_{00a}} + \frac{1}{K_{00b}} - \frac{1}{K_{11a}} - \frac{1}{K_{11b}}\right) \frac{1}{2G} \tag{9}$$

In real circuit, only when V_{o4} is a negative value, the above four solutions K_{00a}, K_{00b}, K_{11a} and K_{11b} are all real number and can be found by scanning the programable K values as described in Section II-A. As a result, the DUT offset value V_{off} can be obtained by (9).

When V_{o4} is a positive value, those four solutions could be complex numbers and can not be found by scanning the programable K values. Extra combinations for phase inversions are required, such as K_{01}, which means only V_{out} is inverted, and K_{10}, which means only V_{in} is inverted. Similar calculations can be made for K_{01} and K_{10}. The DUT offset V_{off} can be obtained by the four solutions for K_{01} and K_{10} as well.

C. Gain Monitor Theory

The gain of the DUT, A, is expressed in (8). The only problem to calculate A from (8) is that there is an extra unknown variable V_{o4}. In order to calculate A, we need another new equation to get V_{o4} first. Fortunately, it is not difficult to find such a equation. Just bypass the DUT and connect the second input path of the monitor, which used to be connected with V_{out}, to the same V_{in} as well. Now it is known for sure that the gain of the DUT is equal to one, and (10) can be obtained.

$$V_{o4} = \frac{1}{G \cdot K_{xxa} K_{xxb}} \tag{10}$$

In (10), K_{xxa} and K_{xxb} means the solutions for K equations under the bypassed DUT configuration. The gain A of the DUT can be calculated by substitute (10) into (8). The final result for A is shown in (11).

$$A = \frac{K_{00a} K_{00b}}{K_{xxa} K_{xxb}} \tag{11}$$

III. System Configuration and Design

In order to verify the proposed theory, a testing EI is designed in TSMC 65nm low-power (LP) digital CMOS technology. At system level, the selection of G together with the programmable range of K determine the offset/gain measurement range and resolution. In this design, G is fixed at 10, and K is programmed as in (12).

$$K = \frac{1000}{\beta}, \quad \beta = 1 \sim 1000 \quad \text{with stepsize} = 1 \tag{12}$$

With these configurations, the theoretical detectable offset range is from $100\mu V$ to $100mV$ with a step-size of $100\mu V$. The detectable gain range is from $0dB$ to $60dB$. The EI architecture is shown in Fig. 4. It is a full differential system. The programmable amplifier is combined with the comparison gain stage. There are 10 bits available to program β from 1 to 1000. The detection circuit for V_c is also depicted in Fig. 4. It is a voltage-shifter circuit which is used to determine the "strong" 1 and 0. The "strong" means one input is much larger or much smaller than the other input, which corresponds

TABLE I. MONITOR SIMULATION RESULTS

Random Generated Performance						Monitor Results	
V_{off} (mV)	V_{o1} (mV)	V_{o2} (mV)	V_{o3} (mV)	V_{o4} (mV)	Gain (dB)	V_{off} (mV)	Gain (dB)
1	0	0	0	0	34	1.05	NA
1	0.5	-1	10	0.1	34	1.17	32.8
10	-8	4	25	-2	12	11.05	11
0.2	0.5	-1	2	-0.4	40	0.20	37.5
70	25	18	-20	10	0	64.8	-1.8
					Maximum Error:	$10\% \pm 0.1$mV	-2.5dB

to the plot shown in Fig. 2. The control logic control switches $SW1$, $SW2$, and $SW3$, as well as switch-mixers $SM1$ and $SM2$. These are the same kind of switch-mixers employed in chopper-stabilization circuits [5]. Based on the signal detector and the 10-bits configurations of the programmable amplifier, the digital controller logic can find six results and write into registers as from "Offset Reg 1" to "Gain Reg 2". These registers contain four solutions for the offset measurement, such as K_{00a}, K_{00b}, K_{11a} and K_{11b}, and two solutions for the gain measurement, K_{xxa} and K_{xxb}. With the help of (9) and (11), the self-calibrated offset and gain results can be calculated using the CPU inside the SoC. The control register "Ctrl Reg" is used to communicate with the digital world. It controls the monitor like "start", "reset", "enable", "error" and "ready". All these registers are communicating via the IEEE P1687 interface.

The four-quadrant transconductance multiplier is based on FVF technology [6]. Actually, the multiplier is not a rail-to-rail input circuit. Its maximum input range is from 0 to 0.6V. In this EI design, the rail-to-rail capability is realized by dividing both inputs with two and finally amplify the multiplication result by four. The digital programmable amplifier and the comparator gain stage can be combined into an instrumentation-amplifier like system. The 10-bits digital programmability is realized by two "R-2R" resistor ladders. The comparator gain stage is realized in a subtractive circuit format together with a gain G. In order to reach a 1000 times close-loop amplification K, the open-loop gain of the OpAmps should be at least $80dB$. In 65nm LP digital CMOS technology, the intrinsic gain of a transistor is only $20dB$. So a $80dB$ gain will require 4 gain stages or gain boosting stages for realization. In addition, transistors stack between supply and ground cannot exceed one V_{gs} plus two V_{ds} for $1.2V$ power supply. The OpAmp design applies a constant-gm controlled rail-to-rail input stage, a folding mesh summary stage and a class-AB rail-to-rail output stage [7]. A gain boosting technique is used to further increase the gain. Simulation results show the gains of the OpAmp above 80dB for all input common mode voltages.

IV. SIMULATION RESULTS

In order to validate the self-calibration technique, five random generated gain and offsets combinations were applied. The results are shown in Table I. For offset measurements, there is an additive error which is less than $0.1mV$, and a multiplying error which is around 10% of the measured result. For gain measurements, the error is about $-2.5dB$. The theoretical detectable range is $100\mu V \sim 100mV$ for the offset, and $0 \sim 60dB$ for the gain. However, in this test circuit, the maximum detectable gain is about $40dB$ and the maximum detectable offset is $70mV$. If the gain and offset are too large, the theoretical signal value of V_c will be above the $1.2V$ supply limit and causes the monitor to saturate. It may be possible to solve this problem by making G programmable between 1 and 10 as well instead of fixing at 10. The minimum offset value $100\mu V$ is also not always reachable. It is because the V_c sometimes changes only when β is smaller than 1, which is not reachable for the monitor at such a small offset. So the actual range for the offset is $200\mu V \sim 70mV$, and $0 \sim 40dB$ for the gain. The testing time for the EI is dependent on the frequency of the input signal. The maximum testing time could be 240 times the input signal period. For example, the maximum possible input signal frequency is $30KHz$ due to the EI bandwidth limitation. In this input frequency, the testing time of the EI is $8ms$. The total current consumption is around $3mA$ without optimization for low power operation.

V. CONCLUSION

An embedded offset and gain instrument for OpAmp IPs has been designed based on a new measurement theory. The monitor does not need to isolate DUT OpAmp IPs from its connected feedback networks and other IPs. Neither does it need accurate stimulation sources. This EI can self-calibrate its resident offsets in the digital domain after each measurement. The monitor is designed in TSMC 65nm LP digital CMOS process and provides an IEEE P1687 interface. It can be shared with other analog OpAmp IPs to reduce the cost and shut down in idle situation to save power. The detection range is $200\mu V \sim 70mV$ for the offset and $0dB \sim 40dB$ for the gain. The simulation results show that the error for offset measurements can be 10% of the measurement value plus/minus $0.1mV$. For gain measurements, the error is about $-2.5dB$. The testing time of the EI can be $8ms$ and the total current consumption is around $3mA$.

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