

Modeling of an Analog Recording System Design for ECoG and AP Signals

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Abstract—The recording of neural activities has turned out to be a promising approach to understand the basic function of specific brain parts like the visual or motor cortex. However, the development and design of advanced neural recording systems is very challenging since the number of parallel measurement channels increases continuously. Beside the analog recording channels digital preprocessing becomes mandatory to handle the corresponding amount of data and to adapt this data to the available transmission bandwidth. In this paper we present the design as well as the behavioral modeling of an analog recording front-end. Simulation and measurement results demonstrate the performances of the system for recording neural signals. Since simulation of this analog front-end is very time consuming but essential for large fully-integrated designs, a mixed-signal model approach is introduced that enables a significant simulation acceleration of integrated and external analog front-ends. The simulation can be accelerated by a factor of up to 22.2 for a single front-end. The proposed system has been fabricated in a 0.35 μm CMOS technology and performances have been measured. This demonstrates that the behavioral model is compatible to the transistor level design. A neural spike detector shows the transient performance of the modeled design on real input stimuli.

Index Terms—Neural Measurement System, Modeling, HDL, ECoG, AP, Mixed-Signal

I. INTRODUCTION

The measurement of electrocorticographic (ECoG) signals and Action Potentials (APs) has enabled a wide range of advances in the study of neural activities. The simultaneous observation of multiple measurement channels is an important method to investigate the operation of the cortex. The visual and motor cortex have been monitored to understand the basic function of movement and visual perceptions [1] [2]. Arrays of more than 100 electrodes are desirable to receive a sufficient resolution for the analysis of neural activities. Nevertheless, this is a small number compared to the amount of neural sources within the brain. Therefore the demand for recording systems with more and more parallel recording channels increases continuously. However, limitations exist due to rising complexity of the design, the dimension of the electrode array and the technical capabilities of transmitting the monitored data out of the skull [3].

In recent years many research institutes have developed components for the use in neural measurement systems. In addition to specific low-noise analog amplifier ASICs [4] [5], micromechanical coils and transmitters for energy transmission [6] [7] as well as wireless transmitters [8] have been

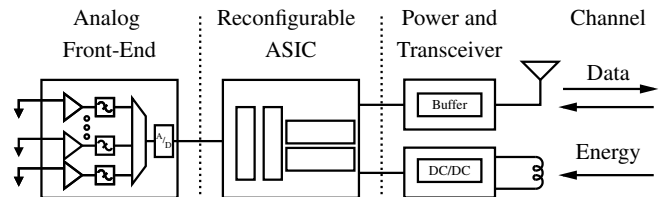


Fig. 1. Schematic overview of a neural measurement system.

presented. All these devices deal with the same problem of low energy consumption, minimal heat dissipation and small die size. Beside these single ASICs also specialized systems for neural recording have been proposed. In [9] and [8], for example, head-mounted systems are presented with focus on long distance wireless transmission and free movement of test animals. Fully implantable systems are shown in [10] [11]. The systems vary in the use of commercial components and integration density. The use of commercial ASICs as building blocks for a complete system allows the integration of advanced and tested components in a whole neural measurement system, in contrast the integration of components within one ASIC reduces die size and the dimension of the final system.

However, a fully-integrated system is very challenging in terms of mixed-signal behavior and the accurate modeling of multiple independent measurement channels. Besides the parallel analog recording channels, a common digital preprocessing unit is mandatory to adapt the amount of acquired data to the transmission bandwidth of the transceiver [12]. The simulation of multiple independent analog measurement channel within the digital design is a time consuming and complex task. Nevertheless, it is necessary to test and verify the functionality of the mixed-signal system. The behavioral modeling of analog channels of a neural recording system design is presented in this paper. The approach leads to an acceleration of the simulation time without losing a significant degree of system performance precision.

The paper is structured as follows. Section II describes the proposed analog design and presents relevant simulation results for the behavioral modeling of the analog components. The modeling and mixed-signal simulation is presented in section III. Measurement of a fabricated ASIC and mixed-signal simulation results are discussed in section IV.

TABLE I
CHARACTERISTICS OF SIGNAL TYPES FOR THE NMS MEASUREMENT.

	Bandwidth	Amplitude	Gain
Spike	200 Hz- 10 kHz	50 μ V - 500 μ V	76 dB
LFP	1 Hz - 300 Hz	< 5 mV	56 dB

II. NEURAL RECORDING SYSTEM

The proposed and investigated neural measurement system (NMS) is basically developed for the recording of up to 128 parallel connected electrodes. The NMS consists of integrated analog recording channels and of biomedical external components (Fig. 1). Therefore, an important aspect of the design is the implementation and simulation of interfaces to external as well as the integration of internal components.

Up to eight analog front-ends can be used in the system, each acquiring data from a maximum of 16 electrodes. Depending on the system configuration the analog recording channels are able to measure various neural signal types. Especially the study of local field potentials (LFPs) and APs is of great interests (Table I) enabling novel understandings of cortical operation. Based on the number of activated measurement channels, the raw data rate alters and has to be reduced to the transmission rate of the transceiver. To handle the configuration of the analog channels and to limit the data bandwidth a reconfigurable digital ASIC was developed [13] that enables the selection of dedicated measurement channels, the limitation of the sampling frequency and the reduction of the digital resolution.

It is important to point out the basic operation of the reconfigurable digital design to explain the need for a behavioral model for a precise and accelerated mixed-signal simulation. The modeling of analog behavior allows the adjustment of each analog channel and helps the designer to evaluate the potential possibilities of the design for selected neural signals. By this it is possible to investigate and simulate the amount of detected spikes for certain settings of the system (e.g. low digital resolution, high sampling frequency).

A. Analog Front-End

The proposed analog front-end, which is described in this paper, consists of a maximum of 16 parallel measurement channels for the recording of neural signals, an analog multiplexer for the time-multiplexing of parallel signals and an ADC for data conversion. Biasing and digital control circuits are used to set the operation points of the proposed circuits (Fig. 2). The first stage of each neural measurement channel is composed of a capacitively coupled low-noise amplifier (LNA) [4] and an integrated highpass filter. The capacitive coupling enables the highpass filtering of neural signals and the simultaneous suppression of DC components. An additional highpass filter is employed to limit the higher cut-off frequencies of the amplified signal in dependency of the measured signal type. As the amplitude of the first stage output signal is still too small, a second stage variable gain amplifier (VGA) is used.

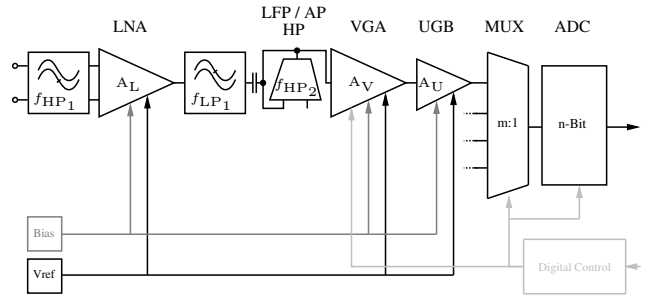


Fig. 2. Schematic of the analog neural front-end.

The gain can be adjusted to the maximum expected peak-to-peak voltage of APs and ECoG signals. A third amplifier is used, in order to lower the gain-bandwidth (GBW) for a low-power second stage amplifier and to charge the sample & hold capacity of the ADC. A unity-gain buffer (UGB) with rail-to-rail in- and output is used to fulfill this requirement.

B. Low-Noise-Amplifier

The most relevant analog function block of the neural measurement system is the first amplification stage, which is directly connected with the electrodes. Based on the requirements for the amplification of very small signal amplitudes, a low-noise amplifier is essential to minimize the noise that is added to the ambient noise of the measurement electrodes. The gain has to be sufficient to minimize the influence of second and third stage noise to the input equivalent noise of the whole measurement channel. Coupling capacitors are used at the input, in order to suppress DC components of the electrodes and to avoid the saturation of the amplifier. Adding a capacitive feedback, the gain can be adjusted, too. Various amplifier topologies that fulfill these requirements have been presented in literature [3] [4]. Besides single-ended topologies [5] fully-differential approaches also exist.

In this paper we focus on a low-noise telescopic cascode opamp that is presented by Borghi et al. [14], having a relatively small energy consumption and a good compatibility to the proposed technology. The gain of the first amplifier is set constant to $A_{LNA} = 36.4$ dB.

C. LFP / AP Highpass

A continuous-time highpass filter is used, as the lower cut-off frequency of the amplified signal has to be adapted to the need of APs and ECoG signals. A gm-C filter composed of an operational transconductance amplifier and capacitor is proposed for this application. The filter allows tuning of the lower-cut off frequency and has a low energy consumption. For the gm-C filter a wide linear-range transconductance amplifier is used to enhance the linear range of $U_{lin} = \pm 66 \cdot 2.5$ mV = ± 165 mV [15]. Two techniques are implemented to increase the linear range to this limits: source degeneration and bump linearization (Fig. 3). Source degeneration is a known-technique and converts the transistor current through a diode into a voltage. This voltage can be fed back to the source and thus decreases the corresponding current. The second

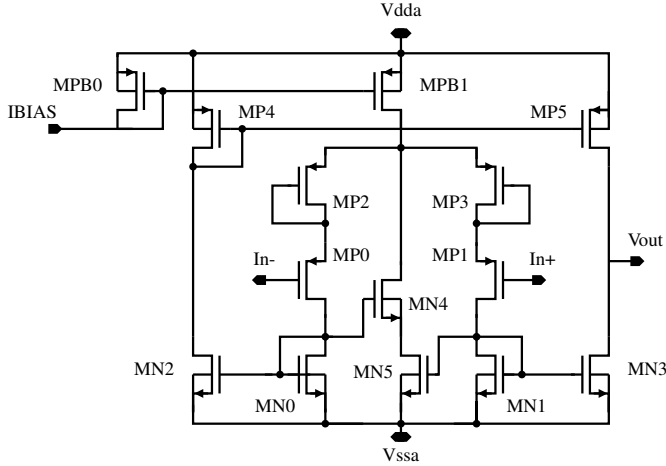


Fig. 3. Schematic of the transconductance amplifier for the proposed gm-C filter.

technique is bump-linearization that extends the linear range of a subthreshold differential pair. A central arm (MN4 / MN5) is introduced, besides the two outer ones of the differential pair. If the differential voltage rises or falls, one of these transistors shuts down and the current through the transistors decreases. This reduces the flat zone near the origin and therefore enables an extension of the linear range.

For the capacitor a value of $C_{HP} = 7$ pF has been chosen. The conductance G_{HP} of the amplifier can be adjusted by the bias current I_{BIAS} and is responsible for the lower cut-off frequency of the filter. Depending on the desired frequency, a current of 1 pA up to 10 nA is necessary. An adjustable nanoampere bias current source is required for this application. The range of the lower cut-off frequency can be set from 100 mHz to 400 Hz.

D. Variable Gain Amplifier

The function of the second stage VGA is further amplification of the bandpass-filtered and amplified neural signal. This is necessary to exploit the whole dynamic range of the following ADC. Thus the amplification can be adjusted to $A_{VGA1} = 20$ dB and $A_{VGA2} = 40$ dB. The variable gain is required to adapt the overall amplification to the requirements of the neural signal. In order to solve the problem of an unstable OTA, due to the varying capacitive load, a dual amplifier approach is used. The amplification is achieved by a simple two-stage OTA followed by a class AB buffer. A capacitive feedback is applied to achieve the desired amplification (Fig. 4). The capacitive feedback decreases the resistive load of the OTA and reduces the energy consumption of the amplifier. A select-transistor (MSel) is used to set up the amplification by the reconfigurable digital part.

A Miller-compensated two-stage-OTA is used for the VGA enabling a rail-to-rail output of the amplified signal. This is necessary as the overall amplification of the neural channel covers nearly the whole operating voltage. In [14] a UGB has

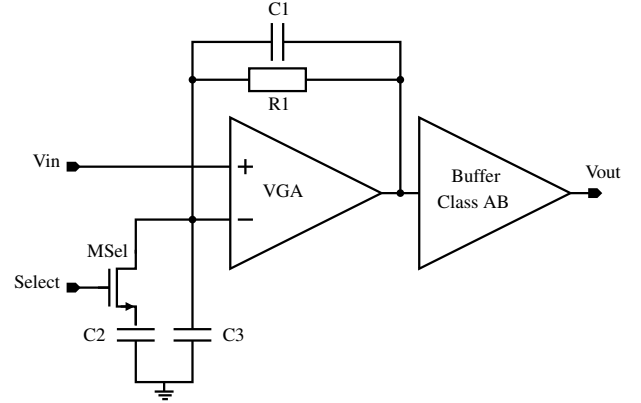


Fig. 4. Schematic of the variable second stage amplification.

TABLE II
SIMULATED PERFORMANCES FOR THE AMPLIFIER COMPONENTS OF A NEURAL MEASUREMENT CHANNEL (0.35 μ m CMOS).

		LNA	VGA	UGB
Gain	[dB]	36.31	20.1 / 40.6	1
Bandwidth	[Hz]	15.5 k	159 k / 14.0 k	1.59 M
Lower cut-off	[Hz]	36 m	\times	\times
Higher cut-off	[Hz]	15.5 k	159 k / 15.9 k	1.59 M
Noise	[μ Vrms]	6.08	\times	\times
CMRR	[dB]	64.54	> 120	\times
PSRR	[dB]	> 75.5	> 40	60
Supply voltage	[V]	± 1.65	± 1.65	± 1.65
Supply current	[A]	4 μ	2.3 μ	17.9 μ

been proposed for the buffering of the output signal, however the proposed architecture is not fully rail-to-rail compatible. An enhanced design overcomes this problem and allows rail-to-rail in- and output based on [16]. The UGB consists of two single buffers that are complementary to each other. The individual in- and output range is added to a common one with rail-to-rail characteristics. Both single buffers are using flipped-voltage followers with differential input.

E. Neural-Measurement Channel

The proposed functional blocks were composed to a neural measurement channel, capable of recording neural signals. A MUX time-multiplexes the output data and data conversion is done by a 10 bit SAR-ADC. Relevant performance parameters of the neural measurement channel have been simulated and are summarized in Table II. For the measurement of ECoG signals, especially information in lower frequencies is of interest. Therefore, the highpass has to be adjusted to very low-frequencies and the amplification of the VGA has to be set to A_{VGA1} . Since the higher frequency range is of less interest, the sampling of the ADC can be set to a few hundred Hertz and therefore allows the operation of more channels, due to the reduced amount of data. The design has been realized in a 0.35 μ m CMOS technology.

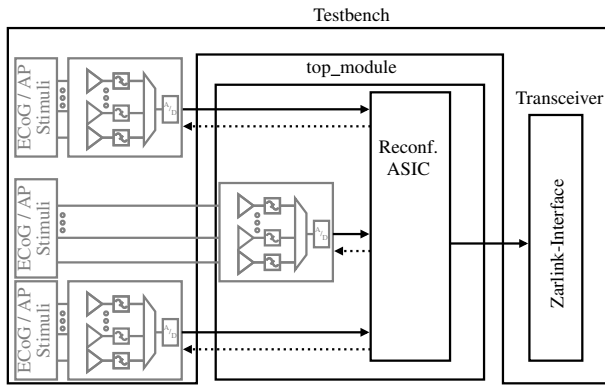


Fig. 5. Modeling of the analog frontend for NMS simulation.

III. ANALOG FRONT-END MODELING

Behavioral modeling of the analog front-end is a valid approach to accelerate the simulation time of the mixed-signal top level simulation. This task is especially important since SPICE simulation of complex analog components is a very time consuming task [17]. The proposed neural measurement system consists not only of analog components, but also of digital parts, making a mixed-signal simulation necessary to investigate the behavior of the overall system. In this paper we focus on the modeling of a modular analog front-end that can be used inside the testbench and the ASIC top-module. The reuse of the front-end is important, because not all analog front-ends have to be integrated in the ASIC and also external analog front-ends might be used (Fig. 5). In addition to the analog parts and the reconfigurable digital unit, a wireless transceiver model and neural input stimuli are used for the testbench setup. The input stimuli (LFPs and APs) are recorded from the visual cortex of a rhesus monkey.

A. Analog Channel Modeling

The modeling of a single measurement channel, based on the structure of the proposed analog front-end above, has been investigated in a first step. Verilog-A has been chosen for the analog modeling. This allows a suitable combination of analog and digital hardware description. Verilog-A enables the simple description of analog behavior and connect modules are used for the combination of digital and analog domain within common simulation environments. The most relevant properties have been modeled, based on the simulated performance of the single components (Tab. II). Therefore simplified equations describing the function of the complex transistor level designs have been implemented. Since the transistor dimensions of the proposed components are defined according to section II, all the performance parameters are fixed. Other approaches like response surface models (RSM) are possible to adapt the performances of the models to operating parameters and transistor parameters. For simplification the supply voltage of the system is fixed to $V_{DD} = 3.3$ V. This allows to focus the modeling on small signal parameters that can be obtained

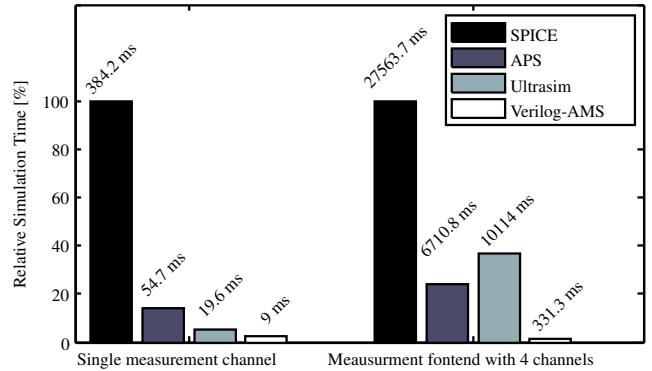


Fig. 6. Simulation time of transistor level design and model approach.

by an ac analysis (bandwidth, gain and cut-off frequencies). Implementation of noise is optionally achieved by the use of a noise table that represents the noise power over the corresponding frequencies.

The analog components have been modeled separately and the parameters have been set according to the simulation results. The cut-off frequency of the highpass-filter can be shifted by an input bias-current and the amplification of the VGA (A_{VGA1} or A_{VGA2}) is controlled by a digital input signal. In addition to the proposed analog components an analog multiplexer and an ADC has been modeled to arrange a complete analog front-end. In addition to the transistor level ADC, the resolution of the behavioral model can be adjusted.

B. Model Simulation

A mixed-signal simulation has been performed to determine the simulation time of the proposed behavioral model implementation and to calculate the improvements in acceleration. The simulation is set-up using the Cadence environment. A transient simulation time of about one second has been set-up, containing enough information to test the settings of the analog channels and to validate the recorded signals. First of all a single analog channel has been investigated using SPICE, Accelerated Parallel Simulator (APS) and UltraSim for the netlist design. The equations for the behavioral models have also been simulated and an average simulation time has been calculated (Fig. 6). The SPICE simulation takes $t_{SPICE} = 384,2$ ms for this setup, whereas the analog model only need $t_{AMS} = 9$ ms. This is a significant acceleration in speed, especially since only a single channel is simulated and components like ADC and Mux are not integrated. UltraSim and APS are advanced simulators that allow multi-threading of the simulation (APS) and simplified MOSFET models (UltraSim). An acceleration-factor of about 6.1 was achieved comparing APS and the behavioral model and a factor of 2.2 compared to UltraSim.

In a second step an entire neural front-end with four measurement channels, a multiplexer and an ADC has been simulated. The transient time has been reduced to a factor of ten to accelerate the simulation. The simulation time for

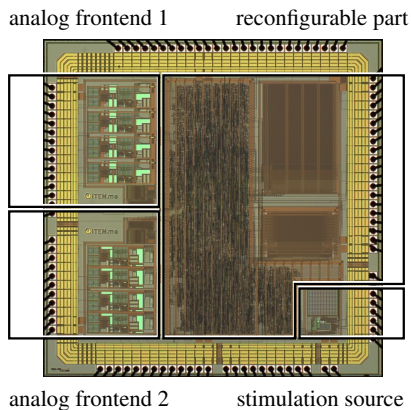


Fig. 7. Picture of mixed-signal ASIC for recording of AP and ECoG signals.

the behavioral model is $t_{AMS} = 331.3$ ms, which is about $83\times$ faster compared to SPICE and $22\times$ faster compared to APS. These accelerations demonstrate the potential of the proposed behavioral models for the design of complex neural measurement systems.

IV. RESULTS

In order to verify the simulation results of the neural front-end, the proposed analog components have been fabricated in a $0.35\ \mu\text{m}$ CMOS process. The size of the final die is about $2.9\ \text{mm} \times 2.9\ \text{mm}$ (Fig. 7). The ASIC contains two analog front-ends, a reconfigurable digital part and an eight channel stimulation source. The stimulation source allows the sequential current stimulation of up to eight electrodes. The results of the measurements are compared to the behavior of the analog models and demonstrate the precision of the behavioral model approach.

A. Component Performance

Since the proposed system is able to acquire APs as well as ECoG signals, two different configurations of the evaluated analog front-end are measured. The focus is set on the frequency response to validate that the major performance of the model and the proposed design agree. According to Table I the demands for measuring LFP signals are low cut-off frequency and an amplification of about $A_{\text{all}} = 56$ dB to exploit the whole dynamic range of the ADC.

In order to validate the design the frequency response of the LNA is measured and compared to the modeled and simulated response. Depending on the capacitive load of the LNA the measured higher cut-off frequency is 12.25 kHz and the amplification is about $A_{\text{LNA}} = 36.05$ dB, which fits the simulated and modeled performance (Fig. 8). Variances appear in the measurement of the lower-cut-off frequency ($f < 100$ mHz) which results from the measurement setup for small frequencies and the simulation of small conductances for the pseudo-resistors. Nevertheless, the lower cut-off frequency for the analog channel is defined by the reconfigurable highpass

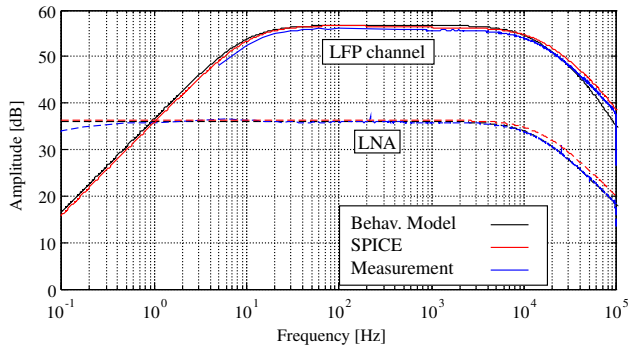


Fig. 8. Frequency response of the LNA and analog channel for LFP configuration.

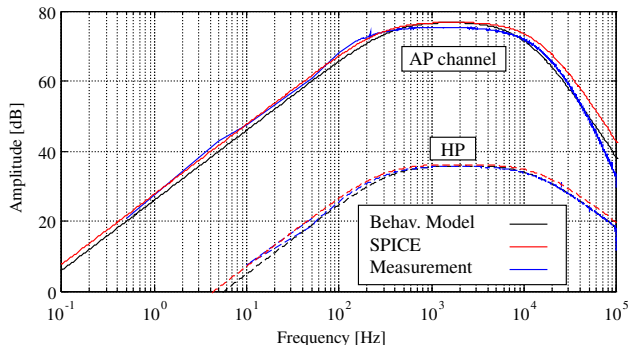


Fig. 9. Frequency response of the adjustable highpass filter and analog channel for AP configuration.

configuration that is set to $f_{3\text{dB}} = 10$ Hz resulting in a sufficient response modeling for the whole channel.

The configuration for AP measurement is different, fulfilling the demand for a higher overall amplification and a higher cut-off frequency for the HP-filter. By reconfiguring the analog channels the measured, simulated and modeled designs show nearly identical behavior. Small deviations appear as the behavioral model consists of a single pole configuration leading to a falling response of 20 dB / decade while the measured design consist of a second pole for high frequencies (Fig. 9). The measured overall amplification of the AP configuration is $A_{\text{all}} = 75.24$ dB having a higher cut-off frequency of 7.99 kHz and a lower one that is depending on the gm-C-cell bias current.

B. Spike Detection

For transient simulation input stimuli of about two seconds have been used. The stimuli contain APs and were recorded from a rhesus monkey that was visually stimulated. For the analysis of the SPICE design and the behavioral model a spike detector was set up, that detects APs within the noisy signal and sums up the total amount of detected spikes.

The algorithm of the spike detector defines a spike threshold by

$$AP_{\text{th}} = 3 \cdot \sigma = 3 \cdot \sqrt{\frac{1}{N} \sum_{i=1}^N (x_i - \mu)^2}. \quad (1)$$

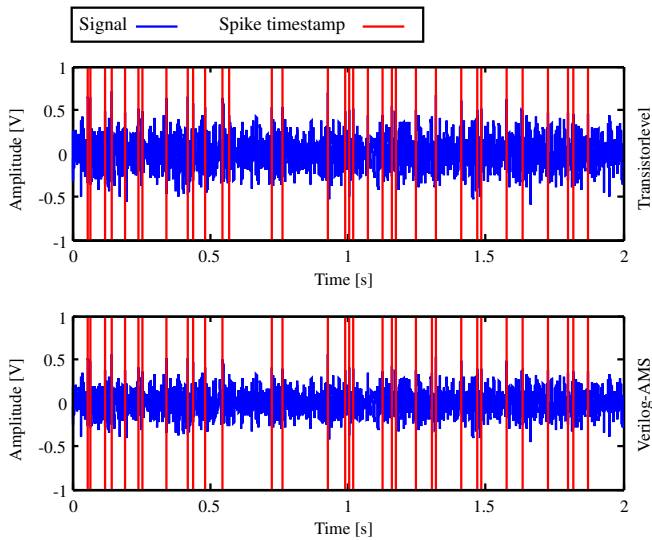


Fig. 10. Transient simulation and timestamps for detected spikes of transistor level and Verilog-AMS model.

Values that exceed this noise level are considered as potential APs. However, the appearance of APs is limited due to the firing rate of each neuron. Therefore, a spike-width is defined that determines the spike interval. Within each interval, the maximum amplitude is considered as potential neural spike.

For both simulation setups nearly the same number of spikes (N_{AP}) was detected, regarding the simulation on transistor level $N_{AP} = 34$ and for the Verilog-AMS model $N_{AP} = 33$. There is a small variation as the APs are very close to the noise level and small variations of the model have an essential influence of the detection rate. Nevertheless, the number of detected APs is sufficient to use the proposed model as a reference with reduced simulation time and to validate basic components of the digital reconfigurable ASIC and the complete mixed-signal IC.

V. CONCLUSION

The modeling of a complex analog recording front-end design for neural measurement systems is shown in this paper. The proposed recording system can measure ECoG as well as AP signals, enabling a wide range of potential application areas. The architecture of the analog channels consists of a low-noise amplifier, an adjustable highpass filter and a variable amplifier stage. An analog front-end combines up to 16 channels with an analog multiplexer and an analog to digital converter. The design and an ASIC implementation for simulation and measurements is demonstrated. Since the simulation of multiple analog channels is very time consuming but important for the test of a whole mixed-signal setup, the modeling in an analog hardware description language is shown. In this way, the simulation is speed up by a factor of 22.2 for a simple four channel front-end. Finally, measurement results of a mixed-signal ASIC are compared to the simulation results on transistor level and to the modeling results. The

results demonstrate the accurate behavior of the frequency response and the transient behavior for the detection of AP signals.

ACKNOWLEDGEMENTS

This research project (RELY) is supported by the Federal Ministry of Education and Research, Germany, under reference number 01M3091.

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