On Candidate Fault Sets for Fault Diagnosis and Dominance Graphs of Equivalence Classes

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Abstract - **The goal of fault diagnosis is to identify a set of candidate faults, or fault locations, that explain an observed faulty output response of a chip. In fault diagnosis procedures that are based on specific fault models, a scoring algorithm can be used for defining sets of candidate faults that include the faults with the highest scores. This paper shows that it is possible to capture the underlying concepts that make fault scoring effective through a graph, which is referred to as the dominance graph. With a test set T used for fault diagnosis, the graph represents the dominance relations between the equivalence classes obtained with respect to T. The observed response R_{obs} of a chip-under-diagnosis is associated with an equivalence class C_{obs}, and C_{obs} is added to the dominance graph. A candidate fault set is defined based on the dominance relations that are added to the graph due to the addition of C_{obs}. Certain properties of these dominance relations point to the type of the defect present in the chip, and the most appropriate algorithm for defining a set of candidate faults based on it.**

I. INTRODUCTION

For a chip that produced a faulty output response to a test set, a fault diagnosis procedure defines a set of candidate faults, or a set of candidate fault locations, which is expected to include the locations of the defects present in the chip [1]-[16].

In a fault diagnosis procedure that is based on a specific fault model, a matching or scoring algorithm can be used for computing a score for every modeled fault [1], [3], [11]. The score measures the likelihood that the fault is present in the chip-under-diagnosis given the faulty observed output response of the chip. The faults with the highest scores are included in the set of candidate faults.

A scoring algorithm considers the numbers of cases (the numbers of tests and observable outputs) of the following types for every modeled fault.

(1) Cases where the modeled fault produces the same value as the chip-under-diagnosis. These cases are denoted by *pass/pass* or $fail/fail$ to indicate that both the modeled fault and the chip produce passing or failing values, respectively. The scoring algorithm typically increases the score in these cases since the response of the modeled fault matches the observed response.

(2) Cases where the modeled fault produces a fault free output value while the output value of the chip is faulty. These cases are indicated by $pass/fail$. The scoring algorithm typically decreases the score for this case since the modeled fault does not explain an observed faulty output value, and other faults must be present to explain it.

(3) Cases where the modeled fault produces a faulty output value while the observed output value of the chip is fault free. These cases are indicated by $fail/pass$. The scoring algorithm may not change the score for this case since the disappearance of a fault effect can be due to the differences between defects and modeled faults, or due to pattern-dependent effects. The modeled fault may still be the best explanation to the observed output response even with this discrepancy. Moreover, other faults do not need to be present in order to explain a faulty output value.

A fault that has no *pass/fail* cases explains all the faulty output values produced by the chip-under-diagnosis. Such a fault typically has a high score, and it is a likely candidate to explain the observed response. The response of such a fault is said to dominate the observed response. Dominance refers to the fact that the fault produces a faulty value for every test and output where the observed response is faulty. Dominance relations were used for accommodating the differences between modeled faults and defects during fault diagnosis in [6]. They were also used in [9] and [10] for speeding up fault diagnosis.

This paper observes that it is possible to capture the underlying concepts that make scoring algorithms effective through a graph, which is referred to as the dominance graph. For this discussion, the dominance graph is defined with respect to the test set T that is used for fault diagnosis. The graph represents the dominance relations between the equivalence classes obtained with respect to T. An equivalence class contains faults that produce identical output responses to T, while faults in different equivalence classes produce different output responses to T. An equivalence class C_{i1} dominates an equivalence class C_{i2} if a fault $f_{i1} \in C_{i1}$ produces a faulty value in response to T for every test and output where a fault $f_{i2} \in C_{i2}$ produces a faulty value. In the dominance graph there is an edge from C_{i2} to C_{i1} in this case.

Let $C = \{C_0, C_1, \cdots, C_{m-1}\}$ be the set of equivalence classes with respect to T. For an equivalence class $C_i \in C$, let R_i be the output response of every fault in C_i to T. Let R_{obs} be the observed response of the chip-under-diagnosis. The analysis presented in this paper defines an equivalence class C_{obs} with output response R_{obs}, and adds it to the dominance graph (only

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the response R_{obs} is known with respect to C_{obs}). Based on the dominance relations that are added to the graph due to the addition of C_{obs}, the paper shows that it is possible to select a set of candidate faults that provides a good match for R_{obs}.

In this paper, the set of modeled faults consists of single stuck-at faults. Other fault models can be considered in a similar way. With single stuck-at faults, several cases are possible depending on the type of defect that produces R_{obs}.

If R_{obs} is obtained due to a single stuck-at fault, $R_{obs} = R_i$ for some $C_i \in C$. In this case, the set of candidate faults should include C_i.

If R_{obs} is obtained due to a single transition or bridging fault, it is possible to show that C_{obs} will be dominated by one or more equivalence classes in C. One of these equivalence classes contains the fault that defines R_{obs}. This is the basis for the fault diagnosis procedure described in [6], and for the procedures from [9]-[10]. In this case, the set of candidate faults should include the equivalence classes that dominate C_{obs}.

The paper focuses on the case where R_{obs} is obtained due to a multiple stuck-at fault. In this case, the paper shows that C_{obs} dominates one or more equivalence classes in C. In most cases, one or more of these equivalence classes contain the faults that define R_{obs}. Therefore, the set of candidate faults should include the equivalence classes that are dominated by C_{obs}. For the small number of cases where R_{obs} is not diagnosed correctly using the equivalence classes dominated by C_{obs}, the paper describes two algorithms by which the set of candidate faults can be extended. The extension is also based on the dominance relations in the dominance graph that include C_{obs}.

A similar analysis can be done for the case where R_{obs} is defined based on defects of different types. The advantage of using the dominance graph is that it is not restricted to a single scoring algorithm. Instead, it allows the relationship between observed responses and the responses of modeled faults to be considered for defining the most accurate set of candidate faults.

An interesting by-product of this analysis is that the dominance relations added to the dominance graph for C_{obs} point to the type of the defect present in the chip. Such information is not provided by scoring algorithms. In addition, the dominance graph points to additional equivalence classes that need to be added to the set of candidate faults in order to ensure that the set includes the defect location(s) in the chip.

The paper is organized as follows. Section II defines the dominance graph, describes its computation, and provides an example to illustrate its features. Section III describes algorithms for defining sets of candidate faults based on the dominance graph. Section IV presents experimental results.

II. DOMINANCE GRAPH

This section defines the dominance graph, describes a procedure for computing it, and illustrates its features.

The dominance graph has a vertex for every equivalence class obtained with respect to a given test set T. The equivalence classes for T are obtained by diagnostic fault simulation. Initially, for a set of faults F, the set of equivalence classes C includes a single equivalence class, $C_0 = F$. Fault simulation of F under a test $t_j \in T$ yields output responses $r_0, r_1, \cdots, r_{l-1}$. Corresponding to r_p there is a set of faults F_p such that all the faults in F_p produce the output response r_p for t_j. The faults in F_p produce an output response that is different from all the other faults in F. Therefore, r_p defines an equivalence class $F_p \cap C_i$ for every $C_i \in C$. Computing $F_p \cap C_i$ for every $0 \le p < l$ and $C_i \in C$, and discarding empty equivalence classes, yields a new set of equivalence classes C. The set of equivalence classes with respect to T is obtained after refining C based on every $t_j \in T$.

During fault diagnosis based on a test set T, all the faults in an equivalence class $C_i \in C$ based on T are included (or excluded) together in (from) the set of candidate faults. This is because all the faults produce the same output response. A diagnostic test set T produces the smallest possible equivalence classes, and allows a fault diagnosis procedure to produce the smallest possible sets of candidate faults.

For illustration, ISCAS-89 benchmark $s27$ is shown in Figure 1. A diagnostic test set for single stuck-at faults in the circuit is shown in Table I. The equivalence classes obtained with respect to this test set using single stuck-at faults are shown in Table II. The fault g stuck-at a is denoted by g/a. For an equivalence class C_i, the set under column R_i describes the response of the faulty circuit in the presence of the faults included in C_i. The set includes an entry j,k if a faulty output value is obtained for test t_j on output z_k. For $s27$, z_0 is line 15, z_1 is line 24, z_2 is line 25 and z_3 is line 26. For the discussion that follows, R_i is taken to be the set of such entries.

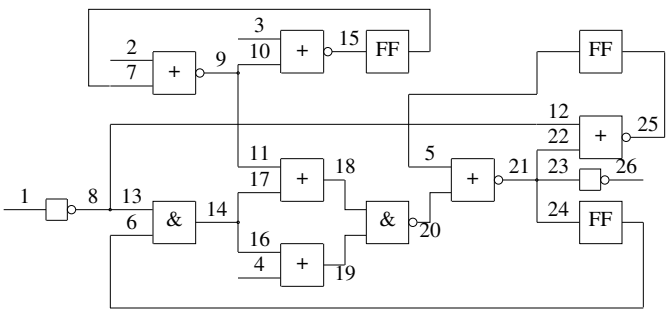

Figure 1. $s27$

TABLE I. Diagnostic Test Set

j	t_j
0	0000011
1	1001010
2	0100110
3	0111001
4	1101011
5	1010000
6	0001011
7	0000010

An equivalence class C_{i1} dominates an equivalence class C_{i2} if $R_{i2} \subseteq R_{i1}$. In this case, the faulty circuit in the

TABLE II. Equivalence Classes

i	C_i	R_i
0	1/0, 8/1	4,1 4,2 4,3 5,2
1	4/1, 16/1, 19/1	5,1 5,2 5,3
2	12/1, 22/1, 25/0	4,2 5,2
3	11/1, 17/1, 18/1	3,1 3,3 4,1 4,2 4,3
4	14/1, 20/0	3,1 3,3 4,1 4,2 4,3 5,1 5,2 5,3
5	23/1, 26/0	2,3 3,3 4,3 5,3
6	2/1, 7/1, 9/0	1,0 1,1 1,2 1,3 7,0
7	4/0, 11/0	1,1 1,2 1,3
8	1/1, 8/0	0,1 0,2 0,3 2,2 3,2 6,1 6,2 6,3 7,1 7,2 7,3
9	3/1, 10/1, 15/0	0,0 2,0 4,0 6,0
10	6/0, 13/0, 14/0	0,1 0,3 6,1 6,3 7,1 7,3
11	5/1, 18/0, 19/0, 20/1, 21/0	0,1 0,3 1,1 1,2 1,3 6,1 6,3 7,1 7,3
12	23/0, 26/1	0,3 1,3 6,3 7,3
13	2/0	2,0
14	3/0	3,0
15	5/0	2,1 2,3
16	6/1	3,1 3,3
17	7/0	0,0 6,0
18	9/1	0,0 2,0 3,1 3,3 4,0 4,1 4,2 4,3 6,0
19	10/0	1,0 7,0
20	12/0	2,2 3,2
21	13/1	4,1 4,2 4,3
22	15/1	1,0 3,0 5,0 7,0
23	16/0	0,1 0,3 7,1 7,3
24	17/0	0,1 0,3 6,1 6,3
25	21/1	2,1 2,3 3,1 3,3 4,1 4,2 4,3 5,1 5,2 5,3
26	22/0	1,2
27	24/0	0,1 1,1 6,1 7,1
28	24/1	2,1 3,1 4,1 5,1
29	25/1	0,2 1,2 2,2 3,2 6,2 7,2

presence of a fault from C_{i1} produces all the faulty output values that are produced in the presence of a fault from C_{i2}. The dominance relation is indicated by an edge from C_{i2} to C_{i1} in the dominance graph.

In the example of $s27$, C_0 dominates C_2 since $R_2 \subseteq R_0$. C_4 dominates C_0 since $R_0 \subseteq R_4$.

To simplify the graph, dominance relations that can be deduced from transitivity are not included in the dominance graph. Thus, if C_{i1} dominates C_{i2}, and C_{i2} dominates C_{i3}, the edge from C_{i3} to C_{i1} is omitted.

In the example of $s27$, C_4 dominates C_0, and C_0 dominates C_2. The edge from C_2 to C_4 is omitted. The dominance graph for $s27$ is shown in Figure 2.

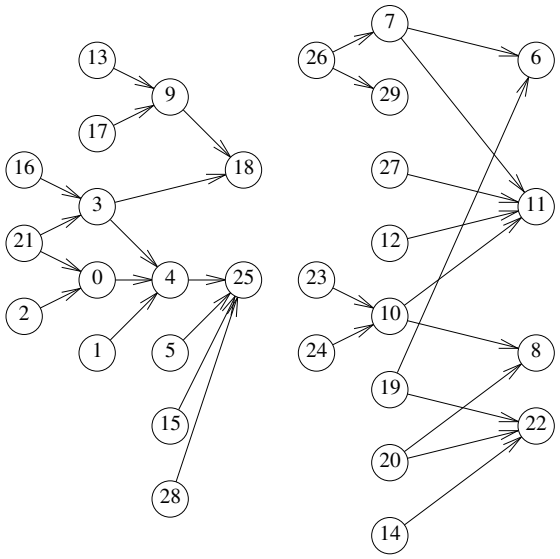

Figure 2. Dominance Graph

The computation of the sets R_i requires fault simulation without fault dropping. This requirement is common for procedures related to fault diagnosis. For example, diagnostic fault simulation performs only limited fault dropping. The computation of the dominance graph requires only set operations and does not require additional fault simulation. Storage of the dominance graph is manageable since the number of vertices is bounded by the number of faults, and the number of edges is typically approximately two or three times the number of vertices.

The following dominance relations obtained for $s27$ illustrate that there exists a structural proximity between equivalence classes that are connected by edges in the graph. This proximity is the basis for the effectiveness of the dominance graph in guiding the definition of sets of candidate faults.

The equivalence class $C_{10} = \{6/0, 13/0, 14/0\}$, with output response $R_{10} = \{0,1, 0,3, 6,1, 6,3, 7,1, 7,3\}$, dominates the equivalence classes $C_{23} = \{16/0\}$ and $C_{24} = \{17/0\}$ with output responses $R_{23} = \{0,1, 0,3, 7,1, 7,3\}$ and $R_{24} = \{0,1, 0,3, 6,1, 6,3\}$, respectively. Lines 16 and 17 are fanout branches of line 14. The faults on the fanout branches have fewer opportunities to propagate to an output. As a result they create fewer faulty values, causing them to be dominated by the fault on the fanout stem.

The equivalence class $C_{10} = \{6/0, 13/0, 14/0\}$ is dominated by the equivalence class $C_8 = \{1/1, 8/0\}$ for a similar reason. In this case, the dominance is related to the fact that line 13 is a fanout branch of line 8.

The opposite can also occur. The equivalence class $C_3 = \{11/1, 17/1, 18/1\}$ dominates the equivalence class $C_{16} = \{6/1\}$. Although there are more paths from line 6 to the outputs than from lines 11, 17 or 18, the longer paths from line 6 require more values to be assigned in order to allow fault propagation. Some of the combinations of values that are required for fault propagation are not possible. The result is fewer faulty output values for the fault on line 6.

In most of the cases, when there is an edge between two equivalence classes in the dominance graph, the faults in the two equivalence classes are included in adjacent fanout free regions of the circuit. Thus, there is a structural proximity between the faults. This proximity is the basis for using the dominance graph to guide the selection of sets of candidate faults as described in the next section.

III. COMPUTING A SET OF CANDIDATE FAULTS

This section describes a procedure for defining a set of candidate faults for a chip with an observed response denoted by R_{obs}, and using the dominance graph.

As in the case of output responses of modeled faults, an entry $j,k \in R_{obs}$ indicates that the observed response has a faulty value for test t_j and output z_k.

Corresponding to R_{obs} the procedure described in this section defines an equivalence class denoted by C_{obs}. The procedure inserts C_{obs} into the dominance graph and computes the dominance relations that need to be added. This does not require fault simulation if the output responses corresponding to the equivalence classes of

modeled faults are stored. Otherwise, fault simulation can be speeded up as in [9]-[10]. As before, dominance relations that can be deduced by transitivity are precluded.

This section focuses on the case where R_{obs} corresponds to a multiple stuck-at fault. Other types of defects can be considered as discussed in Section I. The following examples consider $s27$ with three different multiple stuck-at faults. The faults were selected out of 100 random multiple faults to illustrate the different cases that may occur. A multiple stuck-at fault, which is used for producing an observed response, is denoted by f_{obs}.

The fault f_{obs} = {3/1, 12/1, 22/1} of $s27$ results in R_{obs} = {0,0, 2,0, 4,0, 4,2, 5,2, 6,0}. The addition of C_{obs}, with response R_{obs}, to the dominance graph shown in Figure 2 results in the addition of the edges $C_2 \rightarrow C_{obs}$ and $C_9 \rightarrow C_{obs}$. These edges are based on R_2 = {4,2, 5,2} and R_9 = {0,0, 2,0, 4,0, 6,0}, which are shown in Table II. We have that $R_2 \subseteq R_{obs}$ and $R_9 \subseteq R_{obs}$, implying that C_{obs} dominates C_2 and C_9. In addition, C_2 = {12/1, 22/1, 25/0} and C_9 = {3/1, 10/1, 15/0}. In this case, C_2 and C_9 include all the faults from f_{obs} (and faults that are equivalent to them with respect to the test set). A set of candidate faults that consists of $C_2 \bigcup C_9$ yields the best possible match for the observed response.

The fault f_{obs} = {10/0, 17/1, 25/0} results in R_{obs} = {1,0, 3,1, 3,3, 4,1, 4,2, 4,3, 5,2, 7,0}. The addition of C_{obs}, with response R_{obs}, to the dominance graph shown in Figure 2 results in the addition of the edges $C_0 \rightarrow C_{obs}$, $C_3 \rightarrow C_{obs}$ and $C_{19} \rightarrow C_{obs}$. These edges are based on R_0 = {4,1, 4,2, 4,3, 5,2} $\subseteq R_{obs}$, R_3 = {3,1, 3,3, 4,1, 4,2, 4,3} $\subseteq R_{obs}$ and R_{19} = {1,0, 7,0} $\subseteq R_{obs}$. We have that C_0 = {1/0, 8/1}, C_3 = {11/1, 17/1, 18/1} and C_{19} = {10/0}. Thus, C_3 and C_{19} include two of the faults from f_{obs} (10/0 and 17/1). A set of candidate faults that consists of $C_0 \bigcup C_3 \bigcup C_{19}$ includes two of the faults from f_{obs}. In addition, the fault 8/1 from C_0 is structurally close to the third fault in f_{obs}, 25/0. For the discussion in this paper, only the two faults from f_{obs} that are included in the set of candidate faults $C_0 \bigcup C_3 \bigcup C_{19}$ are taken as an indication of the accuracy of diagnosis.

The fault f_{obs} = {11/1, 14/0, 15/0} results in R_{obs} = {0,0, 0,1, 0,3, 2,0, 3,1, 3,3, 4,0, 4,1, 4,2, 4,3, 6,0, 7,1, 7,3}. The addition of C_{obs} to the dominance graph shown in Figure 2 results in the addition of the edges $C_{18} \rightarrow C_{obs}$ and $C_{23} \rightarrow C_{obs}$. We have that C_{18} = {9/1} and C_{23} = {16/0}. In this case, C_{18} and C_{23} do not include any of the faults from f_{obs}. However, the fault 9/1 from C_{18} is structurally adjacent to the fault 11/1 from f_{obs} (line 11 is a fanout branch of line 9). In addition, the fault 16/0 from C_{23} is structurally adjacent to the fault 14/0 from f_{obs} (line 16 is a fanout branch of line 14). Including C_{18} and C_{23} in the set of candidate faults provides information that may be sufficient to identify the location of the defects. However, for the discussion in this paper, it is required that at least one fault from f_{obs} would be included in the set of candidate faults for the results of fault diagnosis to be considered accurate.

Further analysis shows that C_{23} is dominated by C_{10}, which includes the fault 14/0 from f_{obs}. In addition, C_3 and C_9 are dominated by C_{18}, and these equivalence classes include the faults 11/1 and 15/0 from f_{obs}. Thus, considering the equivalence classes with dominance relations to the ones dominated by C_{obs} provides a way by which to ensure that faults from f_{obs} would be included in the set of candidate faults.

In general, the structural proximity that goes together with dominance relations between equivalence classes makes the dominance graph an effective tool for defining sets of candidate faults. The last example illustrates that, even if the equivalence classes dominated by C_{obs} do not include faults from f_{obs}, they include faults that are at close structural proximity to them. In addition, the dominating or dominated equivalence classes can be used for expanding the set of candidate faults and ensuring that the set includes faults from f_{obs}.

Based on these examples and an analysis of other benchmarks, three algorithms for defining a set of candidate faults are given next. The first algorithm defines the smallest set of candidate faults. Experimental results indicate that it is sufficient in most cases to ensure that the set of candidate faults would include at least one fault from f_{obs}. The second and third algorithms define progressively larger sets of candidate faults for cases where the first set does not include any of the faults from f_{obs}.

All the algorithms define an equivalence class C_{obs} based on R_{obs}, add it to the dominance graph, and find the dominance relations that are added to the graph. All the algorithms target the case where adding C_{obs} defines relations where C_{obs} dominates other equivalence classes in the dominance graph. In all the cases, the set of candidate faults consists of one or more equivalence classes.

Algorithm 0: The set of candidate faults, denoted by $CAND_0$, includes every equivalence class C_i such that C_{obs} dominates C_i.

Algorithm 1: The set of candidate faults, denoted by $CAND_1$, includes $CAND_0$. In addition, it includes every equivalence class $C_i \in C - CAND_0$ such that C_i dominates at least two equivalence classes from $CAND_0$.

This is motivated by several observed responses in benchmark circuits where faults from f_{obs} are included in equivalence classes that dominate two or more equivalence classes from $CAND_0$.

Algorithm 2: The set of candidate faults, denoted by $CAND_2$, includes $CAND_0$. In addition, it includes every equivalence class $C_i \in C - CAND_0$ such that C_i dominates at least one equivalence class from $CAND_0$.

This is motivated by several observed responses in benchmark circuits, including the third example based on $s27$, where faults from f_{obs} are included in equivalence classes that dominate one or more equivalence classes from $CAND_0$.

IV. EXPERIMENTAL RESULTS

This section presents the results of computing sets of candidate faults for observed responses of multiple stuck-at faults based on dominance graphs for benchmark circuits. The goal is not to show that the algorithm based on the dominance graph is more accurate than scoring

algorithms, but that it captures correctly the properties that lead to the accurate identification of sets of candidate faults. As discussed earlier, the dominance graph provides insights into defect properties that are not provided by scoring algorithms. These insights can be used for adjusting the algorithm so as to produce accurate sets of candidate faults for various types of defects.

The test set T used for diagnosis is a compact fault detection test set for single stuck-at faults. Information about the test set is shown in Table III. Column *tests* shows the number of tests in T. Column *cls* shows the number of equivalence classes obtained with respect to T. Column *dom* shows the number of edges corresponding to dominance relations in the dominance graph. For m equivalence classes, the number of edges is bounded by $m(m-1)/2$. Significantly fewer edges are obtained.

TABLE III. Test Sets

circuit	tests	cls	dom
s208	27	201	367
s298	24	274	520
s344	15	309	534
s382	25	372	630
s420	43	398	770
s510	54	547	1423
s526	50	505	1250
s641	22	443	750
s820	94	759	2043
s953	76	1061	2323
s1196	138	1191	2867
s1423	26	1296	2872
s1488	101	1418	4009
s5378	100	4126	10158
s9234	111	5082	12752
s13207	235	7769	18372
s15850	97	9105	20591
s35932	13	22060	49829
s38417	87	27117	59970
s38584	142	31985	72304
b03	24	447	763
b04	44	1321	2939
b05	65	1621	4200
b07	56	1165	2618
b08	39	429	797
b09	25	405	689
b10	45	498	977
b11	60	1021	2771
b14	335	8942	32668
b15	454	19230	109764
b20	437	20423	71566

Observed responses were computed by using 100 random multiple stuck-at faults with multiplicity M, for $M = 5$ and 10. Every fault, denoted by f_{obs}, was simulated to obtain an observed response R_{obs}. In all the cases considered, the equivalence class C_{obs} corresponding to f_{obs} dominated at least one equivalence class based on modeled faults.

A set of candidate faults was defined for every observed response using Algorithm 0. Algorithms 1 and 2 were applied only if the circuit had a set of candidate faults that did not include any fault from f_{obs}.

For an observed response R_{obs}, and for $A = 0$, 1 and 2, let $CAND_A$ be the set of candidate faults computed by Algorithm A. The appearance of a fault from f_{obs} in $CAND_A$ is referred to as a match. The number of matches obtained for f_{obs} using Algorithm A is denoted by n_A. With observed responses corresponding to faults of multiplicity M, $0 \le n_A \le M$. The set of candidate faults is assumed to point correctly to the site of f_{obs} if there is at least one match, or $n_A \ge 1$. A higher value is preferred since it points to more of the sites of the faults in f_{obs}.

TABLE IV. Experimental Results (Multiplicity Five)

			matches						ave
circuit	M	A	0	1	2	3	4	5	cls
s208	5	0	0	4	11	25	40	20	4.55
s298	5	0	0	1	8	10	32	49	6.22
s344	5	0	2	0	11	19	43	25	6.43
s344	5	1	0	0	4	16	45	35	8.72
s382	5	0	0	0	3	15	29	53	5.34
s420	5	0	0	2	11	30	35	22	4.51
s510	5	0	1	3	12	28	35	21	8.01
s510	5	1	0	0	7	23	39	31	11.79
s526	5	0	0	0	4	18	20	58	6.28
s641	5	0	1	4	7	21	35	32	7.81
s641	5	1	0	1	5	12	30	52	12.54
s820	5	0	0	2	1	7	33	57	8.42
s953	5	0	1	2	5	16	30	46	8.33
s953	5	1	0	0	1	12	34	53	11.51
s1196	5	0	0	3	5	14	33	45	7.96
s1423	5	0	0	2	1	11	30	56	5.92
s1488	5	0	0	0	1	11	23	65	6.95
s5378	5	0	0	1	2	13	30	54	5.98
s9234	5	0	0	0	4	3	28	65	5.36
s13207	5	0	0	1	0	3	20	76	5.63
s15850	5	0	0	0	2	6	20	72	6.02
s35932	5	0	0	0	0	6	39	55	4.51
s38417	5	0	0	0	0	0	9	91	5.30
s38584	5	0	0	0	1	3	21	75	4.70
b03	5	0	0	1	6	12	35	46	5.90
b04	5	0	0	0	2	15	20	63	6.11
b05	5	0	0	5	12	31	23	29	7.48
b07	5	0	0	2	8	12	25	53	6.21
b08	5	0	0	3	13	34	22	28	5.74
b09	5	0	0	4	10	22	33	31	6.28
b10	5	0	0	4	10	20	36	30	7.01
b11	5	0	2	6	16	24	29	23	7.80
b11	5	1	0	2	7	19	41	31	14.29
b14	5	0	0	2	7	17	29	45	10.23
b15	5	0	0	0	6	15	19	60	15.30
b20	5	0	0	0	3	11	30	56	7.40

The average number of equivalence classes that are included in $CAND_A$ is another parameter that indicates the accuracy of fault diagnosis. A smaller number of equivalence classes is preferred for ensuring that the set of candidate faults is as small as possible.

The results of diagnosing observed responses corresponding to faults of multiplicity five are shown in Table IV, and the results for faults of multiplicity ten are shown in Table V. Column M shows the fault multiplicity used for computing observed responses. Column A shows the algorithm used for defining sets of candidate faults. Column *matches* shows the number of instances (out of the 100 considered) in which $n_A = 0, 1, \cdots, M$. Column *ave cls* shows the average number of equivalence classes that are included in a set of candidate faults, where the average is computed over the 100 instances considered.

From Tables IV and V it can be seen that, in most of the cases, Algorithm 0 is sufficient for ensuring that the set of candidate faults includes at least one fault from f_{obs} (in this case, the number under column *matches* subcolumn 0 is zero). The same applies when f_{obs} is a fault of multiplicity five or ten. Thus, there is no deterioration of the results in this sense when faults of higher multipli-

TABLE V. Experimental Results (Multiplicity Ten)

			matches											ave
circuit	M	A	0	1	2	3	4	5	6	7	8	9	10	cls
s208	10	0	0	4	6	14	17	21	21	13	2	2	0	7.62
s298	10	0	0	1	2	2	5	10	9	17	26	24	4	11.11
s344	10	0	0	1	2	5	19	15	12	32	9	5	0	11.89
s382	10	0	0	0	1	3	5	6	17	24	22	18	4	11.88
s420	10	0	0	0	4	4	15	27	14	22	9	3	2	7.81
s510	10	0	0	1	4	13	17	18	17	16	8	5	1	15.60
s526	10	0	0	0	0	2	3	8	8	17	31	18	13	12.27
s641	10	0	1	0	3	9	8	18	18	17	16	4	6	14.59
s641	10	1	0	0	0	3	8	5	14	22	26	13	9	23.35
s820	10	0	0	0	0	1	3	3	15	13	24	24	17	16.19
s953	10	0	0	1	2	5	7	13	13	17	19	18	5	16.83
s1196	10	0	0	0	0	3	5	14	20	24	22	7	5	18.46
s1423	10	0	0	0	1	0	0	6	12	20	31	24	6	13.99
s1488	10	0	0	0	0	1	1	1	11	8	25	28	25	14.36
s5378	10	0	0	0	0	1	0	4	11	12	23	31	18	13.44
s9234	10	0	0	0	0	0	0	1	6	8	21	35	29	11.65
s13207	10	0	0	0	0	0	0	2	2	5	14	19	58	12.83
s15850	10	0	0	0	0	0	0	1	4	10	14	32	39	13.65
s35932	10	0	0	0	0	0	0	0	0	7	17	50	26	10.22
s38417	10	0	0	0	0	0	0	0	0	0	4	16	80	11.15
s38584	10	0	0	0	0	1	0	0	1	1	8	34	55	11.47
b03	10	0	0	0	1	3	5	6	16	18	26	16	9	12.82
b04	10	0	0	0	0	0	3	4	11	22	27	21	12	12.80
b05	10	0	0	1	3	11	16	17	25	18	5	4	0	16.28
b07	10	0	0	0	1	1	3	10	19	15	22	21	8	13.77
b08	10	0	1	1	3	7	18	23	12	19	9	5	2	10.99
b08	10	1	1	0	1	6	17	15	18	19	15	5	3	14.30
b08	10	2	0	0	1	3	7	11	19	26	22	7	4	34.93
b09	10	0	0	0	0	5	11	16	22	17	14	11	4	11.98
b10	10	0	0	0	4	10	12	19	23	15	11	5	1	14.42
b11	10	0	1	0	3	12	18	22	19	16	7	2	0	15.95
b11	10	1	0	0	0	2	8	17	27	21	21	3	1	32.77
b14	10	0	0	0	4	1	7	10	12	18	19	21	8	28.34
b15	10	0	0	0	0	0	3	14	8	15	13	20	27	36.48
b20	10	0	0	0	0	0	4	2	15	14	26	30	9	22.55

cities are considered.

The number of equivalence classes included in the set of candidate faults is higher when diagnosing faults of multiplicity ten. This is partly due to the fact that more faults should be included in the set of candidate faults since they are included in f_{obs}.

In most of the cases where Algorithm 0 is not sufficient for obtaining a match for f_{obs}, Algorithm 1 is sufficient. The increase in the number of equivalence classes, which are included in the set of candidate faults when using Algorithm 1 or even 2, is manageable.

V. CONCLUDING REMARKS

This paper showed that it is possible to capture the underlying concepts that make scoring algorithms effective for fault diagnosis through a graph, which was referred to as the dominance graph. The graph represents the dominance relations between the equivalence classes obtained with respect to the test set used for fault diagnosis. Under the analysis performed in this paper, the observed response R_{obs} of a chip-under-diagnosis is translated into an equivalence class C_{obs}, and added to the graph. A candidate fault set is defined based on the resulting graph. For multiple stuck-at faults, which were considered in this paper, the addition of C_{obs} adds relations where C_{obs} dominates equivalence classes in the graph. The dominated equivalence classes were used for defining the set of candidate faults. In general, properties of the graph can be used for identifying the type of the defect present in the chip, and the most appropriate algorithm for defining a set of candidate faults based on it.

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