Non-Invasive Pre-Bond TSV Test Using Ring Oscillators and Multiple Voltage Levels*

Sergej Deutsch and Krishnendu Chakrabarty
Duke University
Durham, NC 27708, USA

***Abstract*—Defects in TSVs due to fabrication steps decrease the yield and reliability of 3D stacked ICs, hence these defects need to be screened early in the manufacturing flow. Before wafer thinning, TSVs are buried in silicon and cannot be mechanically contacted, which severely limits test access. Although TSVs become exposed after wafer thinning, probing on them is difficult because of TSV dimensions and the risk of probe-induced damage. To circumvent these problems, we propose a non-invasive method for pre-bond TSV test that does not require TSV probing. We use open TSVs as capacitive loads of their driving gates and measure the propagation delay by means of ring oscillators. Defects in TSVs cause variations in their RC parameters and therefore lead to variations in the propagation delay. By measuring these variations, we can detect resistive open and leakage faults. We exploit different voltage levels to increase the sensitivity of the test and its robustness against random process variations. Results on fault detection effectiveness are presented through HSPICE simulations using realistic models for 45nm CMOS technology. The estimated DfT area cost of our method is negligible for realistic dies.**

I. Introduction

Three-dimensional (3D) stacking with through-silicon vias (TSVs) is gaining considerable traction in the semiconductor industry due to its benefits over traditional stacking with wire-bonds. Unlike wire-bonds, TSVs go directly through the substrate, consuming relatively little silicon area and allowing for high-performance, high-density, and low-power inter-die connections in integrated circuits (ICs) [1].

Testing of 3D ICs for manufacturing defects pose major challenges for the semiconductor industry [2], [3]. One of these challenges is new defects due to the TSV manufacturing process; such defects include voids and pinholes. Voids, as shown in Figure 1 are formed due to insufficient filling [4]. A pinhole is an oxide defect that creates a short between the TSV and the substrate [5]. Many of these defects arise prior to the bonding process. Therefore, they can be targeted during pre-bond testing, increasing the probability of getting a known good die (KGD) prior to bonding and therefore increasing the product yield. It has been widely acknowledged that the lack of KGD can be a serious yield limiter for 3D stacking [2], [6].

However, pre-bond testing of TSVs is difficult because of test access limitations. First, prior to wafer thinning, TSVs are buried in silicon and are only accessible at their front-side through the logic connected to the TSVs. Second, even though the back side of the TSVs is exposed after wafer thinning, probing on those is challenging because of strict requirements on the probing equipment. Recent studies report success in mechanical probing at array pitches of 40 μm [7]; however, such probing solutions are still being researched and it remains to be seen how easily they can be used in practice. Therefore, alternative solutions that do not rely on probing must also be investigated.

In this work, we propose a method for non-invasive pre-bond TSV test using ring oscillators and multiple voltage levels. We can detect resistive opens and leakage faults by measuring variations in the delay of nets connected to TSVs. The proposed method offers the following benefits.

- Due to electromigration and TSV stress, resistive open and leakage defects get aggravated over time. Even though they become more easily detectable in the field, we offer an option for targeting resistive opens and leakage early during manufacturing testing, improving the product yield, reducing long-life failures, and decreasing the need for field testing.
- By exploiting multiple supply voltage levels, we can increase the detection sensitivity and robustness for both resistive-open faults and leakage.
- The proposed TSV test method is non-invasive, which means that we do not require custom cells to be inserted into the design: the proposed DfT circuitry only consists of standard cells. Moreover, no probing with external equipment is necessary.
- The test cost of the proposed method is low since we do not require TSV probing and the DfT area overhead is negligible.

The remainder of this paper is organized as follows. Section 2 outlines related prior work on TSV testing. In Section 3, we describe our TSV fault models and the proposed method for pre-bond TSV test using ring oscillators. Section 4 presents experimental results. Finally, Section 5 concludes the paper.

II. Related Prior Work

3D test has become a hot topic in the testing community. A number of recent publications have addressed several aspects of 3D test, such as new DfT architectures for logic test [8], [9], post-bond TSV test [10], [11], and repair [12]. Pre-bond TSV testing remains one of the major challenges in a 3D test flow due to limited access to TSVs. In the following paragraphs, we briefly review several methods for pre-bond TSV test that have been proposed in the literature.

Noia and Chakrabarty have proposed a method for TSV testing in which multiple TSVs are mechanically contacted by the same probe needle to measure TSV capacitance and

*The work of S. Deutsch and K. Chakrabarty was supported in part by the National Science Foundation under grant no. CCF-1017391 and by the Semiconductor Research Corporation (SRC) under contract no. 2118.001.

978-3-9815370-0-0/DATE13©2013 EDAA

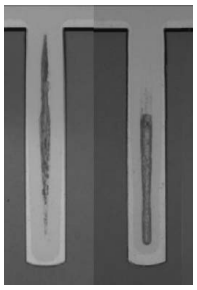

Fig. 1: Voids in 10 μm x 60 μm TSVs [4].

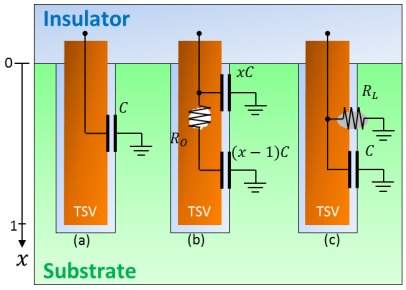

Fig. 2: TSV models: (a) fault-free, (b) micro-void, (c) pinhole.

resistance [13]. This approach allows for the testing of multiple TSVs simultaneously at the expense of measurement resolution, significantly reducing the test time. Simulation results have demonstrated high measurement accuracy even in the presence of process variations and probe contact variations. Despite its benefits, this method has several drawbacks. First, it places extra burden on the test equipment, such as custom and active probe cards. Second, the method requires multiple contacts on the back side of the thinned wafer, which can be difficult in practice. Finally, mechanical force on TSV tips and micro-bumps can result in damage of TSVs, leading to their degraded performance or even failure.

Chen et al. have proposed a methodology for detecting capacitive TSV faults [6]. In this method, a TSV is charged to a certain voltage level and then its charge is shared among a number of TSVs. After charge sharing, a sense amplifier measures the voltage of TSV, from which the TSV capacitance can be deduced. This method also allows for the detection of leakage faults. A major drawback of this approach is its susceptibility to process variations. In addition, this method requires analog structures on the die that are not part of typical standard cell libraries and need to be manually designed and optimized.

Huang et al. have developed a solution for detecting resistive open faults and leakage faults in TSVs [14]. Their method is similar to "input sensitivity analysis", which was designed for post-bond TSV diagnosis using ring oscillators [10].

Hao and McCluskey proposed very-low-voltage testing to detect resistive shorts and hot-carrier-induced degradation [15]. They have shown that the effects of these defects are increased at voltage levels lower than V_{DD}, which has been supported by analytical models and SPICE simulations [16], [17]. This prior work motivated us to consider using multiple voltage levels for pre-bond TSV test. Since multiple-voltage testing neither imposes limits on the test equipment nor requires extra on-chip DfT structures, it can be applied in practice without introducing additional hardware costs [18], [19]. Moreover, since pre-bond TSV test does not require long test sequences (scan data), test time does not grow significantly if multiple voltages are used.

III. Pre-Bond TSV Test Using Ring Oscillators

Many TSV defects manifest themselves as variations in electrical parameters of the TSVs. We propose to detect these faults by a parametric test. Our work is motivated by "input sensitivity analysis" [10], an approach for post-bond TSV diagnosis. We extend this method for pre-bond TSV test and show that it is also possible to use ring oscillators to detect resistive open faults and leakage faults. We next describe our electrical model of a fault-free and faulty TSV, and the proposed test method.

A. TSV Fault Model

We focus on two types of TSV faults: resistive opens and leakage faults. Several TSV defects can be modeled by these faults. For instance, micro-voids increase the TSV resistance at the defect location and thus can be modeled as a resistive-open fault. Pinholes create a conduction path from the TSV to the substrate, resulting in a leakage fault. Since a TSV is a passive structure resembling a wire, it can be modeled using a combination of lumped R, C, and L elements. The TSV inductance is relatively small and has no significant effect below a few GHz signal frequency [20]; therefore we limit our TSV models to RC circuits. In the following, we describe simple electrical TSV models for the three cases: fault-free, resistive-open fault, and leakage.

In the fault-free case, a TSV can be modeled as multiple RC segments, where R is the TSV resistance and C is the capacitance between the TSV and the substrate. R and C depend on the TSV technology; current studies report the following values [20]: $R = 0.1\ \Omega$, $C = 59$ fF.

Since R is significantly smaller than the output resistance of a typical driving gate, it can be neglected. The resulting model is a capacitor between the TSV and substrate, as shown in Figure 2(a). We verified this simplification by using HSPICE to simulate and compare charge curves of (1) multiple RC segments with combined resistance $R = 0.1\ \Omega$ and combined capacitance $C = 59$ fF, and (2) a single capacitor $C = 59$ fF, where both loads are driven by a 4X buffer. The resulting curves show no measurable difference, which justifies the treatment of a fault-free TSV as a lumped capacitor.

Figure 2(b) shows a micro-void in the TSV at an arbitrarily chosen location x and the corresponding electrical model. This defect divides the TSV into two segments. The "top" segment ($[0, x]$) is the part of the TSV until the fault location and can be approximated as a capacitor with the scaled-down capacitance xC. The "bottom" segment ($[x, 1]$) includes the rest of the TSV capacitance $(1 - x)C$ and the increased resistance of the open R_O that depends on the size of the void. The parameter R_O can vary from a few Ω in case of a micro-void to infinity in the case of a full open in the TSV.

Figure 2(c) shows a leakage defect, such as a pinhole defect, which creates a conduction path from the TSV to the substrate. The leakage is modeled by the resistor R_L, which is in parallel to the TSV capacitance. The value of R_L might decrease over time, since leakage faults tend to deteriorate. Such defects are a serious concern for lifetime chip reliability.

B. Ring Oscillators with TSVs

The goal of our method is to detect leakage and resistive-open faults by a parametric test. Deviations in TSV parameters due to defects lead to variations in the propagation delay of the net connected to the TSV. These variations can be measured by ring oscillators. A ring oscillator is a feedback loop containing an even number of inverters. Due to inversion of the signal in

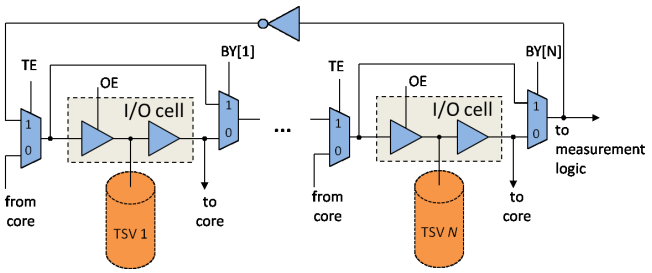

Fig. 3: Ring oscillator with N TSVs.

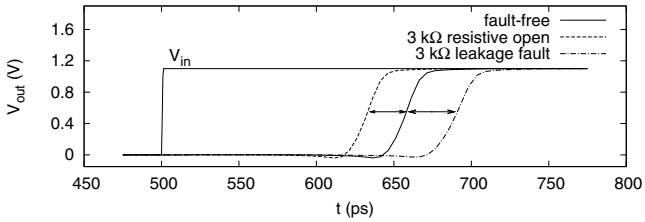

Fig. 4: Voltage waveforms for the fault-free case and 1.5 kΩ open-resistive fault.

the loop, it keeps oscillating with a frequency that depends on the delay of the elements in the loop.

As in [14], we create ring oscillators containing TSV drivers and receivers and use TSVs as loads. Deviations in TSV parameters lead to variations in the propagation delay of the net connected to the TSV and thus variations in the oscillation period. The oscillation period can be captured by simple on-chip DfT hardware based on a binary counter or linear-feedback shift-register and compared with an expected value.

Resistive opens and leakage defects have different impacts on the oscillation period. In the case of a resistive open, the top part of the TSV capacitance xC is separated from the bottom capacitance $(x-1)C$, which increases the charging and discharging rate for the top capacitor. This leads to a decreased delay between the driver and receiver buffers; therefore the oscillation period decreases as well.

A leakage fault has a different effect on the oscillation period. Due to charge leakage to the ground through R_L, the driver charges the TSV capacitance slower but discharges it faster. However, the impact on the charging rate is stronger, hence the period of one oscillation cycle including one low-to-high transition and one high-to-low transition is larger than in a fault-free case.

In contrast to [14], which is limited to the testing of one TSV at a time, we propose to combine N I/O segments and one inverter to form a ring oscillator, as shown in Figure 3. This configurations allows for the testing of M ($1 \leq M \leq N$) TSVs simultaneously and determining whether one of the TSVs under test is faulty. Since resistive opens and leakage faults have the opposite effect on propagation delay, the total delay in a group with two faulty TSVs (one a resistive open and the other a leakage) can be unchanged and the faults can remain undetectable. However, such pairs of faults (and the associated defect-induced delay combinations that cancel out each other) are likely negligible for high-yield TSV processes, which is required for high-volume 3D chip production.

Each I/O segment includes a TSV and a bidirectional I/O cell connected to the front side of the TSV. We assume that the I/O cells are part of the functional circuitry, which is common in industrial designs. This aspect of our design contrasts with [14], where custom I/O cells are required even though these I/O cells are likely to be chosen based on functional requirements. TSVs can also be enhanced with tri-state drivers so that they can be driven appropriately.

Figure 4 shows waveforms of the simulated voltages V_{out} measured at the I/O cell outputs ("to core") if a step function is applied at the input of the cell. In presence of a 3 kΩ resistive open at $x = 0.5$, the propagation delay of the cell with the TSV as load is reduced by ≈ 20 ps. A 3 kΩ leakage fault, in contrast, increases the propagation delay by ≈ 30 ps. This observation is consistent with our theory. Since the propagation delay of the I/O cell adds to the oscillation period T of the ring oscillator, we can detect both types of faults by comparing T with that of the fault-free case.

The number of TSVs in a group (N) can be selected based on the desired oscillation frequency. In the extreme case, if $N = 1$, the ring oscillator contains only a couple of gates, which results in a relatively short oscillation delay (or high frequency). Such an oscillation frequency might be too high to drive the on-chip measurement logic. By appending extra segments, we increase the delay and thus reduce the oscillation frequency, relaxing the speed requirement on the measurement circuitry. In addition, all TSVs in the same group can share the same counter without extra decode logic, since all of them are in the oscillator loop. This reduces wiring and the amount of DfT logic.

The signal `TE` (test enable) controls the multiplexers selecting between the functional outputs coming from the internal logic and the oscillator loop. If `TE`=0, the multiplexers 1 select the functional outputs coming from the internal logic, enabling a functional mode. If `TE`=1, the circuit is configured in an oscillator loop, enabling a TSV test mode. The signals `BY[1]...BY[N]` (Bypass) control the multiplexers that include or exclude a TSV from the oscillator loop. `OE` (output enable) controls the tri-state drivers of the I/O cells. In functional mode, this signal is set by the internal logic. In test mode, `OE` is set to 1 to enable the drivers.

Figure 5 shows an overview of the entire DfT architecture for the pre-bond TSV test. The control logic block receives test control signals from the test equipment or from a higher-level DfT structures that control this part of DfT logic. The control logic generates signals to control the ring oscillators, to select which ring oscillator is measured, and to start, stop and reset the measurement logic. The signals from the oscillators are fed through a decoder to the measurement logic. This logic can be implemented as an n-bit binary counter that uses the oscillating signal as clock. Its count after a fixed amount of time can be directly mapped to an oscillation frequency. Alternatively, we can use a linear feedback shift register (LFSR) in the same way as a binary counter. The LFSR approach requires less gates for the same upper limit on the count; however, a look-up table is needed to determine the oscillation frequency corresponding to the current LFSR state. The resulting signature from the measurement logic is read and interpreted by the test equipment.

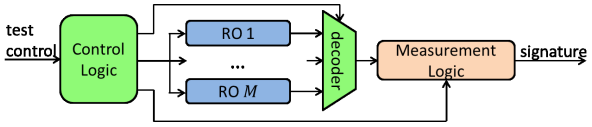

Fig. 5: Pre-bond TSV test DfT architecture.

IV. Experimental Results

We verified our approach by simulations with HSPICE. For the simulations, we used the TSV models described in Section III and the 45 nm Predictive Technology Model (PTM) low-power CMOS models (http://ptm.asu.edu/). As TSV drivers, we use X4 buffers from the Nangate 45nm Open Cell Library (www.nangate.com). For other gates, X1 versions are used. These gate strengths are representative, as reported in recent literature [20].

A. Resistive-Open Faults

First, we simulate a resistive-open fault in one of the TSVs at the location $x = 0.5$ as depicted in Figure 2(b). We create a HSPICE circuit model of the ring oscillator shown in Figure 3 with $N = 5$ TSVs and sweep R_O from 0 Ω (no fault) to 3 kΩ (strong resistive open) at the nominal voltage $V_{DD} = 1.1$ V. With this model, we perform transient analysis and record the oscillation period of the ring oscillator T. In the first run, TSV1 is enabled (`BY[1]=0`) and all other TSVs are bypassed (`BY[2...N]=1`). In the second run, we disable all TSVs. Subsequently, we subtract the oscillation period of the second run T_2 from that of the first run T_1 for each value of R_O:

$$\Delta T = T_1 - T_2$$

During actual test, the values T_1 and T_2 will be measured by the on-chip DfT and the results sent to the test equipment and post-processed there. Alternatively, it is possible to implement on-chip logic for the post-processing and reduce the shift-out time. However, we do not focus on the measurement circuitry in this paper and leave these details for future work.

The above subtraction step removes the propagation delay of the path through I/O cells $2 \ldots N$ and the inverter. The remainder is the propagation delay due to the I/O cell and TSV1, which is under test. This approach greatly reduces the effect of delay variations in gates and interconnects due to random process variations.

The results of this simulation are shown in Figure 6. As expected, an increase in R_O leads to a reduction of the oscillation period. This indicates that we can detect resistive opens of a sufficient size by measuring the oscillation period. For instance, ΔT of a resistive defect of size 1 kΩ at $x = 0.5$ is reduced by 10% compared to the fault-free case that can be identified.

The location x of the defect plays a critical role for fault detection. The more the fault is moved to the top of the TSV, where it is connected to the driver, the more easily we can detect it. A void at the bottom of the TSV is not detectable. However, this is a problem for all pre-bond TSV test methods.

In a realistic (3D) IC, propagation delays of gates vary significantly because of random process variations. This can potentially have a detrimental effect on the resolution of our test method, since we rely on relatively constant delays in our DfT circuitry to be able to detect variations of the delay on the net connected to the TSV. Therefore, we need to verify whether our method is robust to random process variations, which leads us to the next set of experiments using HSPICE.

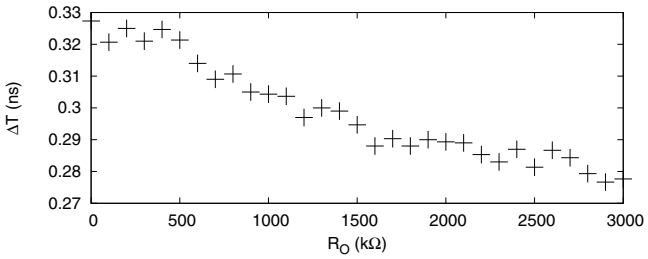

Fig. 6: ΔT as a function of R_O at location $x = 0.5$ and at 1.1 V supply voltage.

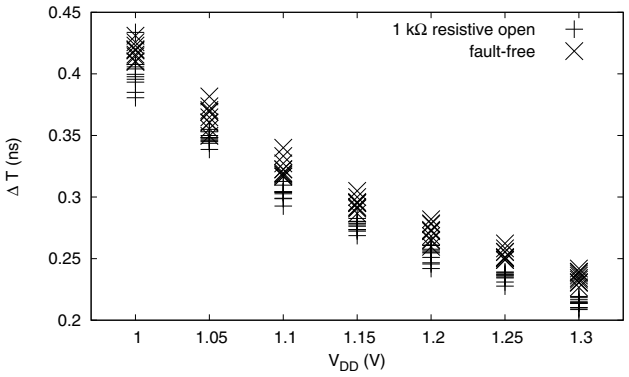

Fig. 7: ΔT as a function of supply voltage in (a) fault-free case and (b) in case of 1 kΩ resistive open at $x = 0.5$.

To see the effect of process variations and the effect of applying different supply voltages, we run a number of Monte Carlo (MC) simulations using the model described above extended by the following process-variation model: $3\sigma_{V_{th}} = 3$, $3\sigma_{L_{eff}} = 10\%$, where $\sigma_{V_{th}}$ is the variation in threshold voltage and $\sigma_{L_{eff}}$ is the variation in gate length. These data are consistent with the those reported by industry for recent technology nodes [21].

Figure 7 shows the results of MC simulation for a fault-free TSV and a TSV with a resistive open defect of size 1 kΩ. We varied the supply voltage and analyzed the spread in the fault-free and faulty cases. We observe that at lower supply voltage levels, a part of data points from both fault-free and faulty cases overlap and thus become indistinguishable. If we increase the supply voltage, this overlap reduces to a minimum until we see no aliasing. From this, we conclude the following.

- Even in presence of process variations, our TSV test method allows for detection of resistive-open defects that have a sufficiently large size and are located in the upper part of the TSV. The test resolution depends on the process variation: the more variation, the harder it becomes to distinguish small resistive opens from the fault-free case.
- Higher supply voltage results in a better resolution: aliasing is reduced, allowing for detection of smaller resistive-open faults.

B. Leakage Faults

Leakage faults exhibit a different behavior than resistive open faults. To show this, we used the same simulation

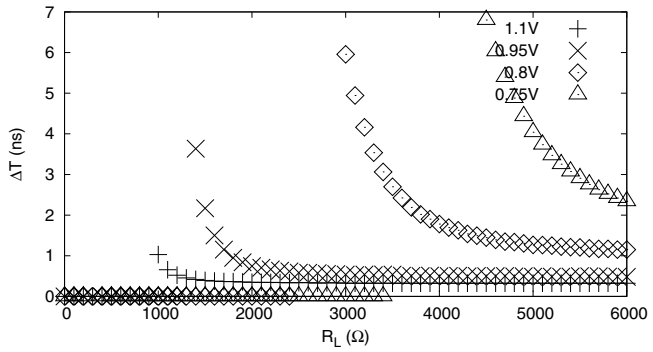

Fig. 8: ΔT as a function of R_L at different voltage levels.

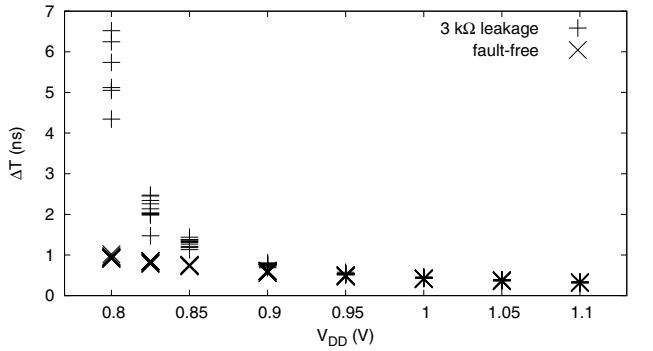

Fig. 9: ΔT as a function of supply voltage in (a) fault-free case, and (b) in case of 3 kΩ leakage fault.

approach as described above ($N = 5$). Figure 8 shows the dependence of ΔT on the leakage R_L for different voltage levels. First, we observe that leakage faults increase the oscillation period, which makes them distinguishable from the fault-free case as well as resistive open faults. This is also consistent with our expectation. Second, strong leakage faults below a certain threshold, $R_L \approx 1$ kΩ, prevent the circuit from oscillating. In other words, the TSV exhibits stuck-at-0 behavior. This threshold depends on the supply voltage: it drops as we increase the voltage. The third observation is that in the regions slightly above each threshold, ΔT is extremely sensitive to small variation in leakage. This indicates that we can easily detect leakage of a wide range if we test at different voltage levels. Strong leakage (R_L low) will show up at higher V_{DD}. Weak leakage will become detectable at lower V_{DD}. This observation is consistent with the results of prior work on very-low-voltage tests for bridging faults [16], [17].

Next, we perform MC simulations to verify the robustness of our test method. Figure 9 shows the results of MC simulations for a 3 kΩ leakage fault and the fault-free case at different voltage levels. We see that in the sensitive region right above the threshold (≈ 0.75 V), the data points for the two cases do not overlap. As we increase V_{DD}, the gap between them becomes smaller such that we cannot distinguish between the faulty and fault-free cases.

The simulation results confirm that resistive opens and leakage faults significantly change the oscillation period T and hence we can detect them using the proposed method. Since resistive opens reduce T and leakage faults increase T, these fault types are distinguishable from each other. The results also show that TSVs should be tested at multiple voltage levels in order to increase fault detectability.

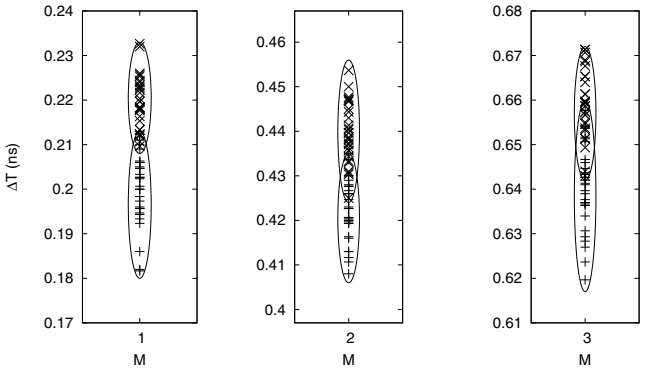

Fig. 10: Spread overlap for fault-free and faulty (1 kΩ resistive open at $x = 0.5$) cases increases with M.

C. Detection Resolution Limitations

Even though we significantly reduce the effect of process variations by cancelling out the propagation delay of all elements in the oscillation loop except for the segment with the TSV under test, the variations in this segment limit the detection resolution of our method. It cannot be identified whether a small deviation of T from that of the fault-free case is due to a TSV defect or due to variations in the gates or both. Therefore, for each measured T, there is a certain range of faults that correspond to it (aliasing). This range depends on the process parameters and on the circuit layout. A more mature process and a more robust circuit layout reduce aliasing. A quantitative analysis of aliasing due to process variations is an item for future work.

Our method allows for simultaneous testing of M TSVs included in one oscillator loop. We ran a number of MC simulations for different values of M. Figure 10 shows the spread of ΔT for a faulty and a fault-free TSV with larger M. In case $M = 1$, the overlap is relatively small, hence the probability for aliasing is also small and the fault is likely to be detected. As M increases, the overlapping areas grow such that the faulty and the fault-free cases cannot be distinguished. This results from the fact that the effect of process variation is not cancelled out for the M segments under test. Therefore, there is a trade-off between the number of TSVs tested in parallel and detection resolution.

Another mechanism limiting detection resolution is measurement inaccuracy of binary counters and LFSRs. We use a reference clock to generate "reset" and "stop" signals for the counter such that the time interval t between them is known. The clock input of the counter is driven by the oscillator output signal, the period of which we want to measure. After "reset", the counter starts counting and stops after "stop". Subsequently, the counter is reconfigured into a shift register and the counter state (signature) c is shifted out to the test equipment for post-processing. The oscillation period is then calculated as $T^* = \frac{t}{c}$.

This value may differ from the actual oscillation period T due to the digital nature of the counter as a measurement circuit. Figure 11 shows two extreme cases of "reset" and "stop" times with respect to the waveform of the oscillating signal V_{out}.

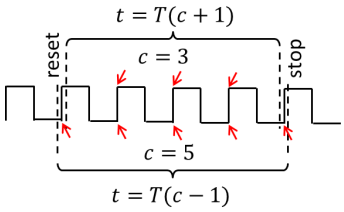

Fig. 11: Two extreme cases for "reset" and "stop" positions on the signal waveform.

In one case, the counter is reset shortly after a rising edge of V_{out} and stopped shortly before a rising edge, such that the counter "misses" an entire cycle. In the opposite extreme case, the counter is reset shortly before a rising edge of V_{out} and stopped shortly after a rising edge. As a result, the counter will count one extra cycle. Therefore, we have upper and lower bounds on the counter state based on t and T:

$$\frac{t}{T} - 1 \leq c \leq \frac{t}{T} + 1$$

In the first extreme case, the calculated period T^* will be larger than the actual one:

$$T^* = \frac{t}{c} = \frac{t}{\frac{t}{T} - 1} = T\left(\frac{t}{t-T}\right) = T + \frac{T^2}{t-T} = T + E_+,$$

where $E_+ = T^2/(t-T)$ is the absolute error. Similarly, the other case will result in a T^* smaller than T with the error $E_- = T - T^* = T^2/(t+T)$. Since we use $t \gg T$ for precise measurements, both errors can be approximated as $E = T^2/t$. This implies, that the measurement result obtained with a binary counter will be no worse than $T \pm E$.

As an example, consider a ring oscillator configuration with $T = 5$ ns (200 MHz). For a maximum error $E = 0.005$ ns, a time interval $t \geq 5^2/0.005$ ns $= 5$ μs is required. The counter state after 5 μs will be 1000, which means that at least a 10-bit binary counter is needed for the required maximum error.

D. DfT Area Cost

The standard cell area overhead of our DfT is relatively small. Per TSV, we add two multiplexers to select between functional and test signals and to be able to include (exclude) any TSV into (from) the oscillator loop. The inverter in each ring oscillator is shared among N TSVs. In our experiments, we used multiplexers from the Nangate 45nm library with the standard cell area 3.75 μm^2 and inverters with the standard cell area 1.41 μm^2. If the functional design contains 1000 TSVs and $N = 5$, the total standard cell area of the oscillators is

$$2 \times 3.75 \times 1000 + 1.41 \times 1000/5 = 7782\ \mu\text{m}^2 < 0.01\ \text{mm}^2,$$

which is less than 0.04% of a 25 mm^2 large die and hence is negligible.

The circuitry for test control and measurement of the oscillation period can be implemented using standard digital cells. The exact implementation of this circuitry is not the focus of this work; however, this DfT hardware can be shared among multiple TSV groups such that the total amount of pre-bond TSV test logic becomes negligible compared to the area of the entire die.

V. Conclusions

We have introduced a method for pre-bond TSV test using ring oscillators. We have shown that we can detect leakage and resistive-open faults early during manufacturing testing, thereby increasing the product yield. Our test method provides a high degree of resolution, hence we can identify weak faults that might become critical during "aging" of the product.

Our method is non-invasive: we do not require TSV probing, which is associated with increased cost for the probe equipment and possible damage to the TSV. We only use standard cell for our DfT structures, hence no custom circuit layout is required. We exploit different levels of supply voltage to increase resolution. The results show that the test for resistive open defects is more robust at higher voltage levels. Leakage faults, in contrast, should be tested at lower voltages. For each voltage level, there is a certain range of the leakage that can easily be detected. This approach allows for the detection of weak leakage faults that are hard to detect at the nominal voltage. Monte Carlo simulations show that our method is effective in the presence of process variations, a key requirement for nanoscale devices.

References

[1] K. Banerjee *et al.*, "3-D ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration," *Proceedings of the IEEE*, vol. 89, pp. 602–633, 2001.

[2] H.-H. S. Lee and K. Chakrabarty, "Test Challenges for 3D Integrated Circuits," *IEEE Design & Test of Computers*, vol. 26, pp. 26–35, 2009.

[3] E. J. Marinissen and Y. Zorian, "Testing 3D Chips Containing Through-Silicon Vias," in *ITC*, Nov. 2009, pp. 1–11.

[4] D. Rohde *et al.*, "Filling TSV of Different Dimension Using Galvanic Copper Deposition," in *IMPACT*, Oct. 2011, pp. 355–358.

[5] M. Tsai *et al.*, "Through Silicon Via (TSV) Defect/Pinhole Self Test Circuit for 3D-IC," in *3DIC*, Sep. 2009, pp. 1–8.

[6] P.-Y. Chen, C.-W. Wu, and D.-M. Kwai, "On-Chip Testing of Blind and Open-Sleeve TSVs for 3D IC before Bonding," in *VTS*, Apr. 2010, pp. 263–268.

[7] K. Smith *et al.*, "Evaluation of TSV and Micro-Bump Probing for Wide I/O Testing," in *ITC*, Sep. 2011, pp. 1–10.

[8] E. J. Marinissen, J. Verbree, and M. Konijnenburg, "A Structured and Scalable Test Access Architecture for TSV-Based 3D Stacked ICs," in *VTS*, Apr. 2010, pp. 269–274.

[9] S. Deutsch *et al.*, "Automation of 3D-DfT Insertion," in *ATS*, Nov. 2011, pp. 395–400.

[10] J.-W. You *et al.*, "Performance Characterization of TSV in 3D IC via Sensitivity Analysis," in *ATS*, Dec. 2010, pp. 389–394.

[11] S.-Y. Huang *et al.*, "Small Delay Testing for TSVs in 3-D ICs," in *DAC*, Jun. 2012, pp. 1031–1036.

[12] L. Jiang, Q. Xu, and B. Eklow, "On Effective TSV Repair for 3D-Stacked ICs," in *DATE*, Mar. 2012.

[13] B. Noia and K. Chakrabarty, "Pre-bond probing of TSVs in 3D stacked ICs," in *ITC*, Sep. 2011.

[14] L.-R. Huang *et al.*, "Radar-Like Pre-bond TSV Test and Diagnosis," in *private correspondence*, 2012.

[15] H. Hao and E. McCluskey, "Very-Low-Voltage Testing for Weak CMOS Logic ICs," in *ITC*, Oct. 1993, pp. 275–284.

[16] Y. Liao and D. Walker, "Fault Coverage Analysis for Physically-based CMOS Bridging Faults at Different Power Supply Voltages," in *ITC*, Oct. 1996, pp. 767–775.

[17] M. Renovell, P. Huc, and Y. Bertrand, "Bridging Fault Coverage Improvement by Power Supply Control," in *VTS*, 1996.

[18] P. Engelke *et al.*, "The Pros and Cons of Very-Low-Voltage Testing: an Analysis Based on Resistive Bridging Faults," in *VTS*, 2004.

[19] D. Arumi *et al.*, "Diagnosis of Bridging Defects Based on Current Signatures at Low Power Supply Voltages," in *VTS*, 2007.

[20] Y.-J. Lee, I. Hong, and S. K. Lim, "Slew-Aware Buffer Insertion for Through-Silicon-Via-Based 3D ICs," in *CICC*, 2012, invited Paper.

[21] K. Bernstein, "High-performance CMOS variability in the 65-nm regime and beyond," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 433–449, Jul. 2006.