

UTBB FD-SOI: a Process/Design symbiosis for breakthrough energy-efficiency

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Abstract— UTBB FD-SOI technology has become mainstream within STMicroelectronics, with the objective to serve a wide spectrum of mobile multimedia products. This breakthrough technology brings a significant improvement in terms of performance and power saving, complemented by an excellent responsiveness to power management design techniques for energy efficiency optimization. The symbiosis between process and design is key in this achievement enabling to provide already at 28nm node a real differentiation in terms of flexibility, cost and energy efficiency with respect to any process available on the market.

Keywords: *UTBB FD-SOI, CMOS, high-performance, low-power, mobile application, SoC, energy efficiency, Back-Bias*

I. INTRODUCTION

Nowadays, going to the 20nm node – and even already at 28nm – conventional planar transistors become unable to offer optimal performance without draining your battery or raising the temperature of your smartphone beyond safe limits. The conventional CMOS on Bulk silicon is highly inefficient to meet the demands of Smart Mobile Devices, mainly because of the so-called short channel effects that more and more impact the speed increase at each subsequent technology node. In the last decade, all possible strain techniques have been applied to boost the mobility and continue the performance growth rate. Looking at next CMOS generation, 20nm and beyond, customers have started complaining that the speed boost offered by the technology is not enough, also compared to the exponential increase of manufacturing costs. Today, the industry has identified in the building of fully depleted transistor a way to continue the technology roadmap, thanks to the good electrostatic control offered by such devices.

Using fully depleted devices, and in particular FD-SOI, enable not only running CPUs at very high maximum frequency but also enables very low voltage operations still getting a much better CPU performance than bulk and then allowing to run “CPU consuming tasks” while minimizing power dissipation. In this context, STMicroelectronics is implementing planar fully depleted silicon technology

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considered by the industry as the best-in class candidate to compete in the forthcoming superphones era and multimedia convergence segments.

II. PLANAR UTBB FD-SOI: STRUCTURE AND ADVANTAGES

Fully depleted transistors can be either planar or tri-dimensional. In the tri-dimensional flavor (FinFET or TriGate), the gate wraps around the sides of a vertical silicon ‘fin’. In the planar flavor, thin film transistors are fabricated in an ultra-thin layer of silicon over a buried oxide (BOX) (Fig. 1). Being a natural evolution of the conventional planar Bulk technology, STMicroelectronics has chosen the 2D planar fully depleted silicon-on-insulator as mainstream CMOS technology [1]. An industrial solution is currently deployed at 28nm with the aim to get a boost in speed and power improvement before the 20nm bulk technology arrival.

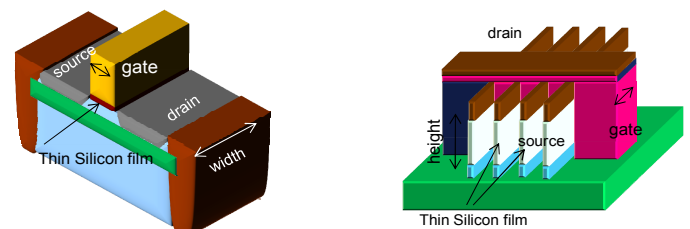


Figure 1. 2D Planar UTBB FD-SOI and 3D Finfet devices perspective

28nm UTBB FD-SOI CMOS transistors are fabricated in a 7nm thin layer of silicon sitting over a 25nm buried oxide (BOX) [2] (Fig. 2). The process is comparatively simple with respect to Finfet and even conventional bulk technologies. The UTBB FD-SOI has been plugged on the basis of the 28LP Bulk HKMG process from ISDA. At this node, more than

10% of the process steps and three masks are saved, resulting in an overall process cost saving of 10%.

Only 3 process steps are specific to UTBB FD-SOI, all the others being derived from the conventional 28LP Bulk:

- Raised S/D epitaxy for access resistance reduction
- Ground plane implantation for threshold voltage adjustment
- Hybridization for SOI/BULK co-integration

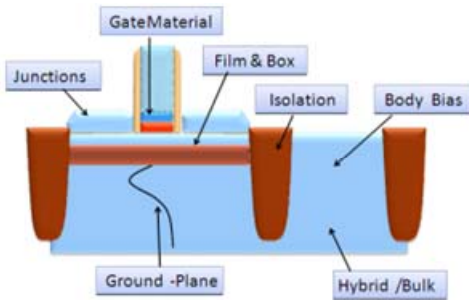


Figure 2. 2D Planar UTBB FD-SOI cross section

As a fully depleted technology, UTBB FD-SOI enable to strongly reduce the impact of the two major detractors to the efficiency of traditional technology that are the transistor variability and the electrostatics, which govern the Ion/Ioff current ratios. The planar FD transistors do not require doping or pocket implants in the channel to control the electrostatic and tune the threshold voltages, which is a fundamental advantage from a variability point of view. The thin silicon film ensures that all electrical paths between source and drain are confined close to the gate, leading to a significant improvement of the sub-threshold slope and DIBL [3]. This means for a given leakage target, the minimum channel length of the UTBB FD-SOI technology can be further scaled down over its bulk counterpart. For instance, at 28nm the minimum channel of the UTBB transistor is 24nm while in bulk it cannot be scaled down below 28nm (Fig. 3). It is one of the key differentiator offered by the technologists offering to circuit designers a significant speed boost or wider range of static power optimization thanks to poly biasing.

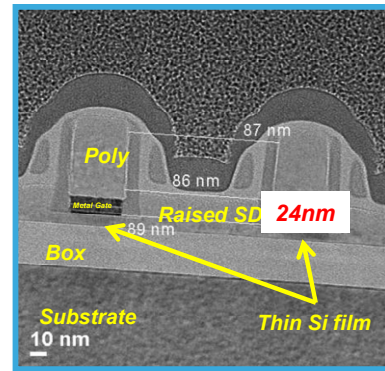


Figure 3. UTBB FD-SOI transistors cross section

In addition, the BOX offers naturally ultra-shallow junctions and a total dielectric isolation of the transistor, leading to lower source/drain capacitance, lower leakage as well as a pretty good latch-up immunity. The BOX enables also a wider range of body biasing that bulk or Finfet technologies cannot match. In this case, the substrate is doped underneath the box and plays the role of a second gate that can be independently biased.

A. UTBB FD-SOI: a hybrid technology

To be compliant with already existing design developed in bulk technology, a hybrid solution has been introduced enabling the co-integration of bulk and SOI devices on the same die. The hybrid section is obtained prior to device fabrication by etching the top silicon and BOX as shown in Fig. 4. Thanks to this key solution, both body biasing design techniques and ESD protection strategies do not need to be specifically redeveloped and thus can be easily ported from bulk technology. In order keep the cost of the UTBB FD-SOI technology under control and minimize the impact at design level, the decision was taken conjointly between process and design engineers to put most of the gated devices on the SOI region and implement the volume conduction devices such as bipolar, vertical diodes on the bulk side as described in Figure 5.

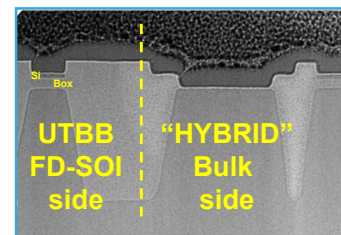


Figure 4. Hybridization in UTBB FD-SOI

Device Type	UTBB FDSOI	BULK
Logic	2Vt	
SRAM	✓	
Cap, Varactor	✓	
Drift MOS (OTP)		✓
Digital I/O	✓	
Analog MOS	✓	
RF MOS	✓	
Resistors	✓ (Poly)	✓ (Active)
Diodes (antenna)		✓
ESD Devices	✓ (FET)	✓ (FET, diode, SCR)
Vertical Bipolar		✓

Figure 5. Device partitioning

B. UTBB FD-SOIs vs Bulk effort metrics

The strategy when developing the 28nm planar FD technology has been to reuse as much as possible the 28nm low-power bulk CMOS process. Overall, the back-end of the line is identical to the traditional 28nm bulk low-power CMOS process, and the front-end is 80% common with that same process (Fig. 6). In addition to sharing many steps, the planar FD process saves about 10% of the processing steps required to fabricate the chips. This roughly offsets the increased wafer cost. As a result, the 28nm planar FD technology matches the cost of a conventional low-power technology while, delivering extremely competitive performance and offering 10% lead time versus a full new development in the next generation. It is worth noticing, since UTBB FD-SOI is derived from a 2D planar bulk technology, no investment in manufacturing equipment is required [5].

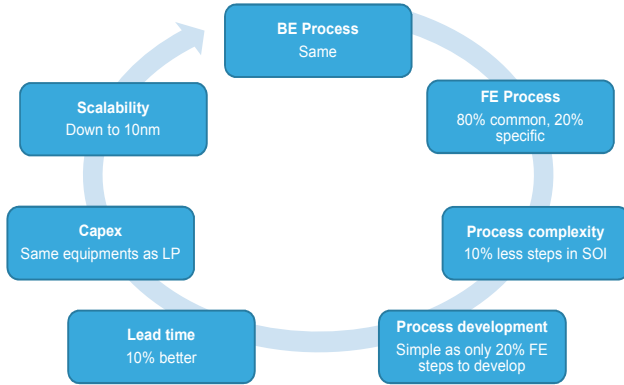


Figure 6. UTBB FD-SOI vs BULK: effort metrics

III. DESIGN CONSIDERATIONS

A. Design Platform in UTBB FD-SOI

STMicroelectronics has developed a complete design platform for SOC including a full set of library and its associated design flow. Thanks to the fact UTBB FD-SOI is non-disruptive with respect to previous node, this technology enables the reuse of not only process blocks but also design practices and IPs. UTBB FD-SOI offers the advantage of using a conventional design flow as conceived for bulk technologies. The CAD tools to design on UTBB FD-SOI are the same as those classically used with any the industry (Fig. 7.).

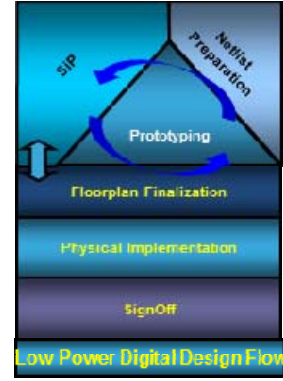


Figure 7. UTBB FD-SOI SOC Design Flow

About the content of the design platform, it is identical to the one developed in bulk technology (Fig. 6). It contains a first set of IPs such as logic library cells, memory compilers that are directly ported from bulk without any modifications [4]. This is made possible thanks to the fact the process engineers are able to easily maintain the same NMOS/PMOS current ratio between both technologies. With respect to the second set of IPs such as I/Os, analog IPs and fuses for instance, a redesign/retuning is mandatory in order to take into account the analog/ESD characteristics of the FDSOI devices and manage the co-integration at layout level. On low power techniques, the same is applicable are applicable to FD-SOI. However, some specificities exist if wanting to leverage the FD-SOI technology such as optimized power switches, extended poly-bias offer in multi-channel standard cells libraries and extended body bias. Of course, the full design platform must be re-characterized with a specific UTBB FD-SOI model [5] for various bias conditions depending on the performances targeted. From an electrical point of view, FD-SOI transistors are modeled as standard 4-terminal transistors, so no requiring any change in netlists.

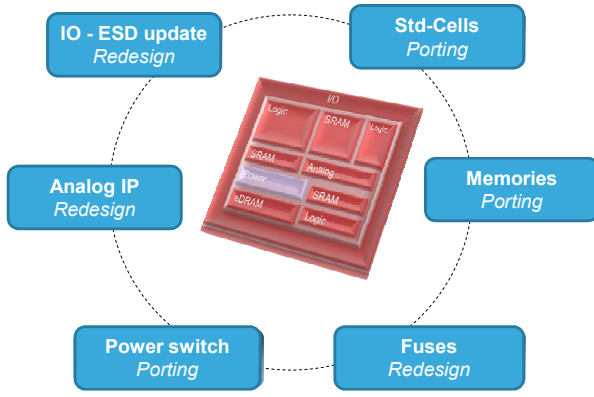


Figure 8. Bulk to UTBB FD-SOI migration strategy

B. Dynamic Process Scaling in UTBB FD-SOI

Dynamic Process Scaling in UTBB FD-SOI is the key feature of the technology enabling to combine high performance and low power for optimum energy efficiency. Dynamic Process Scaling consists in applying a voltage just under the BOX of target transistors in order to shift their threshold voltage to either get higher performance or reduce the leakage power consumption. The principle is well known and widely applied in bulk technology but unfortunately less and less efficient in advanced CMOS technologies. Thanks to its better electrostatics, UTBB FD-SOI exhibits a higher body factor over its bulk counterpart, 85mV/V vs 25mV/V which leads to a significant drive current boost as shown in Figure 9 [6]. Moreover, it is worth noting the body bias range in bulk technology is limited to -300mV in RBB due to GIDL, while FBB is limited to +300mV because of source-drain junction leakage and latch-up risk at higher voltage and temperature (Fig. 10). The UTBB FD-SOI technology enables an extended body-bias range from -3V (RBB) up to +3V (FBB). This provides designers a new lever for energy efficiency optimization, performance boosting, ultra-low-voltage functionality and leakage reduction [7].

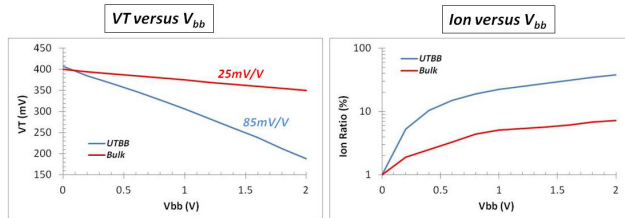


Figure 9. Body bias efficiency of 28nm UTBB FDSOI vs Bulk

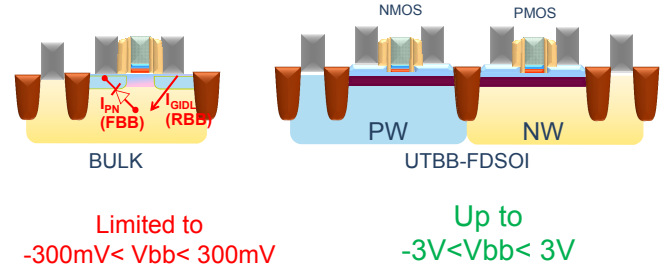


Figure 10. UTBB FDSOI vs Bulk body biasing structure

C. SOC migration in UTBB FD-SOI

The porting of an SOC from Bulk to UTBB FD-SOI is quite straightforward. The migration of an existing design from bulk to UTBB FD-SOI represents an effort comparable to half-node migration. All the high speed blocks leveraging body biasing like CPUs or GPUs must be synthesized. All the others such as SOC blocks for which the main objective is power savings, by reaching the target operating frequencies at lower Vdd, a direct porting with ECO is possible. Of course, all the analog and IOs must be swapped by their FDSOI counterpart.

IV. CIRCUIT LEVEL BENCHMARK: UTBB FD-SOI vs BULK

Thanks to excellent device electrostatics, FDSOI is capable of showing fast devices, typical of “G” processes with the low leakage characteristic of “LP” technologies. This is exemplified through the chart shown in figure 11, illustrating the speed/leakage trade-off of 28nm FD-SOI devices vs. the ones in 28LP and 28G technologies, in worst-case sign-off conditions, characterized for a core critical path. As we can see in the graph, 28nm FDSOI technology is faster than 28G, with better leakage than 28LP. With the Dynamic Process Scaling capability obtained through back-biasing, it is possible to dynamically shift device V_t in order to either lower the V_t when needing more speed, or raise it when running at lower speeds to optimize the leakage power.

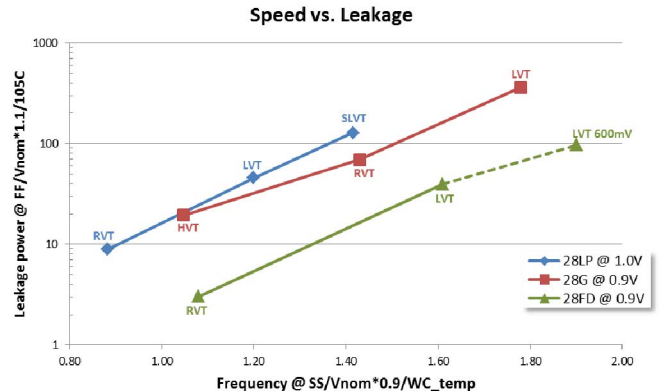


Figure 11. Best operating frequency for any class of leakage

Thanks to its extended Vdd range, FD-SOI technology is also best suited for Dynamic Voltage and Frequency Scaling (DVFS) [8]. A comparison for a multi-core subsystem is shown in figure 12. 28nm FD-SOI technology is able to provide outstanding performances at low Vdd, 550MHz at 0.6V and up to 800MHz if applying 600mV of forward back-bias. In terms of relative performances vs. 28LP technology, it means +29% or +39% with 600mV FBB at 1.2V, and +247% or +403% with 600mV FBB at 0.6V.

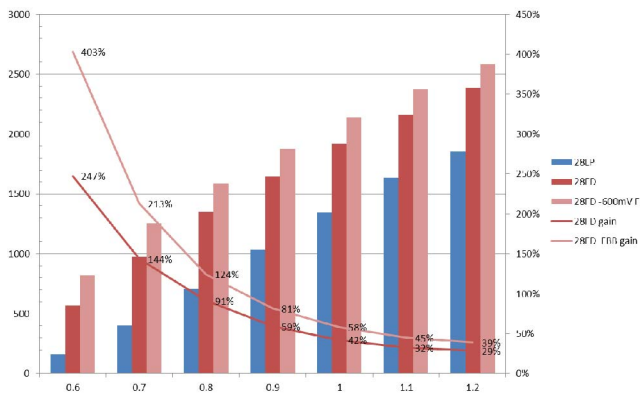


Figure 12. Multi-core speed vs. Vdd

Figure 13 illustrates the energy efficiency of a multi-core subsystem measured in DMIPS/mW as function of the core speed. Looking at the three technologies, we can observe that while 28LP is negatively affected by dynamic power consumption and 28G is affected by high leakage, 28nm FD-SOI is able offering the best compromise, resulting in best power efficiency up to 50% better than 28LP and 2x better than 28G.

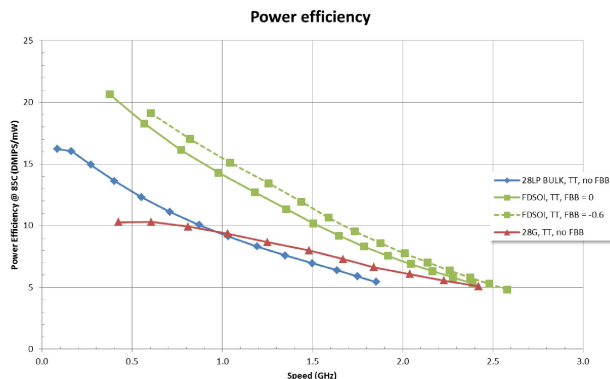


Figure 13. Energy efficiency for a multi-core subsystem

V. TECHNOLOGY ROADMAP

MOSFET scalability is nowadays monitored with the intensity of the so called drain-induced barrier lowering,

DIBL. For its scalability, UTBB FD-SOI technology can leverage on both gate and substrate dimensions. For next generations, the box thickness will play a key role to continue the scaling while keeping a good electrostatic control. [8] published a roadmap in 2010 for devices scaling down to 10nm, and demonstrated being able to process gates on silicon films as thick as 3.5nm.

Node	28nm	20nm	14nm	10nm
T_{SOI} (nm)	7.5	6.5	6	5.5
T_{BOX} (nm)	25	20	15	10

Figure 14. Tbox scaling for gate shrink

A roadmap for scaling FD-SOI down to 10nm is already established including the introduction of boosters for improving device mobility, as illustrated in figure 15.

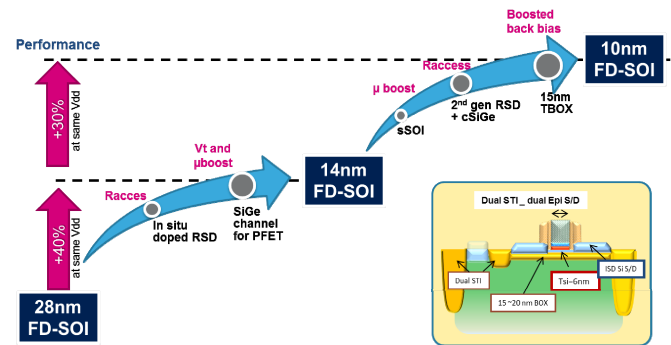


Figure 15. FD-SOI process scaling roadmap

As a result, ST UTBB FD-SOI technology roadmap is defined, encompassing a 14nm node to be available for prototyping by H1 2014, and a 10nm node for 2016, as shown in figure 16.

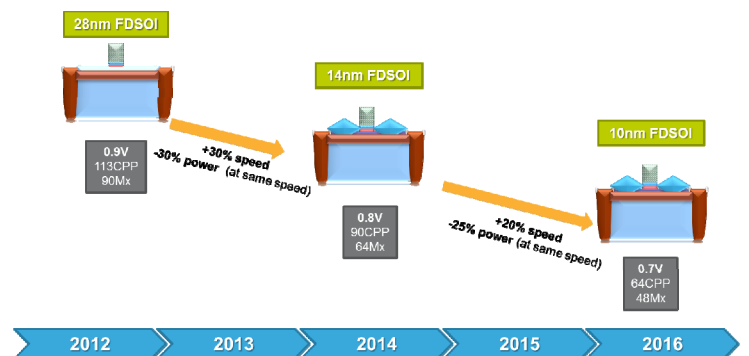


Figure 16. UTBB FD-SOI wafer scalability down to 10nm node

VI. CONCLUSION

UTBB FD-SOI is becoming a must for modern mobile and consumer multimedia products targeting high performance at low power in a cost effective manner. Today at 28nm, moving from a conventional bulk technology to UTBB FD-SOI is equivalent to a full node benefit for simply half node effort. Looking ahead at 14nm and beyond, UTBB FD-SOI will remain the most compelling solution over the competition thanks to its ability to extend the life of 2D planar process and design architectures at low manufacturing risk and to offer best in class energy efficient solution based on the unique concept of dynamic Process scaling.

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