Towards Adaptive Test of Multi-core RF SoCs

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Abstract: *This paper discusses how adaptive test techniques can be applied to multi-core RF SoCs, together with design implementation and test challenges. Various techniques specific to RF circuits covering calibration trims, power management modules, co-existence issues, concurrent testing, and test measurements are explained. Results on different designs are presented. Together, they highlight the need and scope of adaptive test for RF circuits, and share a new dimension in the test of multi-core circuits, under different constraints of design, test and test equipment.*

Keywords: *Adaptive test, RF test, multi-core chips, test time optimization.*

I. Introduction

Test in traditional multi-core devices has been investigated in the literature to perform optimizations in the test schedule under the constraints of design and tester resources, to optimize a combination of test time, test mode power, test data throughput, test interface bandwidth, etc. Various core configurations have been considered with different variations of DFT therein, and with different levels of DFT in the SoC which integrates these cores. SoCs are moving towards integrating multiple RF modules in a single chip implementing various transmission protocols and standards (e.g. WLAN, GPS and derivatives, FM, BTH, NFC, etc.), and supporting their concurrent operation. These multi-core RF SoCs pose some new challenges for test by virtue of the fact that there are new issues of dependencies between cores and dependencies on how these cores are integrated into an SoC. Examples of this include: (i) There is a need for several trims and calibrations (sometimes applied in a specified sequence) in the SoC level and in the RF cores before tests can be applied. (ii) Many configurations of power management modules have to be considered for test and characterization, corresponding to different functional scenarios. (iii) While concurrent test amongst the RF cores is desirable, its feasibility depends not only upon available tester resources, but also upon the level of coupling / interference between the cores. (iv) Architecting an optimal test schedule is more challenging since the cores couple with detrimental effect, impacting the accuracy of the measurements. (v) There are many forms of functional tests and BIST, and selection of the right technique is often dependent on factors outside the DUT.

An adaptive test schedule for such multi-core RF SoCs must now comprehend all of the above. In this paper, we illustrate through different examples how adaptivity can be built into the tests for such an SoC, and their benefits. The examples are based on practical design and test considerations. Some new areas of investigation are also proposed.

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In this paper, adaptivity in test includes (i) adaptive tests for test cost reduction, (ii) adaptive tests for better performance characterization, and (iii) adaptive tests for mitigating issues with design and test environments. This paper is organized into seven sections. Sections II to VI discuss adaptive calibration and trims, adaptive test of power management modules, concurrent test of RF modules, handling co-existence issues with multiple radio cores, and different adaptive RF test measurements, respectively. Section VII concludes the paper.

II. Adaptive Test Methods for Power Management Modules

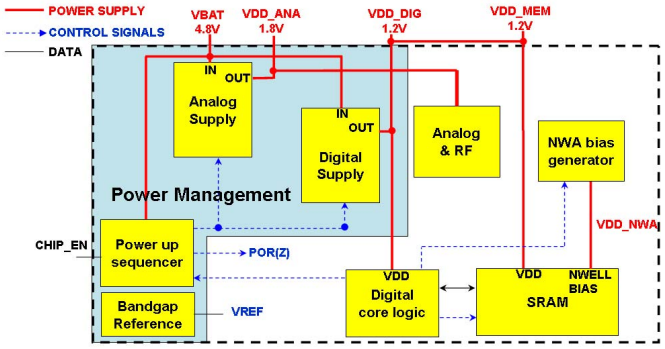

Fig. 1. Typical embedded system with integrated power management

Fig. 1 shows the block diagram of a power management (PM) system integrated in an SoC. Such a PM function is often integrated to take care of diverse power-supply requirements and sequences for all the analog and digital (CPU, peripherals and memories) modules. It offers the advantages of lower cost and increased flexibility at the system level including for dynamic optimization of power and performance, since different power-up sequences can be combined together with different functional and test modes of operation, based on different application scenarios. Such an integrated PM system forces different requirements for adpative test. These are: (i) Different configurations of PM based on customer applications. (ii) Different sequences of power-up amongst the different components, namely analog, digital, embedded digital inside analog, and embedded memories. (iii) Different stress test requirements for these components.

Together, these requirements also provide significant scope for optimizations (in terms of coverage, test power and test time / cost) through adaptive test methods at different stages of maturity of the testing process. Some design and test techniques that enable adaptive test of embedded PM circuits are discussed next.

A. Adaptive Test of Power Management Module

The functional power-up sequence of an SoC with multiple RF cores and embedded PM must allow for necessary settling times of individual PM components (to avoid unintended system level effects like simultaneous inrush currents by spreading the peak current consumption) to improve the operational reliability of portable battery powered systems. Adopting this sequence for test, results in higher test costs, especially with multiple test insertions per device. There are design solutions reported in [1] and [2] having a dedicated shorter power-up sequence by using external tester resources and bypassing the on-chip supplies during various device test modes. The test sequences are now adapted to optimise the number of power supplies required from the tester (ATE), the time required for the power-up sequence to be executed and the number of modules which are required to be powered up for maximum test throughput. This also relaxes the requirement for the on-chip supplies having to support higher peak currents, faster operation, etc. in the test modes. This segregation between functional and test modes also makes the device more easy to integrate into a system. Examples where such techniques have been successfully adopted include optimal VDD_NWA sequencing, (refer to [1] and [3]), to improve the overall robustness and test time of the mandatory reliability qualification test (accelerated stress test) techniques like burn-in (BI) and high temperature operating life (HTOL) with another variation of test mode power-up sequence to work-around the special requirements for memories in ultra-deep sub-micron (UDSM) technologies, etc. Test time savings of several tens of milli-seconds have been realised for each test insertion / test application with a dedicated power-up sequence.

B. Trim for Package Stress Effect Mitigation

Many critical analog parameters are influenced by several environmental and neighborhood conditions like noise coupling, temperature, humidity, supply voltage levels and mechanical stress due to the package and neighbouring circuit structures on the chip. The effect of package stress on critical analog components has been reported in literature [4] causing both absolute parametric shifts and device mismatches. There are no known formal methods to perform pre-silicon analysis to study these effects on circuit and system performance. Hence additional design margin and DFT hooks, e.g. providing for trim capability of certain critical circuits post-packaging, extending trim range and resolution for existing parametric trims, etc. are needed. This directly impacts the ability to deliver useable packaged parts through dynamic test adaptation, to circumvent issues due to highly sensitive circuits like bandgap reference (BGR) and oscillator circuits, and eventual failures at power-up of the system (at specific temperatures, and packages, etc.). Post-package trim capabilities enable selective yield improvement as well as on-field circuit / function tuning.

C. Adaptive Stress Test Methods

Accelerated stress tests like BI and HTOL are important for integrated circuit (IC) reliability qualification [5]. While the design closure is done to ensure functionality at extreme environmental conditions, the stress tests themselves do not mandate a tight distribution of all electrical parameters during the stress application. Instead, nominal functionality has to be ensured after the completion of such tests. Deviations of some electrical parameters beyond a certain threshold during the application of the stress tests can result in unacceptable stress conditions and eventually in catastrophic life-time operating failures. Such failures are detected late at silicon qualification time when stress tests are applied for extended hours, (as against first silicon bringup) and can result in many design / DFT and test iterations. Such analysis is even more difficult with legacy or older technologies and with vendor fabrication services, for which the necessary reliability and ageing simulation models may not exist. Such an analysis is helpful to adaptively test devices for different operating life-time conditions (e.g. which amongst modules A and B will be on for a longer time) based on the end customer application. A few illustrations follow.

1) Life Time Parametric Shift: Supply Monitor Threshold

Portable battery powered applications require that the PM function in the SoC monitors the power supply voltage levels, and accordingly switches between multiple main and stand-by sources of power. Any deviation in the threshold of supply levels being tolerated before a switch, can result in performance degradation, or even failure (e.g., significant reduction in usable life time of an autonomous system). Parametric shifts post HTOL are hence critical to analyse. The test requirements must be handled adaptively, depending upon which module / monitor reports the failure under which specific application. Also, since the power-up and monitoring sequences are not unique, an alternate sequence of measurements may be required to offset the HTOL fails. For representative SoC designs, such analyses have been routinely performed, and the HTOL sequence adapted to provide the best use-case analysis.

2) Application Specific Tests

In a system with multiple target applications, e.g. different power-up scenarios with different input supply levels, testing of every scenario is critical for the device qualification. In instances where the device has a reliability issue post HTOL, application scenarios are analysed to target specific tests where it is possible to have longer HTOL test time under lower stress for the same life-time requirements [5]. SoCs have been routinely subjected to such adaptive test methods to meet stringent and varying customer requirements without the need for gross over-design or re-design. It has been possible to target a specific application scenario (e.g. one with lower supply voltage level), based upon requirements. This adaptive startegy has also enabled qualification under multiple HTOL conditions with marginal test cost impact.

3) Adaptive Stress Test Targeting Power Management

Usually for cost reduction and faster cycle times, test hardware like BI boards are reused across several pin-compatible ICs. This causes test challenges for PM and other high power circuits [5]. Consider an LC based switching regulator. Given the switching nature of such circuits, at higher load requirements, its performance is very sensitive to package parasitics. Package parasitic inductances can result in higher

terminal voltage fluctuations causing catastrophic failures under stress test applications. To overcome this issue, an adaptive stress strategy with dynamic HTOL activation for lower load conditions and/or ICs with smaller package parasitics or those with a linear regulator, and static HTOL activiation for higher load conditions and/or ICs with higher package parasitics, has been used. Methods have been developed to formally derive equivalent static stress conditions that can result in the same amount of life-time stress application corresponding to a specific dynamic scenario.

III. Adaptive Calibration and Trims

As was seen in Section II, BGR circuits are widely used due to their higher insensitivity to power supply and temperature variations. However process variations and physical / topological mismatches induce large variations in reference voltages and currents across different dies on a wafer and across wafers, sometimes as high as ±100mV (of ~1.2V). In order to minimise such variations appropriate electrical parameters are trimmed. The trim code is usually stored in a non-volatile memory and re-used at every power-up of the device. The determination of the right trim code is an iterative process in which different trim codes are provided based on the observation of an appropriate electrical parameter of the circuit. The final trim code corresponds to the desired value, range and allowable error of this parameter. Apart from BGRs, other circuits whose performance are affected by process variations and hence require trimming include (i) I/Os for slew rate, overshoot and undershoot control, (ii) oscillators for frequency, duty cycle and jitter / phase noise control, (iii) line driver delay for packet error rate (PER) control, (iv) low noise amplifiers (LNA) and trans-conductance amplifiers (TA) for performance and current consumption .

A. Trim Procedure

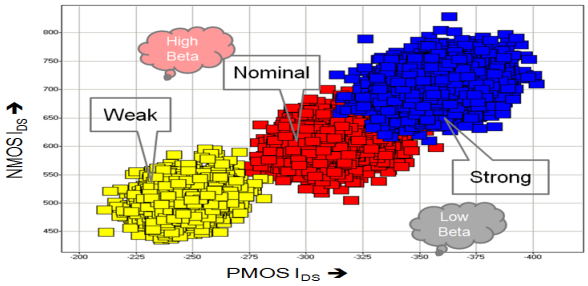

Fig. 2. I_{DS} of PMOS and NMOS in ODP determines the process corner

SoCs have multiple BGRs and power supplies to cater for several integrated analog, PM and RF functions, resulting in a large number of trimming procedures. In a representative design this can take upto 30% of the overall test time, which is often in excess of five seconds. There is hence a need to trim (and test) the DUT adaptively. The total number of trims required can be optimized. Integrated circuits today have built-in On-Die Process parameter monitor (ODP) circuits. The drain-source (I_{DS}) current of MOSFETs and the collector current (I_C) of BJTs in the ODP circuits determine the process corner of the device (hot / strong, cold / weak, nominal, high beta or low beta). Fig. 2 shows a typical spread of I_{DS} of NMOS versus PMOS transistors across a large sample of DUTs. The process corner information thus obtained can be used to either centre the process during manufacturing as well as to determine the right default values during the search procedures employed for trim. The order in which the various trims are carried out can also be changed for further optimization. In a typical flow, BGRs are first trimmed at the SOC level, followed by trims of BGRs in the RF IP cores, followed by other I/O and performance parameter trims. The BGRs are trimmed for magnitude as well as curvature variations. The trim procedure [3] is either search based or lookup table (LUT) based. The search based trim procedure uses a binary or linear search mechanism. A detailed study of the trim process for a representative SoC has revealed that some of the trims are ODP variation dependent i.e. knowing the type of device, the trim code can be directly applied without involving any search mechanism.

B. Trim Optimizations

In this representative SoC, the trim codes required for all BGRs on-chip have been analysed to understand the correlation between the codes. Given the similarity in the different BGR circuits, such correlation studies have revealed that the same trim code can be used across different BGR circuits "belonging to a group", thereby saving trim search time. A few possible approaches to trim time optimization are listed below.

1) Hybrid Search: The conventional trim process using binary or linear search is time consuming. The iterations can be reduced to almost half by using a hybrid (of binary and linear) search starting with an optimal initial trim code which is more closer to the final. This initial code is the mean trim code at any time at wafer test, and is used for follow-on wafers. This is more effective when the trim codes are tightly distributed. For example, given a trim range of 32, a mean trim code of 13 with a variation of ±2 observed at a particular time in wafer test can lead to the search getting completed (final trim code being ascertained) in just two iterations using the hybrid search method with 13 as an initial trim code, as compared to four iterations required using binary search with a deault trim code at mid-range.

2) Parallelism: The trims corresponding to those parameters which must be set independently, (i.e. do not depend upon any other trims), can be carried out in parallel, provided tester resources are available for the parametric measurements.

3) Procedural Optimization: Some of the trim procedures are differential in nature. A typical example is that of analog modules requiring quiescent current trims involving dual current measurements, first when enabled and the other when disabled. In such a situation a specific trim procedure optimization illustrated in Fig. 3 results in reduced test time. Start with all IPs disabled, and then enable one IP at a time additionally after each iteration. The current is measured under each condition. Such a procedure reduces the total number of measurements to N+1 as against 2*N iterations using conventional methods for N modules under trim test.

4) Code Reuse and Code Correlation: It is possible to reuse the trim code of a BGR for another BGR exactly or partially as a starting point of the search. It is also possible to correlate the trim codes with the ODP information using an LUT without requiring any searches.

5) On-Chip Measurement: An on-chip analog measurement (BIST) engine using a precision ADC with insignificant DFT overhead has also been implemented [1][2] to reduce the trim test time significantly by an order of magnitude.

Fig. 3. Trim procedure optimization illustrated with 5 IP current trims

C. Impact of Proposed Optimizations

TABLE I. CUMULATIVE IMPACT OF TRIM OPTIMIZATIONS

Trim type	Conventional trim time (ms)	Trim time with optimizations (ms)				
		Hybrid search	Code reuse	Parallelism	ODP correlate	Trim proc. Changes
BGR1	72.82	52.6	52.6	52.6	48.32	48.32
BGR2	13.84	11.56	NA	BGR1	NA	NA
DCDC1	15.12	13.04	NA	NA	12.65	NA
DCDC2	26.20	24.12	DCDC1	NA	NA	NA
AMP	4386	NA	NA	NA	NA	1686
Total	4513					1747

The cumulative impact of the proposed optimizations for trim is summarized in TABLE I. As can be seen from the table, the optimizations reduce trim test time by about 61%. With an optimized trim code set, the write time of non-volatile memory is also reduced significantly. Additionally, trim codes can also be directly derived from ODP data, using appropriate firmware routines.

IV. CONCURRENT TEST OF MULTIPLE RADIO CORES

The integration of multiple radios in an SoC complicates their testing, both in terms of test creation for concurrent operation and test application on the tester. This is due to three reasons: (a) Multiple radios result in co-existence issues which must be managed during both normal operation and test. (b) Supporting test requirements for different radios in turn requires different test interface and test application configurations, often resulting in more DFT in the SoC, more tester resources and more components on the test boards. It also directly impacts the multi-site factor (i.e. number of devices simultaneously tested in a tester). (c) The need to test these radios concurrently to optimise the test time and test cost further adds to the design and test constraints to be met.

A. Test Requirements

Compared to digital channels, low cost testers have limited RF channels. Hence they have to be shared across radios on a given die. Other trim calibration and power measurement requirements mandate additional components on the load board. As a result, it may be desirable to consider multiple insertions for RF test, one for each sub-set of the radios and the associated sub-set of tests to be applied concurrently. For example, a single X8 solution may require up to 20 s of test time, while a two insertion flow may require 18 s in x16 insertion and 4 s in x4 insertion, which results in an equivalent of just 17 s. The higher multi-site insertion can be used for those tests where the radios can be operated concurrently and where the tester resource requirements (e.g. CW sources) are fewer. However, the overheads due to another insertion (assumed 1 s in the example above) must be managed well, e.g. for different power-up sequences in different insertions.

B. Illustration for Multi Radio Core SoC

The concept of concurrency for RF tests has been proposed in [2]. It involves a hardware controller that lends itself naturally to adaptive test. The test schedule can be managed on-chip using an LUT based approach to denote the test compatibility matrix for various radio IPs, and also dynamically altered based on number of test applications and searches required (e.g. for different die lots at various process corners), without any change to the test program resident on the tester.

TABLE II. TEST TIMES WITH AND WITHOUT CONCURRENT OPERATION

Insertion	Test time (ms)						
	IP1	IP2	IP3	IP4	IP5	Total	Concur.
X16-TT	860	1064	1498	NA	NA	3422	2146
X4-TT	NA	1352	2215	730	2164	6461	3740
Resources	1	2	5	1	0		

An illustration of an SoC with five radio cores is shown in TABLE II. In the concurrent test flow, marked IPs are powered up simultaneously and each IP's test code is loaded into the memory sequentially, followed by concurrent execution of this test in those IPs on which these tests are compatible. The two insertion flow results in a potential savings of 40% when tests are applied concurrently across all IPs. Nine resources are split across the IPs; however, not more than eight are used in any insertion.

V. CO-EXISTENCE IN MULTI-CORE RADIOS

SoCs with multiple radio cores must address unique co-existence challenges due of inter-radio coupling, affecting the functionality of radios and the SoC. Such issues are often harder to detect since the coupling may happen only under specific operating conditions like power or frequency of operation, a specific combination of operating radios, etc. One radio can affect the performance of another radio in multiple ways. Causes include (i) direct interfering emission at transmitter port, (ii) SoC clock or its harmonics falling in-band of the receiver channels, (iii) unwanted clock harmonics appearing as spurs in the used frequency spectrum, (iv) interference amongst IPs in a power domain due to glitches at their shared supplies or references, (v) degradation in VCO affecting the PLL phase noise, and transmitter EVM and spectral masks in turn, (vi) performance degradation of critical

analog components due to supply, ground and substrate noise, etc. These issues must be addressed through design robustness, and corresponding adaptive test sequences.

A. Co-existence Analysis and Mitigation Methodology

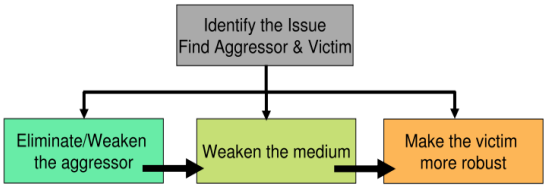

Fig. 4. Co-existence analysis and mitigation

Fig. 4 illustrates how co-existence issues are typically analysed and addressed. Some techniques employed to manage co-existence are summarized in TABLE III.

TABLE III. CO-EXISTENCE MITIGATION TECHNIQUES

	Weaken aggressor	Weaken medium	Shield victim
System level	Radio arch. Freq. planning Clock freq. management Protocol level mgmt.		Notch filter / spur cancel.
Circuit level	Decoupling caps Clock dithering / phasing		Differential analog circuits Increasing linearity
Physical level		Board / chip layout	Guard ring
	Package / Ballout Power domain planning		

At the system level, while performing multi-radio tests, co-existence issues can force design, specification and calibration updates. For example, shared antennae for two radios may prevent simultaneous transmit (Tx) and receive (Rx) operation. Further, the receiver should be blanked in the presence of a power amplifier (PA) operating from a nearby transmitter. This forces a specific protocol to be implemented in multi-radio SoCs to prevent saturation, blanking or jamming conditions.

At the circuit level, while testing multiple radios, the aggressor's clock or its harmonics can fall into the frequency spectrum of victim's receiver. This issue is addressed by adaptively switching the receiver frequency through an alternate PLL. A notch filter can also be used to adaptively block a specific frequency in the receiver.

B. Adaptivity at The Board Level

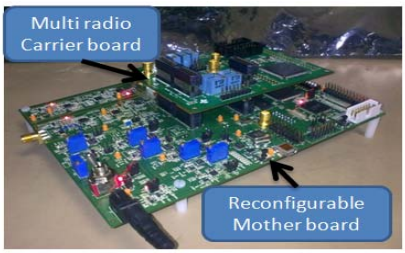

Fig. 5. Board configuration for multi-radio SoC test

The suitable board configuration and required set of instruments will vary across different tests. Fig. 5 shows a re-configurable bench for performance verification of multi-radio SoCs. The carrier board has different configurations for different radios (specifications, modes, process corners, and corresponding tests), stored in an EEPROM. Using this information, the mother board adaptively configures the power and test stimuli for the various radios. In the absence of such an arrangement, different boards may be required to support different configurations of operation of these radios altogether. Multiple radios in an SoC also pose correlation issues between bench based characterisation data and ATE based production test data. This is due to many reasons, the important ones being: (i) differences in ATE multi-site and concurrent test configurations, (ii) differences in external components, sockets and board layouts, and (iii) differences in test interfaces and sequences. Hence appropriate guard bands and local correction factors have to be applied for better correlation. Thus also the test acceptance criteria become adaptive.

VI. ADAPTIVE RF TEST MEASUREMENTS

While increasing integration of multiple radios into one SoC may result in many potential co-existence problems as seen in Section V, it also provides opportunity for significant test cost reduction and adaptive test configurations.

A. Loopback Configurations for RF Test

Loopback is a classic example of DFT in the analog / RF test domain where on-chip stimuli and response generation are used for test cost reduction. The presence of multiple radios on die helps achieve loopback across various interfaces. For example, with Bluetooth (BTH) and WLAN operating in the same frequency band, Tx and Rx can be looped back across BTH and WLAN.

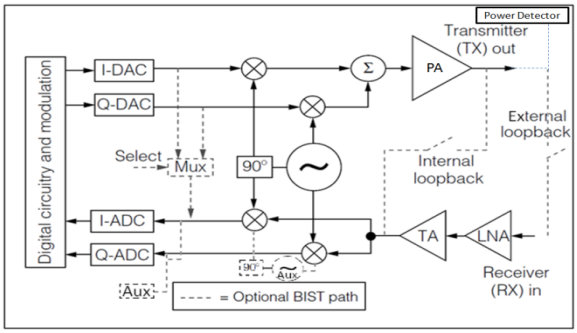

Fig. 6. Block diagram of WLAN RF module

Fig. 6 shows an example of Tx and Rx signal chain in a WLAN module with multiple loopback paths [6] (marked as optional BIST paths) along with alternate signal sources or detectors (e.g. auxiliary oscillator, LDO, power detector). The three loopback paths that are commonly used are: (a) between DAC and ADC, (b) internal loopback between mixers on both Tx and Rx and power amplifier (PA) on integrated Tx, and (c) external loopback to cover the entire Tx and Rx signal chain (including the antenna).

Moving to smaller geometries has resulted in mandatory tuning of the signal chain components to improve the yield and operate at optimal power-performance operating conditions. Adaptivity in test is no longer restricted to test sequences, but also extends to the choice of test paths exercised and choice of tuning parameters. There is a trade-off between test time, multi-site test factor attainable, tester instrumentation required and test coverage obtained in the three loopback schemes. For example, though external loopback test mimics the real world

test requirement, signals have to be brought out to external pads / balls for external measurement, and routed back to the chip. An on-chip power detector can instead be used. These requirements, along with traces that require signal conditioning and impedance matching using additional components, limit the extent of multi-site test possible. However, this support is needed for devices which must be calibrated (per die) for peak power. On the other hand, in case of internal loopback test, we can target multiple adaptive tests such as linearity, gain, offset, filter correction, mismatch correction and calibration, using which either the faulty block in the chain can be identified or the design can be tuned for the right operating point for the best possible performance during the test itself. In the case of data converters, loopback tests are done in production to test for parametric RF specifications.

Adaptivity in the test paths may arise on a per-die basis when the choice of loopback paths is determined based upon the die characteristics. For dies with blocks that require complex trims *(e.g. due to non-linearity issues in PA or sensitivity issues in LNA)* enabled through iterative test and tuning procedures, external loopback may not suffice and direct control and measurements with ATE are required. Similarly, for dies where oscillators require iterative tests for tuning, both internal and external loopbacks may not suffice. For dies which require complex linearity corrections to the data convertors, even DAC→ADC loopback may not suffice.

Implementing such path adaptivity requires die / wafer / lot index based automated identification of potential issues in the signal chain components based on data collected over a large set of samples. One such technique [7] is to automatically predict the performance of Bluetooth radio based on the die-location. Using these loopback paths and additional signal processing (such as re-use of on-chip FFT engines) and data storage, various Tx parameters (e.g. EVM) and Rx parameters (e.g. BER, NF) may be measured on-chip [6], [8], [9].

B. Adaptive Power-Performance Tuning

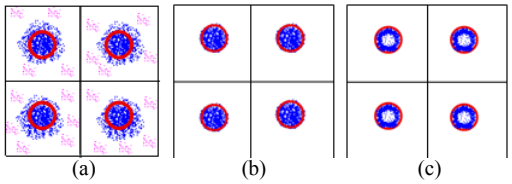

Fig. 7. Power-Yield optimization with EVM

An illustration using an adaptive EVM test for power-yield optimization is shown in Fig. 7 for four points of the constellation diagram of a OFDM transmitter. Fig. 7(a) indicates the EVM constellation diagram of an unoptimized / power failed die. The red circle is the specification bound, i.e. EVM requirement for the standard. The blue points within the circle indicate good points that meet the EVM requirements and those outside indicate marginal failing points. The red points far away from the circle indicate gross fails. Fig. 7(b) indicates the constellation diagram of a "good" die with no power optimization on good points (but with possible yield optimization to include marginally failing points). Fig. 7(c) indicates the constellation diagram of an optimally tuned "good" die that maximally reduces power on good points while meeting performance specification. In such a scheme, the performance of "good" dies is degraded to reduce power with almost zero error (within the data sheet specification). The parameters to tune (or adaptively control) are amongst bias currents of LNA [10] (for the receiver), PA (for the transmitter), jitter parameters of oscillators, and trim bits of other components in the Tx and / or Rx signal path that affect EVM and sensitivity.

VII. CONCLUSIONS

In this paper, various techniques for adaptive test of multi-core RF SoCs have been reviewed. This paper highlights the need and scope for adaptive test scheduling and test management techniques to meet the varying requirements imposed by test / characterization, pass-fail acceptance criteria, and bounds set by affordable test solutions, namely test cost / test time, tester / board infrastructure, and power / co-existence across radio modules. Many of these techniques have been implemented in recent designs, and are silicon proven; some others are newly proposed, and planned to be incorporated in newer designs.

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