Carbon Nanotube Circuits: Opportunities and Challenges

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Abstract— **Carbon Nanotube Field-Effect Transistors (CNFETs) are excellent candidates for building highly energy-efficient digital systems. However, imperfections inherent in carbon nanotubes (CNTs) pose significant hurdles to realizing practical CNFET circuits. In order to achieve CNFET VLSI systems in the presence of these inherent imperfections, careful orchestration of design and processing is required: from device processing and circuit integration, all the way to large-scale system design and optimization. In this paper, we summarize the key ideas that enabled the first experimental demonstration of CNFET arithmetic and storage elements. We also present an overview of a probabilistic framework to analyze the impact of various CNFET circuit design techniques and CNT processing options on system-level energy and delay metrics. We demonstrate how this framework can be used to improve the energy-delay-product (EDP) of CNFET-based digital systems.**

Keywords—Carbon Nanotube; CNT; CNFET; Nanotechnology; Modeling; Imperfection; Variation; Three-Dimensional Circuits;

I. INTRODUCTION

Energy efficiency, often expressed in terms of performance per watt [Laudon 05, Rivoire 07], is a key driver for a vast majority of digital systems, from embedded computing systems to server clouds. Due to their excellent electrostatic and transport properties, carbon nanotube field-effect transistors (*CNFETs*) are excellent candidates for building highly energy-efficient digital systems of the future [Wei 09a, Franklin 12a]. Moreover, CNFET fabrication is compatible with conventional semiconductor fabrication techniques [Patil 09c, Park 12], while enabling new circuit integration techniques such as monolithic three-dimensional ICs [Wei 09b].

Figure 1 shows a typical CNFET device structure. Each carbon nanotube (*CNT*) in a CNFET acts as the transistor channel, whose conductance is modulated by the gate. The gated regions of the CNTs can be undoped, while the source and drain regions are heavily doped. Figure 2 shows an inverter circuit using CNFETs. The gate, source and drain contacts, active region, and interconnects are defined by conventional lithography. The spacing between CNTs is determined by the CNT growth process rather than by lithography, and can therefore be much smaller than the lithographic pitch.

While CNFET circuits are expected to offer an order of magnitude benefit in energy-delay-product (*EDP*) over silicon CMOS circuits [Wei 09a, Franklin 12a], substantial imperfections inherent in CNTs pose significant hurdles to realizing practical CNFET circuits:

1. It is nearly impossible to precisely align and position all CNTs at VLSI scale. This limitation can cause stray conducting paths that result in incorrect logic functionality. Moreover, the CNT density distribution cannot be accurately controlled. CNT density variations can result in CNFET circuit performance variations and functional failures.
2. Metallic CNTs (*m-CNTs*) have zero or near-zero bandgap, and therefore cause source-to-drain shorts in CNFETs. CNFETs that contain m-CNTs result in excessive circuit leakage power or even incorrect circuit functionality.
3. CNFET circuits can suffer from large performance variations, reduced yield, and increased susceptibility to noise due to several sources of process variations (Sec. IV).

Today's CNT processing alone is inadequate to overcome these challenges. The synergy between CNT processing and CNFET circuit design, referred to as the **imperfection-immune design paradigm**, overcomes these challenges by creating CNFET digital VLSI circuits that are immune to these substantial imperfections [Mitra 09, Patil 09a, Wei 11, Zhang 12]. This approach enabled the first experimental demonstration of functional CNFET circuits: 1. VLSI-compatible CNFET arithmetic elements and latches [Patil 09b, Patil 11], 2. Monolithic 3D-ICs using CNFETs [Wei 09b], and 3. Sensor interface circuit built entirely using CNFETs [Shulaker 13]. Other CNFET circuit demonstrations include ring-oscillators on a single CNT [Chen 06], decoder circuits based on percolation transport [Cao 08], and adder circuits on a single CNT [Ding 12a].

To achieve the predicted EDP benefits of CNFET circuits, new solutions spanning device processing, circuit fabrication and integration, and system design optimization are required:

Device processing: *High-performance CNFETs* require major advances in three key areas: 1. High-density (200 CNTs/μm) aligned CNTs (no CNTs crossing each other) [Franklin 12a], 2. p- and n-type doping in the source and drain regions with tunable doping levels, and 3. Low metal-to-CNT contact resistance. These challenges are discussed in Sec. II.

Circuit fabrication and integration: *Scalable CNFET circuit integration* requires all CNFET fabrication and processing techniques to be VLSI-compatible (Sec. III).

Joint exploration of CNT processing and CNFET circuit design: CNFET systems with high energy efficiency and small delay variations require joint exploration of CNT processing and CNFET circuit design techniques to minimize the impact of process variability on system performance, power, and yield (Sec. IV).

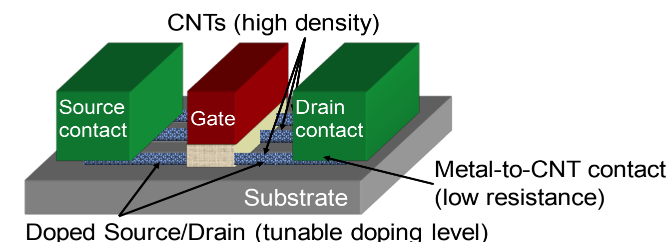

Figure 1. Ideal CNFET device structure.

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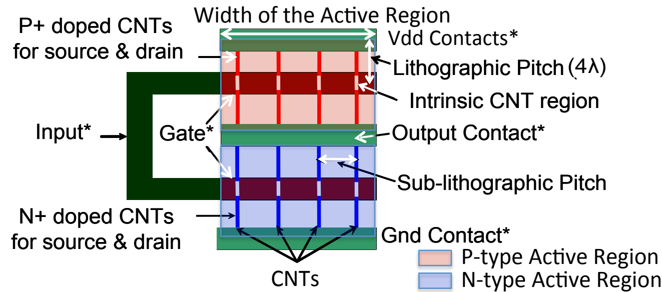

Figure 2. CNFET inverter. *Lithographically defined.

II. Device Processing: High-Performance CNFETs

The CNTs in a CNFET provide high carrier velocity (v_F=1×10^8 cm/s) for high current drive [Wong 11] and nanometer-thin body for excellent electrostatic control [Deng 07a]. Recent studies [Franklin 12a] show that, with 200 CNTs/μm, sub-10nm CNFETs can potentially outperform silicon CMOS transistors, including silicon nanowires, silicon FinFETs, and silicon ETSOI (Extremely Thin Si on Insulator) FETs. CNFETs have also been experimentally demonstrated to operate at a very low supply voltage of 0.4V [Ding 12b]. Gate-All-Around structure has also been achieved for improved gate control and reduced hysteresis in CNFETs [Franklin 12b].

For CNFET-based digital systems, [Wei 09a] shows that the CNFET technology can offer a 5-fold delay advantage **for the same power consumption** (across a wide range of power consumption values from 10mW to 100W) compared to the silicon MOSFET (partially-depleted SOI) at the 11nm technology node for a high-performance multi-core processor. The realization of such an ideal CNFET technology requires advances in three key areas: CNT density, doping, and contact resistance.

A. *CNT Density Enhancement*

CNT density, the number of CNTs that connect the source and drain regions of a CNFET per unit width of the active region (Fig. 2), determines the drive current density (to the first order). One way to grow CNTs is through a high-temperature CVD process [Patil 09c, Xiao 09]. Using patterned catalyst stripes on a quartz wafer (Fig. 3), CNT arrays can be grown with 99.5% CNT alignment (Fig. 3a) [Patil 09c]. After CNT growth on quartz wafers, CNTs are transferred onto a target substrate (e.g. a silicon wafer) for circuit fabrication (Fig. 4) [Patil 09c]. (This transfer technique is a low-temperature process and can therefore be used in a unique way for monolithic CNFET 3D-ICs as detailed in Sec. III.C).

Existing CNT growth techniques achieve typical CNT densities ranging from 3–5 CNTs/μm for each CNT growth, with peak densities up to 30 CNTs/μm observed in local areas [Wong 11]. While researchers are making continued efforts to increase CNT density from a single growth [Lu 11], promising progress has been made through multiple-growth [Hong 10] or multiple-transfer [Shulaker 11, Wang 10] techniques.

Multiple-growth techniques reuse the same growth substrate (e.g. quartz) and increase CNT density through multiple iterations of the same growth process. The highest reported density from multiple-growth techniques is 45 CNTs/μm [Hong 10], still less than the target of 200 CNTs/μm required to achieve the projected EDP benefits of CNFETs [Franklin 12a].

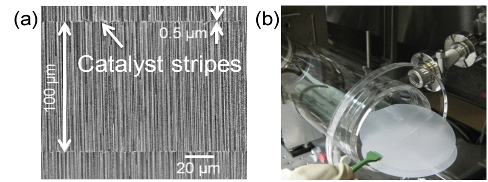

Figure 3. (a) Scanning Electron Microscopy (SEM) images of aligned array of CNTs. (b) Furnace used for CNT growth.

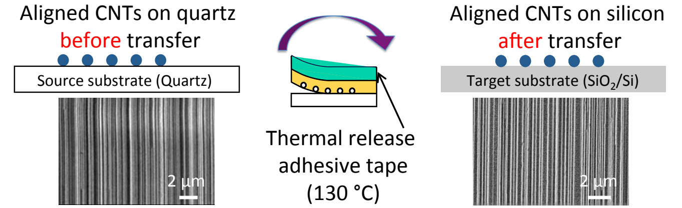

Figure 4. Transfer process for aligned CNTs. Both density and alignment of CNTs are preserved after the transfer process.

Multiple-transfer techniques (shown in Fig. 5a) transfer CNTs multiple times from multiple source substrates (e.g. multiple quartz wafers used for CNT growth) to the same destination substrate (e.g. a silicon wafer). For any multiple-transfer technique, it is important that the increase in density is linear with the number of transfers performed. Otherwise, there may exist a limitation to the maximum current density achievable. CNFET current density must also increase proportionally with increased CNT density. This was recently achieved by a new multiple-transfer technique that uses a thin sacrificial layer between every transferred layer of CNTs to maintain CNT alignment between successive transfers [Shulaker 11]. Up to 5 transfers with associated linear CNT density and linear increases in CNFET current values were experimentally demonstrated (Fig. 5) [Shulaker 11]. Using a multiple-transfer technique, the highest density for aligned CNTs is reported to be 55 CNTs/μm [Wang 10].

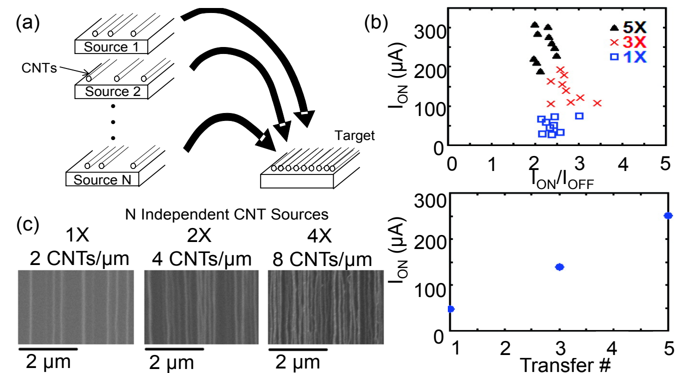

Figure 5. CNT multiple-transfer technique with linear increase of CNT density and CNFET drive current. (a) Overview of the multiple-transfer process. CNTs from several growth substrates are transferred onto the same target wafer. The increase in CNT density on the target wafer is proportional to the number of transfers performed. (b) Linear increase in CNFET drive current. (c) SEM images of samples with 1X, 2X, 4X transfers.

B. *n-Type Doping and p-Type Doping*

Complementary CNFETs are required for highly efficient digital circuits. While stable high-performance p-type CNFETs have been demonstrated through high work-function metal contacts [Javey 03], the realization of high-performance n-type CNFETs that are stable in ambient air still remains a challenge.

Recent work has demonstrated functional n-type CNFETs through: 1. Low work-function metal contacts (Er, Yr [Shahrjerdi 11], Sc [Zhang 08], and Ga [Wang 11]), and 2. ALD-based electrostatic doping [Moriyama 10, Franklin 12b]. Low work-function metals support electron transport through the conduction band of CNTs, providing excellent n-type behavior. However, these metals are highly reactive and a passivation layer is required to prevent oxidation [Shahrjerdi 11]. ALD-based electrostatic doping involves shifting the CNT conduction band using positive fixed charge in high-k dielectrics [Moriyama 10]. This process has yet to be optimized to retain charges at high temperatures for robust circuits.

C. Low Metal-to-CNT Contact Resistance

Low metal-to-CNT contact resistance is important to obtain large CNFET drive current density. The lowest theoretically achievable contact resistance is 6.5kΩ, the quantum limit [Franklin 10]. Current challenges in achieving this limit are mainly: 1. Non-ideal wetting of metal to the CNT (gaps might exist between the metal and CNT surface, acting as tunneling barriers for electrical conduction [Chai 12]), and 2. The Schottky-Barrier (*SB*) between metal and the CNT due to band misalignment (the barrier for electron and hole conduction, similar to silicon CMOS transistors) [Pierret 96]. While efforts are being made in reducing the SB through careful selection of contact metal with the proper work-function [Javey 03, Zhang 08], promising progress has been achieved through improvement of metal-to-CNT wetting. Graphitic carbon interfacial layers are used to increase the contact area between metal and the CNT [Chai 12], resulting in 11-fold reduction in contact resistance with high drive current density and steep sub-threshold swing at room temperature.

III. Circuit Fabrication and Integration

A. Overcoming Challenges of Mis-Positioned CNTs

Mis-positioned CNTs can introduce stray conducting paths, resulting in incorrect logic functionality of CNFET logic circuits. With the *mis-positioned CNT-immune* circuit design technique [Patil 08], functional logic circuits can be built with guaranteed correct functionality. This technique is VLSI-compatible since it does not require die-specific customization, and can utilize existing VLSI design methodologies.

B. Overcoming Challenges of m-CNTs

The presence of m-CNTs causes excessive leakage current and degrades the noise margin of CNFET digital circuits [Zhang 09b]. While preferential growth of 100% semiconducting CNTs (*s-CNTs*) is ideal, today's selective CNT growth results in <97% s-CNTs [Qu 08, Parker 12]. Even with less than ideal growth, however, it has been shown that at least 99.99% of grown m-CNTs must be removed for CNFET digital VLSI [Zhang 09b].

Existing solution-based s-CNT enrichment techniques [LeMeiux 08] can greatly reduce the percentage of m-CNTs, but not enough to satisfy the requirement of 99.99% m-CNT removal. Another option is to remove m-CNTs after CNT growth from an ensemble of m-CNTs and s-CNTs. [Collins 01] introduces a current-induced electrical breakdown technique to remove m-CNTs from individual CNFETs. We refer to this technique as *Single-Device electrical Breakdown* or *SDB*. SDB achieves close to 100% m-CNT removal, but suffers from major VLSI challenges [Patil 09b]: 1. It is impractical to contact the gate, source, and drain of each CNFET individually in gigascale ICs, and 2. m-CNT fragments can produce incorrect logic functionality.

To overcome the drawbacks of SDB, a new imperfection-immune design technique, called *VLSI-compatible Metallic-CNT Removal* (*VMR*) is introduced in [Patil 09b, Wei 10a]. In the VMR technique, a special layout called the VMR structure is created so that m-CNT electrical breakdown can be performed simultaneously for a large number of CNFETs. Next, parts of the VMR structure are etched out to create the final circuit. VMR does not require any die-specific customization. [Patil 09b] proves that any arbitrary logic can be created using VMR, as long as any two CNFETs in series inside a library cell are connected by a contact at minimum pitch.

Experimental results demonstrate that VMR can effectively remove 99.99% of m-CNTs to reproducibly fabricate multiple-CNT CNFETs that exhibit high I_{on}/I_{off} of 10^3 to 10^5 ($I_{on}/I_{off} < 10$ before m-CNT removal). VMR is compatible with the mis-positioned CNT-immune design technique in [Patil 08]. These techniques enabled the first experimental demonstration of VLSI-compatible imperfection-immune CNFET arithmetic and storage circuits [Patil 11]. As CNFETs scale down to the sub-10nm regime, the effectiveness of current-induced m-CNT breakdown from Joule heating [Collins 01] – the mechanism for m-CNT removal in VMR – needs to be further examined.

C. CNFET Monolithic 3D-IC Demonstration

CNFETs provide an exciting opportunity for monolithic 3-dimensional ICs (3D-ICs), where multiple layers of circuits are integrated on the same wafer and conventional vias are used as Inter-Layer Vias or *ILVs* (vias that connect circuits on different layers) [Batude 11, Wei 09b, Wong 07]. Compared to 3D integration techniques that use Through Silicon Vias (*TSVs*) [Borkar 11, Motoyoshi 09], monolithic 3D integration offers two orders of magnitude increase in ILV density [Batude 11], allowing gate-level 3D integration.

Recent advances in imperfection-immune CNFET VLSI [Zhang 12] have enabled CNFET-based monolithic 3D-ICs. The use of the low-temperature transfer technique [Patil 09b] (Sec. II) decouples the high-temperature CNT growth from the low-temperature device/circuit fabrication (Fig. 4). [Wei 09b] demonstrates, for the first time, monolithic 3D-ICs using CNFETs (Fig. 6). The interconnects can be fabricated using conventional wires or CNTs. With the maximum processing temperature of 250°C, CNFET circuits spanning 3 layers have been successfully demonstrated, where conventional vias (instead of TSVs) are used as ILVs for connecting circuits on different layers.

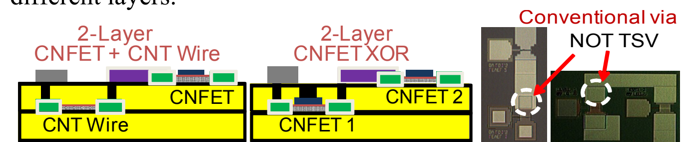

Figure 6. Monolithic 3D-ICs using CNFETs and CNT interconnects [Wei 09b].

IV. Joint Exploration of CNT Processing and CNFET Circuit Design

In addition to process variations that exist for silicon CMOS transistors (such as channel length, oxide thickness,

and threshold voltage variations), CNFETs are subject to *CNT-specific variations*, such as variations in *CNT type (m- or s-CNT)* [Zhang 09b], *CNT diameter* [Zhang 09a, Wei 10b], *CNT density* [Kang 07, Zhang 09a], *CNT alignment* [Patil 09c], and *CNT doping*. To quantify the impact of CNT-specific variations on the overall critical path delay variations of CNFET digital VLSI circuits, a probabilistic modeling and analysis framework is developed in [Zhang 11]. Using this framework, [Zhang 11] shows that CNT-specific variations can degrade the projected speed benefits of CNFET circuits by up to 60% at the 16nm technology node. We overcome this significant challenge by exploring CNT processing improvement options together with CNFET circuit design techniques (Sec. IV.D).

A. CNT-Specific Variations

CNT-specific variations are summarized in Fig. 7. For example, the on-current of a CNFET containing only a single CNT is quite sensitive to CNT diameter variations. However, CNFETs in practical circuits require multiple CNTs in order to achieve high on-current values. Due to statistical averaging, such CNFETs are not very sensitive to variations in diameter, alignment, and doping. The main source of CNFET on-current variation (and consequently delay variation) is the variation in *CNT count* (the number of CNTs in a CNFET). CNT count variations are caused by: 1. Grown CNT density variations (non-uniform spacing between CNTs on the substrate), and 2. m-CNT-induced variations (variations in the remaining CNT count after m-CNT removal using techniques such as VMR [Patil 09b]).

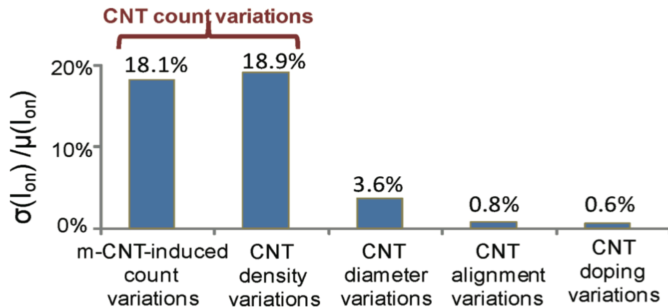

Figure 7. Relative contributions of CNT-specific variations to CNFET on-current variations (details in [Zhang 11]).

CNT processing parameters used to quantify CNT count variations are summarized in Table I. The CNT count inside a CNFET with width W is denoted by $N(W)$. Based on renewal theory [Cox 62], a parameterized model is presented in [Zhang 09a] for the distribution of $N(W)$. A key parameter for describing grown CNT density variations is the *Index of Dispersion Count* (*IDC*), defined as $IDC = \sigma^2[N(W)]/\mu[N(W)]$ [Zhang 11]. Note that, *IDC* is independent of W [Zhang 09a]. The well-known Poisson distribution has $IDC = 1$. The experimentally extracted *IDC* value for the CNT growth in [Zhang 09a] is about 0.5, showing less variability than the Poisson process. Small *IDC* values are critical for reducing CNFET circuit delay variations (Sec. IV.D).

An important aspect of CNT count variations is the (asymmetric) correlation in CNT count between certain CNFETs [Lin 10, Zhang 09a]. As discussed in Sec. II, CNTs are generally aligned. Based on the relative positioning of CNFETs, their CNT counts can either be highly correlated (if they share the same set of CNTs) or uncorrelated (if they do not share any CNTs). This creates complications when performing statistical timing analysis in the presence of CNT count variations. However, clever sampling techniques (details in [Zhang 11]) can overcome these challenges. This asymmetric correlation property can also be effectively utilized to "engineer" correlations between certain CNFETs through special layout designs to increase yield and reduce delay variations [Zhang 10].

TABLE I. CNT PROCESSING PARAMETERS [ZHANG 11].

Processing parameter	*Description*	*Ideal value*	*Experiment value*
IDC	Index of Dispersion of Count in CNT count variations	0	0.5 [Zhang 09b]
p_m	Probability that a given (grown) CNT is an m-CNT	0%	10% [Li 04]
p_{Rs}	Probability that a CNT is removed, given it is an s-CNT	0%	<5% [Patil 09b]
p_{Rm}	Probability that a CNT is removed, given it is an m-CNT	100%	>99.99% [Patil 09b]

B. CNFET Compact Model

The probabilistic framework in [Zhang 11] is based on a variation-aware timing model for CNFET logic gates, which is developed using the CNFET device model [SPICE]. In order to relate the CNT count variations to the CNFET logic gate delay variations, [Zhang 11] runs simulations over various CNT counts for each CNFET in a logic gate, and then models the resulting delay as a function of the CNT counts. To facilitate such variation-aware design, computationally efficient CNFET compact models, e.g. a SPICE model, are essential. A publicly available CNFET SPICE model [SPICE] was developed in [Deng 07a, 07b] for circuit design and performance projections. This SPICE model takes into account acoustic and optical phonon scattering in the channel region and the screening effect between multiple CNTs. It has been calibrated to experimental data with 90% accuracy [Amlani 06].

C. Variation-Aware Design for CNT Digital Systems

CNT count variations can lead to *CNT count failure*, in which case no s-CNT exists in a CNFET. *Count-limited yield* refers to the probability that **all** CNFETs in a circuit contain at least one s-CNT. A naïve solution of upsizing CNFETs increases count-limited yield, but imposes high energy costs [Zhang 10]. Instead, a unique design opportunity exists due to the asymmetric CNT correlation from aligned CNT growth [Patil 09c, Xiao 09]: CNFETs whose active regions are aligned along the CNT direction share the same set of CNTs, and therefore have highly correlated CNT counts [Lin 10, Zhang 09a] (Fig. 8). If the CNT counts of multiple CNFETs are correlated, then so are their individual probabilities of CNT count failure. As a result, the probability that at least one of these CNFETs has CNT count failure **decreases** [Zhang 10]. Therefore, engineering more CNT count correlation between CNFETs can improve count-limited yield. The "aligned-active" layout technique [Zhang 10] leverages this unique opportunity to reduce CNT count failures by aligning the active regions of

all CNFETs along the direction of the aligned CNTs (Fig. 8). This layout technique achieves more than an order of magnitude reduction in CNT count failure probability (and, hence, energy costs to achieve high yield) with little area impact [Zhang 10].

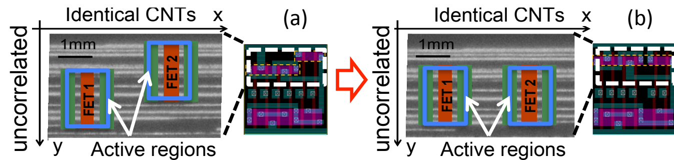

Figure 8. Aligned-active layout technique to increase count-limited yield. AOI222_X1 standard cell [Nangate] is shown before (a) and after the active regions of the CNFETs have been aligned (b). Note that, the CNT direction is horizontal in this case.

D. Overcoming CNFET Circuit Delay Variations

While the aligned-active layout can effectively improve count-limited yield, CNT count variations also lead to a significant increase in circuit delay variations [Zhang 11]. The *delay penalty* metric quantifies the increase in delay due to CNT count variations, and is defined as:

$$delay\ penalty = 100\% \times \left(\frac{T_{95}}{nominal\ delay} - 1\right),$$

where T_{95} is the 95% percentile point of the critical path delay distribution of a circuit. To overcome this challenge, joint exploration of CNT processing improvement options (processing parameters in Table I) and CNFET circuit design (upsizing techniques in conjunction with aligned-active layout design) is performed (details in [Zhang 11]). Figure 9 shows an example of various such "processing routes" that can be obtained as a result of this joint exploration.

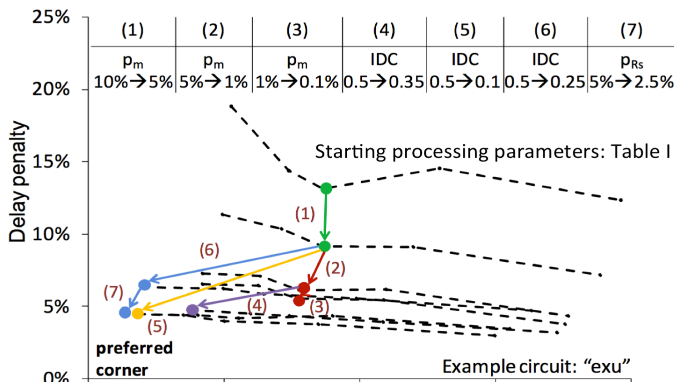

Figure 9. Processing parameter exploration at the 16nm node for the "exu" circuit block of the OpenSPARC T2 SoC design [OpenSPARC]. Parameter p_{Rm} (Table I) is assumed to be 99.99% for all cases. Each of the arrows represents a specific improvement of a processing parameter, labeled and listed at the top of the figure. Two possible processing routes are shown to minimize both delay and energy penalties: Route A: (1)→(2)→(3), and Route B: (1)→(6)→(7).

As shown in Fig. 9, for example, Route A represents the traditional thinking of continuously reducing p_m to very small values (0.1% in Fig. 9). However, this route suffers from diminishing returns and the resulting benefits saturate. In contrast, Route B represents an attractive option with delay penalty of less than 5% and less than 5% increase in energy at the 16nm node (while ensuring high yield using the aligned-active layout). Figure 9 shows that reducing *IDC* leads to large improvements in energy and delay penalties. While existing efforts in CNT growth focus on the average CNT density, it is also critical to focus on the evaluation and reduction of *IDC* values for CNT growth.

V. Conclusion

CNFETs are promising candidates for building highly energy-efficient digital systems. However, inherent CNT imperfections impose significant challenges to building practical CNFET circuits. Improvements in device processing will continue to play a critical role in making the CNFET technology practical. However, as outlined in this paper, the energy efficiency benefits of CNFETs can be fully realized through advances in device processing, imperfection-immune CNFET circuit design, and joint exploration and optimization of synergies between CNT processing and CNFET circuit design techniques.

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