Near-Threshold Voltage Design in Nanoscale CMOS

Vivek De
Circuits Research Lab
Intel Corporation

Near-Threshold Voltage (NTV) operation of a CMOS design is defined as the voltage-frequency operating point where the energy consumed per compute operation (pJ/op) reaches a minimum, or the energy efficiency (Mops/Watt) peaks. Typically, this operating voltage is above the nominal threshold voltage of the transistor. The peak efficiency is achieved by a balance of switching energy and idle or leakage energy.

A complex design that achieves the best overall energy efficiency at NTV must deploy circuit techniques that are sufficiently robust at low voltages against process variations and noises while minimizing area/capacitance overheads. Transistor characteristics need to be targeted optimally. Impacts from die-to-die and within-die variations must be considered. NTV operations across different workload activity profiles should be comprehended at runtime via dynamic platform control. Fine-grain power management techniques are essential to minimize leakage energy.

We present a complex microprocessor [1] in 32nm planar CMOS and a SIMD accelerator engine [2] in 22nm CMOS logic process technology featuring tri-gate transistors [3-4] that demonstrate NTV operation while achieving a wide dynamic operating range. Tri-gate device characteristics such as improved DIBL and steeper subthreshold swings enable robust low-voltage operation and offer significantly reduced leakage power. Circuit and design techniques that can mitigate failures at low voltages due to supply noises, temperature excursions, aging-induced degradations, as well as workload and activity changes are discussed. In particular, techniques for dynamic adaptation to environmental variations, and error detection, preemption and response are introduced. Fine-grain power delivery and management are essential for maximizing the overall energy efficiency at NTV. Efficient voltage regulators, fast voltage control and low-overhead implementations of multiple voltage domains are a must for realizing the full potential of NTV designs.

References

[1] Shailendra Jain, et al., "A 280mV-to-1.2V wide-operating-range IA-32 processor in 32nm CMOS,", *Solid-State Circuits Conference Digest of Technical Papers [ISSCC], 2012 IEEE International,* pp. 66 – 68, 2012

[2] Steven Hsu, et al., "A 280mV-to-1.1V 256b reconfigurable SIMD vector permutation engine with 2-dimensional shuffle in 22nm CMOS," *Solid-State Circuits Conference Digest of Technical Papers [ISSCC], 2012 IEEE International*, pp. 178 – 180, 2012

[3] C. Auth, et al., "A 22nm high performance and low power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," *2012 IEEE Symposium on VLSI Technology*, pp. 131-132, 2012

[4] C.-H. Jan, et al., "A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications", *2012 IEEE International Electron Devices Meeting (IEDM) Technical Digest,* pp. 44-47, 2012

978-3-9815370-0-0/DATE13/©2013 EDAA