

technical programme topic chairs

System Specifications, Models and Methodologies

Andy Pimentel
Amsterdam U, NL
Dominique Borrione
TIMA Laboratory, FR

System Design, Synthesis and Optimization

Jan Madsen
TU Denmark, DK
Luciano Lavagno
Politecnico di Torino, IT

Simulation and Validation

Valeria Bertacco
U of Michigan, US
Franco Fummi
Verona U, IT

Design of Low Power Systems

Tudor Murgan
Intel Mobile Communications, DE
Domenik Helmels,
OFFIS, DE

Power Estimation and Optimisation

Massimo Poncino,
Politecnico di Torino, IT
Jian-Jia Chen,
Karlsruhe Institute of Technology, DE

Emerging Technologies, Systems and Applications

Yuan Xie
Penn State U, US
Sanjukta Bhanja
South Florida U, US

Formal Methods and Verification

Wolfgang Kunz
TU Kaiserslautern, DE
Gianpiero Cabodi
Politecnico di Torino, IT

Network on Chip

Davide Bertozzi
Ferrara U, IT
Federico Angiolini
iNoCs, CH

Architectural and Microarchitectural Design

Laura Pozzi
Lugano U, CH
Tulika Mitra
National U of Singapore, SG

Architectural and High-Level Synthesis

Paolo Ienne
EPF Lausanne, CH
Philippe Coussy
U de Bretagne-Sud/Lab-STICC, FR

Reconfigurable Computing

Fadi Kurdahi
UC Irvine, US
Marco Platzner
Paderborn U, DE

Logic and Technology Dependent Synthesis

Jordi Cortadella,
Barcelona Tech, ES
Sachin Sapatnekar,
Minnesota U, US

Physical Design and Verification

Ralph Otten
TU Eindhoven, NL
Azadeh Davoodi
Wisconsin-Madison U, US

Analogue and Mixed-Signal Systems and Circuits

Catherine Dehollain,
EPF Lausanne, CH
Günhan Dündar
Bogazici U, TR

Interconnect, EMC, EMD and Packaging Modelling

Nick van der Meij
TU Delft, NL
Stefano Grivet-Talocia
Politecnico di Torino, IT

Computing and Green IT Systems

Tajana Simunic Rosing
UC San Diego, US
Ayse Kivilcim Coskun
Boston U, US

Communication, Consumer and Multimedia Systems

Frank Kienle
TU Kaiserslautern, DE
Matthias Sauer
Intel Technologies, DE

Transportation, Management and Energy Generation Systems

Marco Di Natale
Scuola Superiore Sant'Anna, IT
Davide Brunelli
University of Trento, IT

Medical and Healthcare Systems

Chris Van Hoof
IMEC, BE
Yihui Chen
ETH Zuerich, CH

Secure Systems

Jérôme Quévremont
Thales, FR
Patrick Schaumont
Virginia Tech, US

Reliable and Reconfigurable Systems

Jose Ayala
Complutense U of Madrid, ES
Marco Domenico Santambrogio
Politecnico di Milano, IT

Industrial Experiences Brief Papers

Enrico Macii
Politecnico di Torino, IT
Ahmed Jerraya
CEA Leti, FR

Test for Defects, Variability, and Reliability

Sandip Kundu
Massachusetts U, US
Bram Kruseman
NXP Semiconductors, NL

Test Generation, Simulation and Diagnosis

Nicola Nicolici
McMaster U, CA
Grzegorz Mrugalski
Mentor Graphics Poland, PL

Test for Mixed-Signal, Analog, RF, MEMS

Hans Kerkhoff
Twente U, NL
Abhijit Chatterjee
Georgia Tech U, US

Test Access, Design-for-Test, Test Compression, System Test

Sybille Hellebrand
Paderborn U, DE
Rohit Kapur
Synopsys, CH

On-Line Testing and Fault Tolerance

Cecilia Metra
Bologna U, IT
Lorena Anghel
TIMA Laboratory, FR

Real-time, Networked and Dependable Systems

Giuseppe Lipari
Scuola Superiore Sant'Anna, IT
Peter Puschner
TU Wien, AT

Compilers and Software Synthesis for Embedded Systems

Bjoern Franke
Edinburgh U, UK
Heiko Falk
Ulm U, DE

Model-Based Design and Verification for Embedded Systems

Wang Yi
Uppsala U, SE
Saddek Bensalem
Joseph Fourier U, FR

Embedded Software Architectures

Gabriela Nicolescu
Ecole Polytechnique de Montreal, CA
Oliver Bringmann
FZI Karlsruhe, DE

Cyber-Physical Systems

Samarjit Chakraborty
TU Munich, DE
Anton Cervin
Lund U, SE